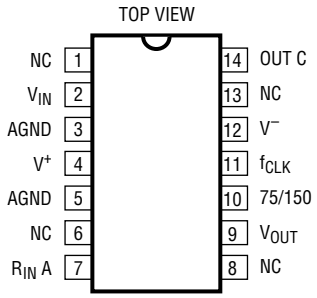
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 400mW
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Operating Temperature Range
LTC1064-3M **(OBSOLETE)** ..... –55°C to 125°C
LTC1064-3C ..... –40°C to 85°C
Input Voltage ..... (V^+ +0.3V) to V^- –0.3V)
Burn-In Voltage 15V

PACKAGE/ORDER INFORMATION

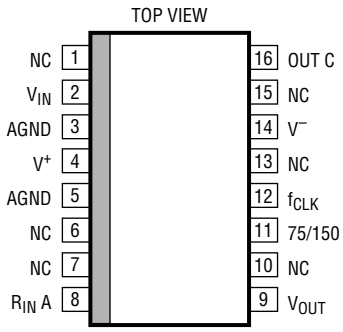


N PACKAGE
14-LEAD PDIP
T_{JMAX} = 110°C, θ_{JA} = 70°C/W

J PACKAGE
14-LEAD CERDIP

OBSOLETE PACKAGE
Consider the N 14 Package for Alternate Source

ORDER PART NUMBER
LTC1064-3CN
LTC1064-3MJ LTC1064-3CJ



SW PACKAGE
16-LEAD PLASTIC (WIDE) SO
T_{JMAX} = 150°C, θ_{JA} = 90°C/W

ORDER PART NUMBER
LTC1064-3CSW

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±7.5V, 75:1, f_{CLK} = 2MHz, R1 = 10k, TTL or CMOS clock input level unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain	Referenced to 0dB, 1Hz to 1kHz	●	–0.5		0.15	dB
Gain TempCo				0.0002		dB/°C
–3dB Frequency	50:1 (f_{CLK} /f_{-3dB} = 75)			26.67		kHz
	100:1 (f_{CLK} /f_{-3dB} = 150)			13.34		kHz
Gain at –3dB Frequency	Referenced to 0dB, f_{IN} = 26.67/13.34kHz	●	–3.8		–2.75	dB
Stopband Attenuation	At 3f_{-3dB}	●	–25	–29		dB
Stopband Attenuation	At 5f_{-3dB}	●	–56	–60		dB
Stopband Attenuation	At 7f_{-3dB}			–84		dB
Input Frequency Range	100:1		0		<f_{CLK}/2	kHz
	50:1		0		<f_{CLK}	kHz
Output Voltage Swing and Operating Input Voltage Range	V_S = ±2.37V	●	±1.1			V
	V_S = ±5V	●	±3.1			V
	V_S = ±7.5V	●	±5			V
Total Harmonic Distortion	V_S = ±5V, Input = 1V_{RMS} at 1kHz			0.015		%
	V_S = ±7.5V, Input = 3V_{RMS} at 1kHz			0.03		%
Wideband Noise	V_S = ±5V, Input = GND 1Hz – 1.99MHz			55		μV_{RMS}
	V_S = ±7.5V, Input = GND 1Hz – 1.99MHz			60		μV_{RMS}

ELECTRICAL CHARACTERISTICS

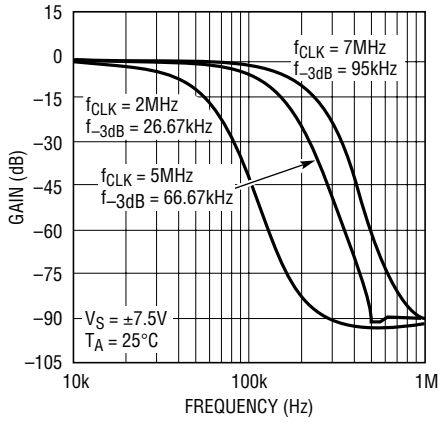
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±7.5V, 75:1, f_{CLK} = 2MHz, R1 = 10k, TTL or CMOS clock input level unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output DC Offset Output DC Offset TempCo	V_S = ±7.5V V_S = ±5V V_S = ±7.5V			±30 ±20 ±50	±150	mV µV/°C µV/°C
Input Impedance			14	22		kΩ
Output Impedance	f_{OUT} = 10kHz			2		Ω
Output Short-Circuit Current	Source/Sink			3/1		mA
Clock Feedthrough				200		μV_{RMS}
Maximum Clock Frequency	V_S ≥ ±7V, 50% Duty Cycle V_S ≥ ±7V, 50% Duty Cycle, T_A = <55°C				5 7	MHz MHz
Power Supply Current	V_S = ±2.37V, f_{CLK} = 1MHz V_S = ±5V, f_{CLK} = 1MHz V_S = ±7.5V, f_{CLK} = 1MHz 	● ● ●		10 12 16 	22 23 26 28 32	mA mA mA mA mA
Power Supply Voltage Range		●	±2.37		±8	V

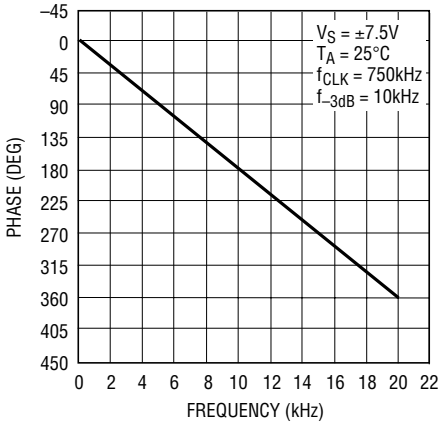
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

TYPICAL PERFORMANCE CHARACTERISTICS

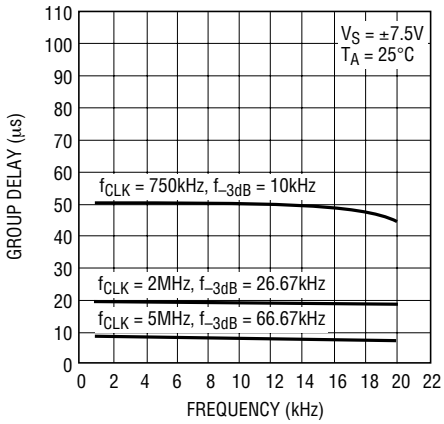
Gain vs Frequency



Phase vs Frequency

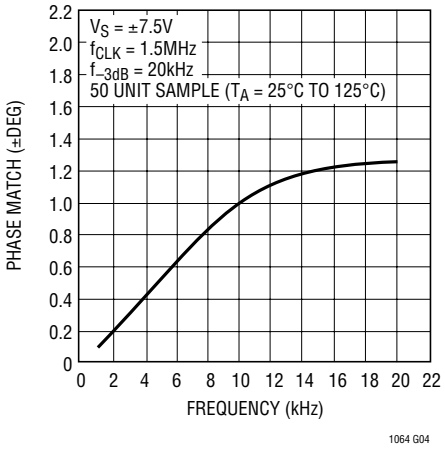


Group Delay

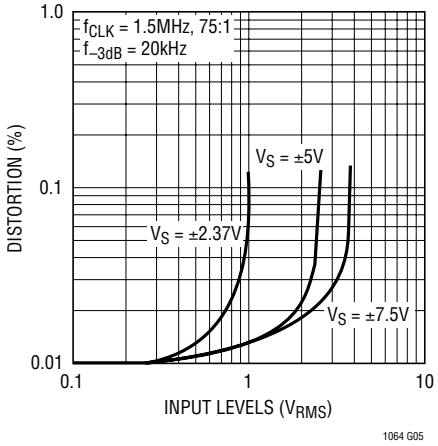


TYPICAL PERFORMANCE CHARACTERISTICS

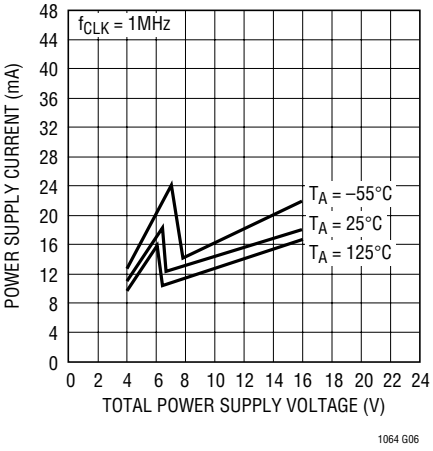
Phase Matching



Total Harmonic Distortion



Power Supply Current vs Power Supply Voltage



Transient Response
Input $10V_{P-P}$ Square Wave
V_S = ±7.5V, Pin 10 to V^+,
f_{CLK} = 1.5MHz

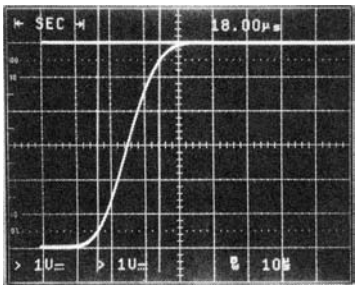


Table 1. Wideband Noise (μV_{RMS})

		V_S = ±2.37V	V_S = ±5V	V_S = ±7.5V
Pin 10 to	f_{CLK}/f_{-3dB}	Noise μV_{RMS}	Noise μV_{RMS}	Noise μV_{RMS}
V^+	75/1	50	55	60
V^-	150/1	52	58	62
GND	120/1	45	50	54

TYPICAL PERFORMANCE CHARACTERISTICS

Table 2. Gain/Phase, f_{-3dB} = 1kHz, LTC1064-3 Typical Response V_S = ±5V, T_A = 25°C, f_{CLK} = 75kHz, Pin 10 at V^+ (fltr 75:1)

FREQUENCY (kHz)	GAIN (dB)	PHASE (deg)
0.500	–0.858	–90.430
1.000	–2.990	179.200
1.500	–6.840	89.600
2.000	–12.780	3.800
2.500	–20.800	–71.000
3.000	–29.900	–129.600
3.500	–38.800	–173.700
4.000	–47.100	152.600
4.500	–54.700	126.000
5.000	–61.600	103.300
5.500	–68.000	85.190
6.000	–73.840	69.060
6.500	–79.250	54.780
7.000	–84.230	42.440
7.500	–88.940	30.060
8.000	–93.360	21.300
8.500	–97.510	10.000
9.000	–100.880	1.520
9.500	–105.780	–7.820

Table 3. Gain/Delay, f_{-3dB} = 1kHz, LTC1064-3 Typical Response V_S = ±5V, T_A = 25°C, f_{CLK} = 75kHz, Pin 10 at V^+ (fltr 75:1)

FREQUENCY (kHz)	GAIN (dB)	DELAY (ms)
0.200	–0.281	0.502
0.300	–0.420	0.503
0.400	–0.610	0.503
0.500	–0.860	0.502
0.600	–1.160	0.502
0.700	–1.530	0.502
0.800	–1.950	0.503
0.900	–2.430	0.503
1.000	–2.990	0.500
1.100	–3.610	0.500
1.200	–4.300	0.500
1.300	–5.060	0.498
1.400	–5.920	0.495
1.500	–6.830	0.491
1.600	–7.840	0.489
1.700	–8.930	0.481
1.800	–10.130	0.473
1.900	–11.410	0.465
2.000	–12.780	0.454

Table 4. Gain/Phase, f_{-3dB} = 1kHz, LTC1064-3 Typical Response V_S = ±5V, T_A = 25°C, f_{CLK} = 150kHz, Pin 10 at V^- (fltr 150:1)

FREQUENCY (kHz)	GAIN (dB)	PHASE (deg)
0.500	–0.955	–88.100
1.000	–3.380	–175.300
1.500	–7.570	99.700
2.000	–13.770	20.100
2.500	–21.800	–48.000
3.000	–30.700	–100.700
3.500	–39.400	–139.900
4.000	–47.600	–169.200
4.500	–55.100	168.300
5.000	–61.900	150.300
5.500	–68.260	135.830
6.000	–74.050	123.660
6.500	–79.450	113.440
7.000	–84.330	104.440
7.500	–89.010	97.670
8.000	–93.250	91.580
8.500	–97.340	84.670
9.000	–101.390	74.600
9.500	–104.980	75.990

Table 5. Gain/Delay, f_{-3dB} = 1kHz, LTC1064-3 Typical Response V_S = ±5V, T_A = 25°C, f_{CLK} = 150kHz, Pin 10 at V^- (fltr 150:1)

FREQUENCY	GAIN (dB)	DELAY (ms)
0.200	–0.284	0.490
0.300	–0.450	0.489
0.400	–0.670	0.489
0.500	–0.960	0.487
0.600	–1.310	0.487
0.700	–1.730	0.485
0.800	–2.210	0.484
0.900	–2.750	0.482
1.000	–3.380	0.478
1.100	–4.070	0.478
1.200	–4.820	0.475
1.300	–5.660	0.470
1.400	–6.580	0.467
1.500	–7.570	0.463
1.600	–8.640	0.456
1.700	–9.790	0.448
1.800	–11.050	0.438
1.900	–12.360	0.428
2.000	–13.770	0.417

TYPICAL PERFORMANCE CHARACTERISTICS

Table 6. Gain/Phase, f_{-3dB} = 1kHz, LTC1064-3 Typical Response V_S = ±5V, T_A = 25°C, f_{CLK} = 120kHz, Pin 10 at GND (fltr 120:1)

FREQUENCY (kHz)	GAIN (dB)	PHASE (deg)
0.500	–0.994d	–82.210
1.000	–3.050	–162.800
1.500	–6.520	116.700
2.000	–12.180	40.200
2.500	–19.460	–23.600
3.000	–27.200	–74.000
3.500	–34.700	–114.200
4.000	–41.900	–146.800
4.500	–48.700	–173.300
5.000	–55.100	164.700
5.500	–60.900	145.800
6.000	–66.500	130.610
6.500	–71.660	117.130
7.000	–76.390	105.880
7.500	–80.910	96.140
8.000	–84.900	87.510
8.500	–88.750	81.380
9.000	–92.410	78.190
9.500	–98.290	52.860

Table 7. Gain/Delay, f_{-3dB} = 1kHz, LTC1064-3 Typical Response V_S = ±5V, T_A = 25°C, f_{CLK} = 120kHz, Pin 10 at GND (fltr 120:1)

FREQUENCY (kHz)	GAIN (dB)	DELAY (ms)
0.200	–0.354	0.458
0.300	–0.520	0.456
0.400	–0.730	0.454
0.500	–1.000	0.452
0.600	–1.320	0.449
0.700	–1.670	0.448
0.800	–2.090	0.446
0.900	–2.540	0.446
1.000	–3.050	0.445
1.100	–3.600	0.446
1.200	–4.220	0.449
1.300	–4.900	0.448
1.400	–5.670	0.447
1.500	–6.520	0.446
1.600	–7.470	0.441
1.700	–8.500	0.432
1.800	–9.650	0.422
1.900	–10.870	0.409
2.000	–12.180	0.395

Table 8. Gain/Phase, f_{-3dB} = 20kHz, LTC1064-3 Typical Response V_S = ±7.5V, f_{CLK} = 1.5MHz, Pin 10 at V^+(fltr 75:1)

T_A = 25°C			T_A = 125°C		
FREQUENCY (kHz)	GAIN (dB)	PHASE (deg)	FREQUENCY (kHz)	GAIN (dB)	PHASE (deg)
10.000	–0.912	–92.270	10.000	–0.944	–92.880
20.000	–3.090	176.000	20.000	–3.170	175.500
30.000	–6.910	85.500	30.000	–6.910	85.700
40.000	–12.710	–1.200	40.000	–12.450	–0.600
50.000	–20.500	–77.800	50.000	–19.920	–78.000
60.000	–29.400	–138.700	60.000	–28.500	–140.700
70.000	–38.300	174.600	70.000	–37.200	170.500
80.000	–46.500	138.300	80.000	–45.300	132.200
90.000	–54.000	109.100	90.000	–52.700	100.900
100.000	–61.000	84.800	100.000	–59.600	74.900
110.000	–67.310	64.040	110.000	–65.900	52.600
120.000	–73.170	46.260	120.000	–71.750	32.850
130.000	–78.600	31.120	130.000	–77.170	15.840
140.000	–83.760	18.050	140.000	–82.370	1.130
150.000	–88.630	7.770	150.000	–87.400	–11.380

PIN FUNCTIONS (Pin Numbers Refer to the 14-Pin Package)

NC (Pins 1, 6, 8 and 13): The "no connection" pins should be preferably grounded. These pins are not internally connected.

V_{IN}, V_{OUT} (Pins 2, 9): The input Pin 2 is connected to an 18k resistor tied to the inverting input of an op amp. Pin 2 is protected against static discharge. The device's output, Pin 9, is the output of an op amp which can typically source/sink 3mA/1mA. Although the internal op amps are unity gain stable, driving long coax cables is not recommended.

When testing the device for noise and distortion, the output, Pin 9, should be buffered (Figure 1). *The op amp power supply wire (or trace) should be connected directly to the power source. To eliminate switching transients from filter output, buffer filter output with a third order lowpass (see Figure 5).*

AGND (Pins 3, 5): For dual supply operation these pins should be connected to a ground plane. For single supply operation both pins should be tied to one half supply (Figure 3).

V^+, V^- (Pins 4, 12): Should be bypassed with a 0.1μF capacitor to an adequate analog ground. Low noise, nonswitching power supplies are recommended. *To avoid latchup when the power supplies exhibit high turn-on transients, a 1N5817 Schottky diode should be added from the V^+ and V^- pins to ground (Figure 1, 2 and 3).*

R_{IN} A, OUT C (Pins 7, 14): A very short connection between Pin 7 and Pin 14 is recommended. This connection should be preferably done under the IC package. In a breadboard, use a one inch, or less, shielded coaxial cable: the shield should be grounded. In a PC board, use a one inch trace or less; surround the trace by a ground plane.

50/100 (Pin 10): Ratio Pin.The DC level at this pin determines the ratio of clock frequency to the –3dB frequency of the filter. The ratio is 75:1 when Pin 10 is at V^+, 120:1 when Pin 10 is at GND and 150:1 when Pin 10 is at V^-. This pin should be bypassed with a 0.1μF capacitor to analog ground when it's connected to V^- or V^+ (Figure 1). See Tables 2 through 8 for typical gain and delay responses for the three ratios.

f_{CLK} (Pin 11): For ±5V supplies the logic threshold level is 1.4V. For ±8V and 0V to 5V supplies the logic threshold levels are 2.2V and 3V respectively. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock "on" time can be as low as 200ns. The maximum clock frequency for ±5V supplies is 4MHz. For ±7V supplies and above, the maximum clock frequency is 7MHz. Do not allow the clock levels to exceed the power supplies. For single supply operation ≥6V use level shifting at Pin 11 with T^2L levels (see Figure 4).

TYPICAL APPLICATIONS

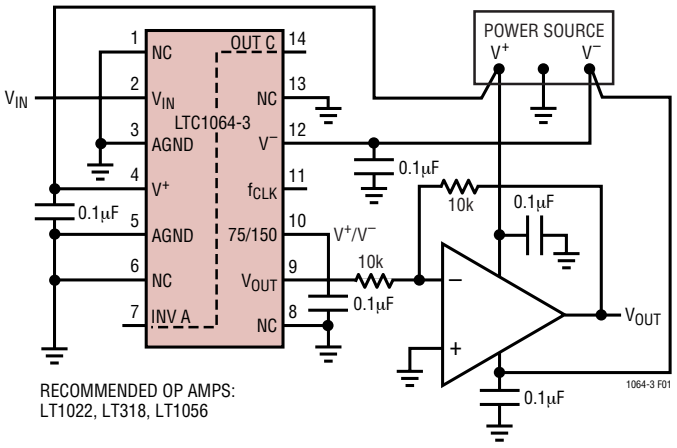


Figure 1. Buffering the Filter Output. The Buffer Op Amp Should Not Share the LTC1064-3 Power Lines

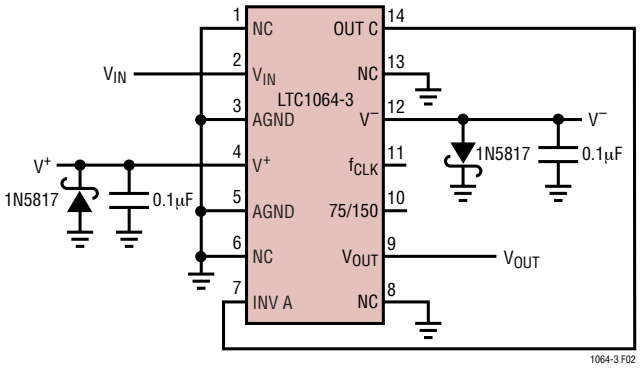


Figure 2. Using Schottky Diodes to Protect the IC from Power Supply Reversal

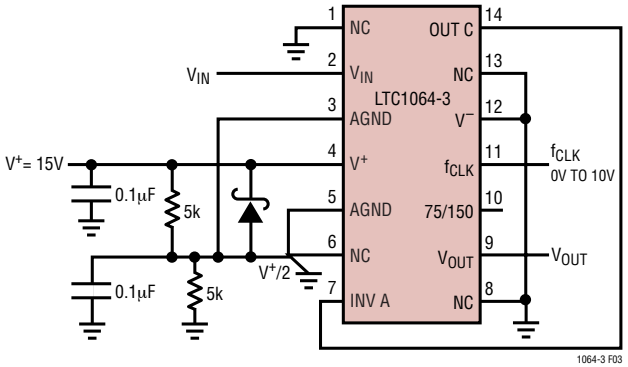


Figure 3. Single Supply Operation. If Fast Power Up or Down Transients are Expected, Use a 1N5817 Schottky Diode Between Pin 4 and Pin 5

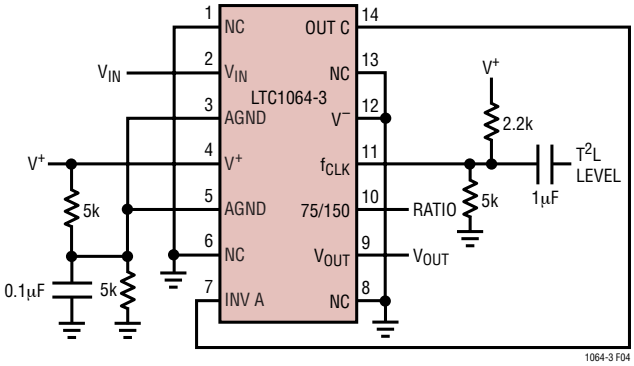


Figure 4. Level Shifting the Input T²L Clock for Single Supply Operation ≥6V

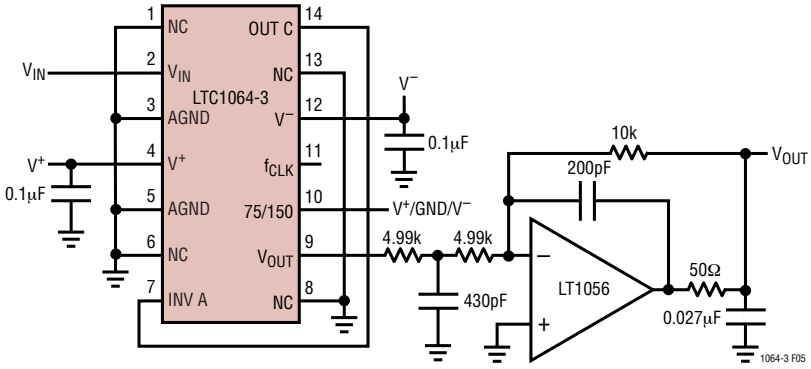
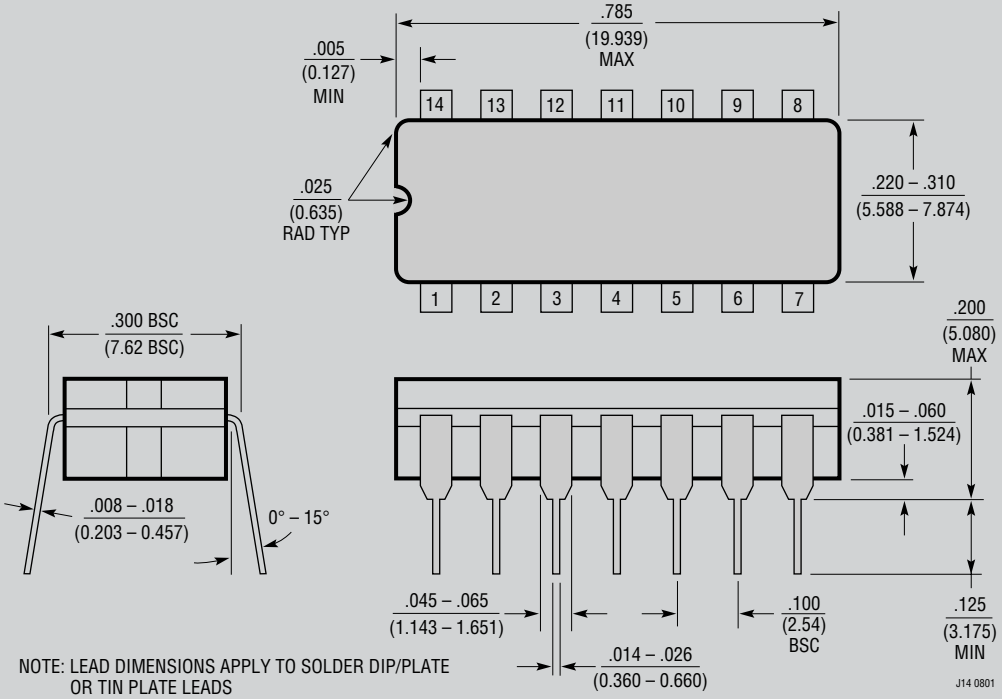


Figure 5. Adding an Output Buffer-Filter to Eliminate Any Clock Feedthrough. Passband ±0.1dB to 50kHz, –3dB at 94kHz

PACKAGE DESCRIPTION

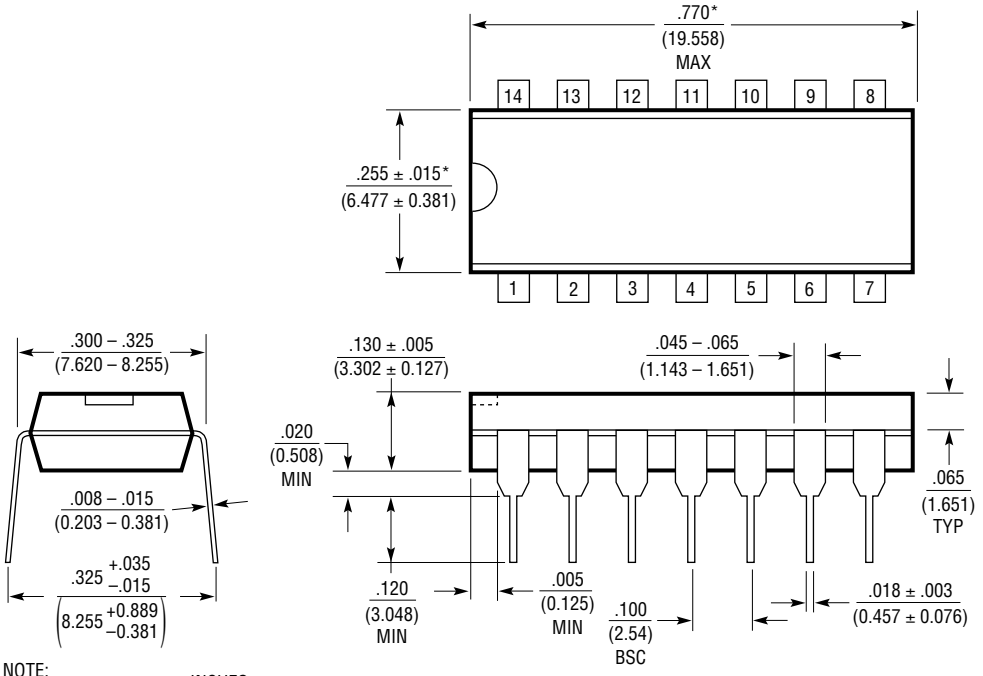
J Package
14-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

PACKAGE DESCRIPTION

N Package
14-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

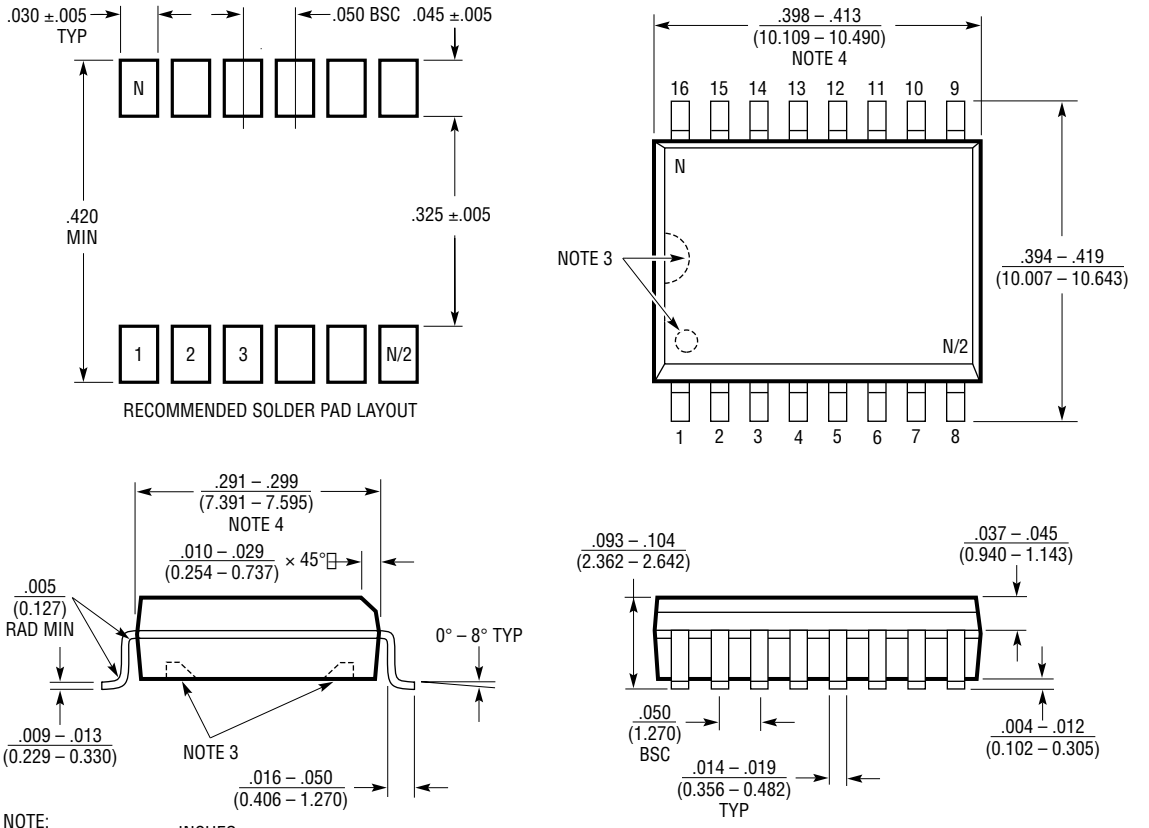


NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

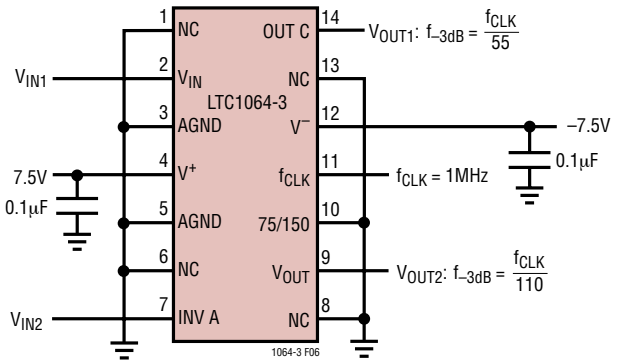
SW Package
16-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



S16 (WIDE) 0502

NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

TYPICAL APPLICATIONS



Amplitude Response

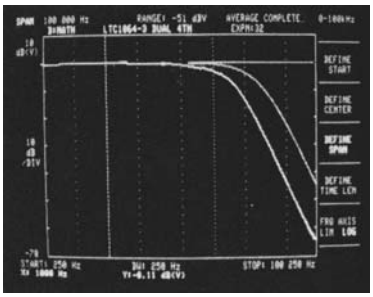


Figure 6. Dual 4th Order Bessel Filters. V_S = ±7.5V, f_{CLK} = 1MHz, Pin 10 to GND. f_{-3dB} = 9kHz and 18kHz

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1069-7	8th Order Linear Phase Lowpass	S0-8 Package
LTC1563	Active RC, 4th Order Bessel Lowpass	Continuous Time, Resistor Programmable Cutoff
LTC1569-6	DC Accurate, 10th Order Lowpass	Linear Phase, Internal Precision Clock, S0-8 Package
LTC1569-7	DC Accurate, 10th Order Lowpass	Linear Phase, Internal Precision Clock, S0-8 Package

Linear Technology Corporation
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