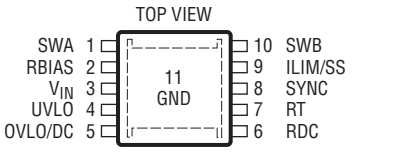
ABSOLUTE MAXIMUM RATINGS (Note 1)

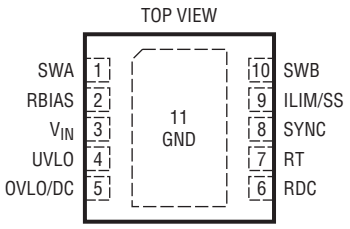
SWA, SWB ..... –0.3V to 80V
V_{IN}, UVLO ..... –0.3V to 60V
OVLO/DC, SYNC ..... –0.3V to 8V
Operating Junction Temperature Range (Note 2)
LT3999E ..... –40°C to 125°C
LT3999I ..... –40°C to 125°C
LT3999H ..... –40°C to 150°C
LT3999MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
10-LEAD PLASTIC MSOP

θ_{JA} = 40°CW, θ_{JC} = 10°CW
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

θ_{JA} = 43°C/W, θ_{JC} = 5.5°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3999EMSE#PBF	LT3999EMSE#TRPBF	LTGKR	10-Lead Plastic MSOP	–40°C to 125°C
LT3999IMSE#PBF	LT3999IMSE#TRPBF	LTGKR	10-Lead Plastic MSOP	–40°C to 125°C
LT3999HMSE#PBF	LT3999HMSE#TRPBF	LTGKR	10-Lead Plastic MSOP	–40°C to 150°C
LT3999MPMSE#PBF	LT3999MPMSE#TRPBF	LTGKR	10-Lead Plastic MSOP	–55°C to 150°C
LT3999EDD#PBF	LT3999EDD#TRPBF	LGKQ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3999IDD#PBF	LT3999IDD#TRPBF	LGKQ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply and Shutdown						
V_{IN} Minimum Operating Voltage		●			2.7	V
V_{IN} Overvoltage Lockout	Internal, Rising	●	36	40	42	V
V_{IN} Supply Current	(Note 3)			4.3		mA
V_{IN} Shutdown Current	V_{UVLO} = 0.3V			0.1	1	µA
UVLO Threshold (Rising)		●	1.15	1.25	1.35	V
UVLO Hysteresis				125		mV
UVLO Pin Current	V_{UVLO} = 1.25V			10	100	nA
OVLO/DC Threshold (Rising)		●	1.15	1.25	1.35	V
OVLO/DC Hysteresis				125		mV
OVLO/DC Pin Current	$V_{OVLO/DC}$ = 1.25V			10	100	nA
Power Switches (SWA, SWB)						
Switch Saturation Voltage	I_{SW} = 1A			350		mV
Switch Current Limit	Internal Default	●	1.0	1.4	1.7	A
Non Overlap Time				70		ns
Switch Base Drive Current	I_{SW} = 1A			35		mA
Oscillator/Sync						
Switching Frequency	R_T = 316k R_T = 49.9k R_T = 12.1k	●	280	50 300 1000	320	kHz kHz kHz
Synchronization Frequency Range			100		1000	kHz
SYNC Voltage Threshold				1.5		V
SYNC Pin Input Resistance				200		kΩ
ILIM/SS						
SWA and SWB Current Limit	$R_{ILIM/SS}$ = 43.2k	●	0.4	0.5	0.6	A
ILIM/SS Pin Current				10		µA
Duty Cycle						
Switch Duty Cycle	OVLO/DC = 0.8V, R_{DC} = 24.3k, R_T = 49.9k OVLO/DC = 0.612V, R_{DC} = 24.3k, R_T = 49.9k OVLO/DC = 0.3V, R_{DC} = 24.3k, R_T = 49.9k	●	22	20 25 48	30	% % %

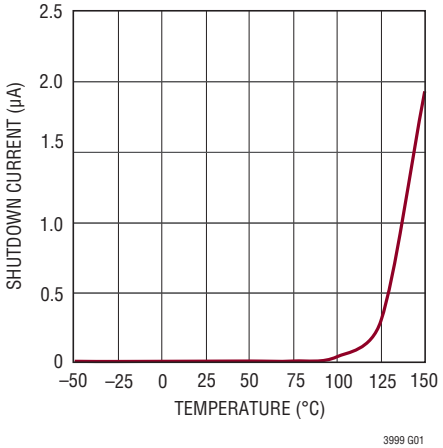
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect the device reliability and lifetime.

Note 2: The LT3999E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT3999I Is guaranteed over the –40°C to 125°C operating junction temperature range. The LT3999H is guaranteed over the full –40°C to 150°C operating junction temperature range. The LT3999MP is 100% tested and guaranteed over the –55°C to 150°C junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C.

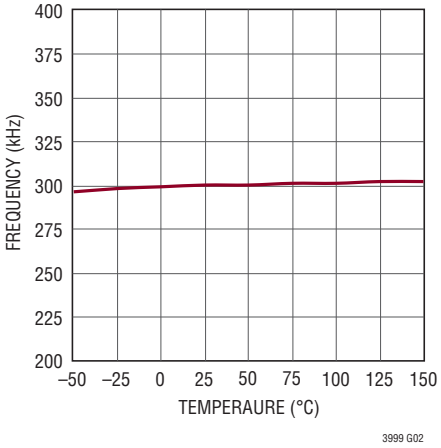
Note 3: Supply current specification does not include switch drive currents. Actual supply currents will be higher.

TYPICAL PERFORMANCE CHARACTERISTICS

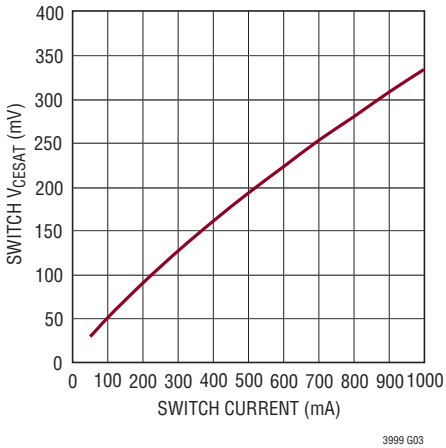
V_{IN} Shutdown Current



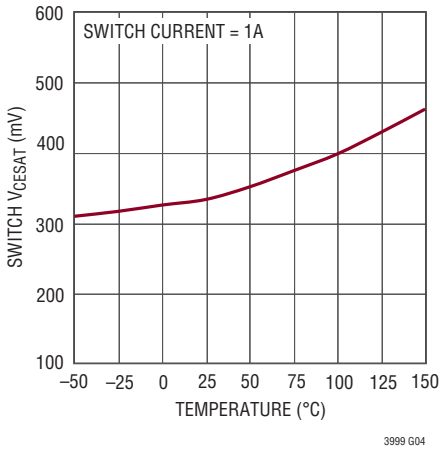
Switching Frequency



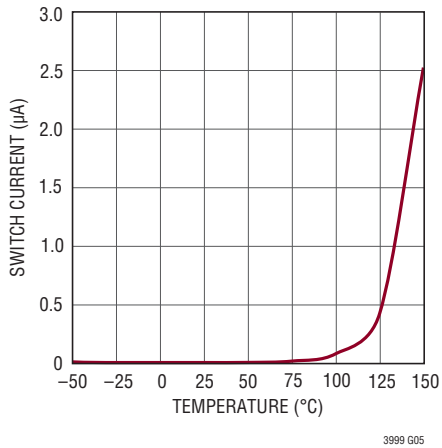
V_{CESAT} vs Switch Current



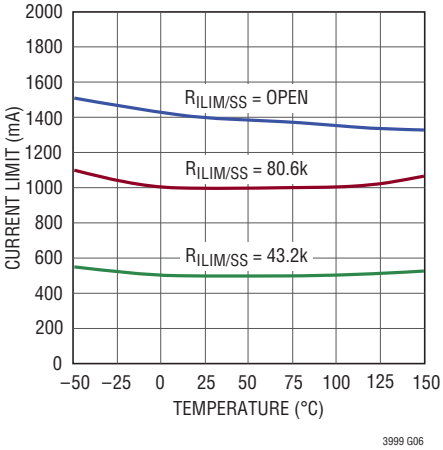
Switch V_{CESAT}



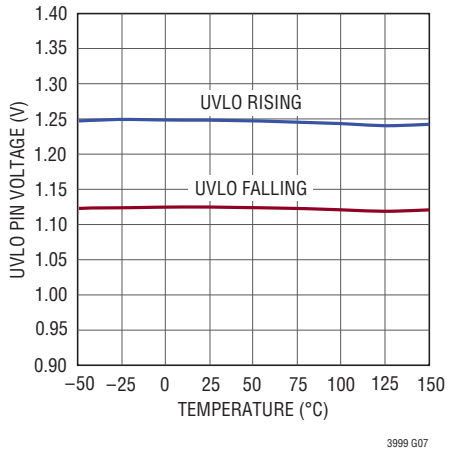
Switch Leakage Current



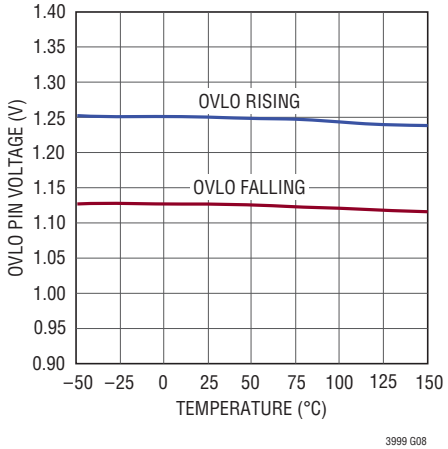
Switch Current Limit



UVLO Threshold Voltage

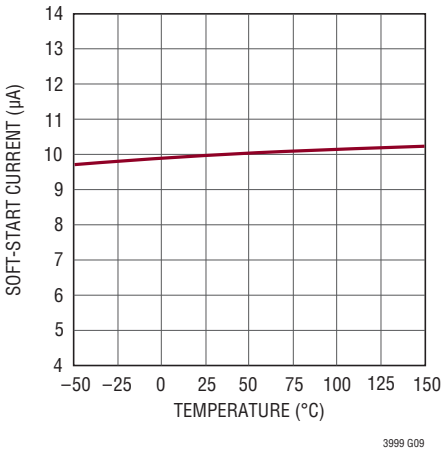


OVLO Threshold Voltage

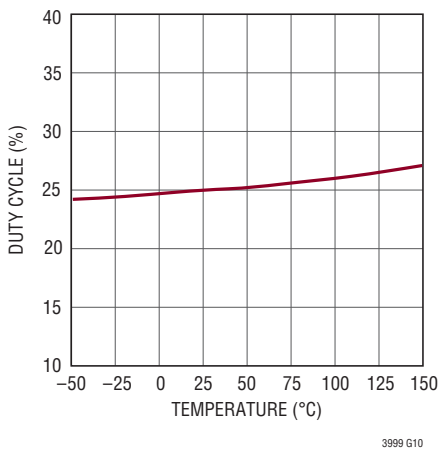


TYPICAL PERFORMANCE CHARACTERISTICS

Soft-Start (ILIM/SS) Current



Switch Duty Cycle



PIN FUNCTIONS

SWA, SWB (Pin 1, Pin 10): SWA and SWB pins are the open-collector nodes of the power switches. These pins drive the transformer and are connected to the outer terminals of the center tapped transformer. Large currents flow through these pins so keep PCB traces short and wide.

RBIAS (Pin 2): The RBIAS pin sets the bias current of the power switches (SWA and SWB). Connect the pin to a 49.9k resistor to GND.

V_{IN} (Pin 3): The V_{IN} pin is the main supply pin for the switch driver and internal regulator. Short duration, high current pulses are produced during the turn on and turn off of the power switches. Connect a low ESR capacitor of 4.7µF or greater.

UVLO (Pin 4): The UVLO pin has a precision threshold with hysteresis to implement an accurate V_{IN} undervoltage lockout. The UVLO function disables switching and sets the part into a low current shutdown mode. Connect the UVLO pin directly to V_{IN} or to a resistor divider string.

OVLO/DC (Pin 5): The OVLO/DC pin has a precision threshold with hysteresis to implement an accurate V_{IN} overvoltage lockout. The OVLO function disables the switching. Connect OVLO/DC pin to ground to disable the function or to a resistor divider string to program the duty cycle.

RDC (Pin 6): The RDC pin is the duty cycle control pin. A resistor to ground sets the duty cycle. If unused leave the pin floating or connect to the OVLO/DC pin.

RT (Pin 7): The RT pin sets the switching frequency of the power switches.

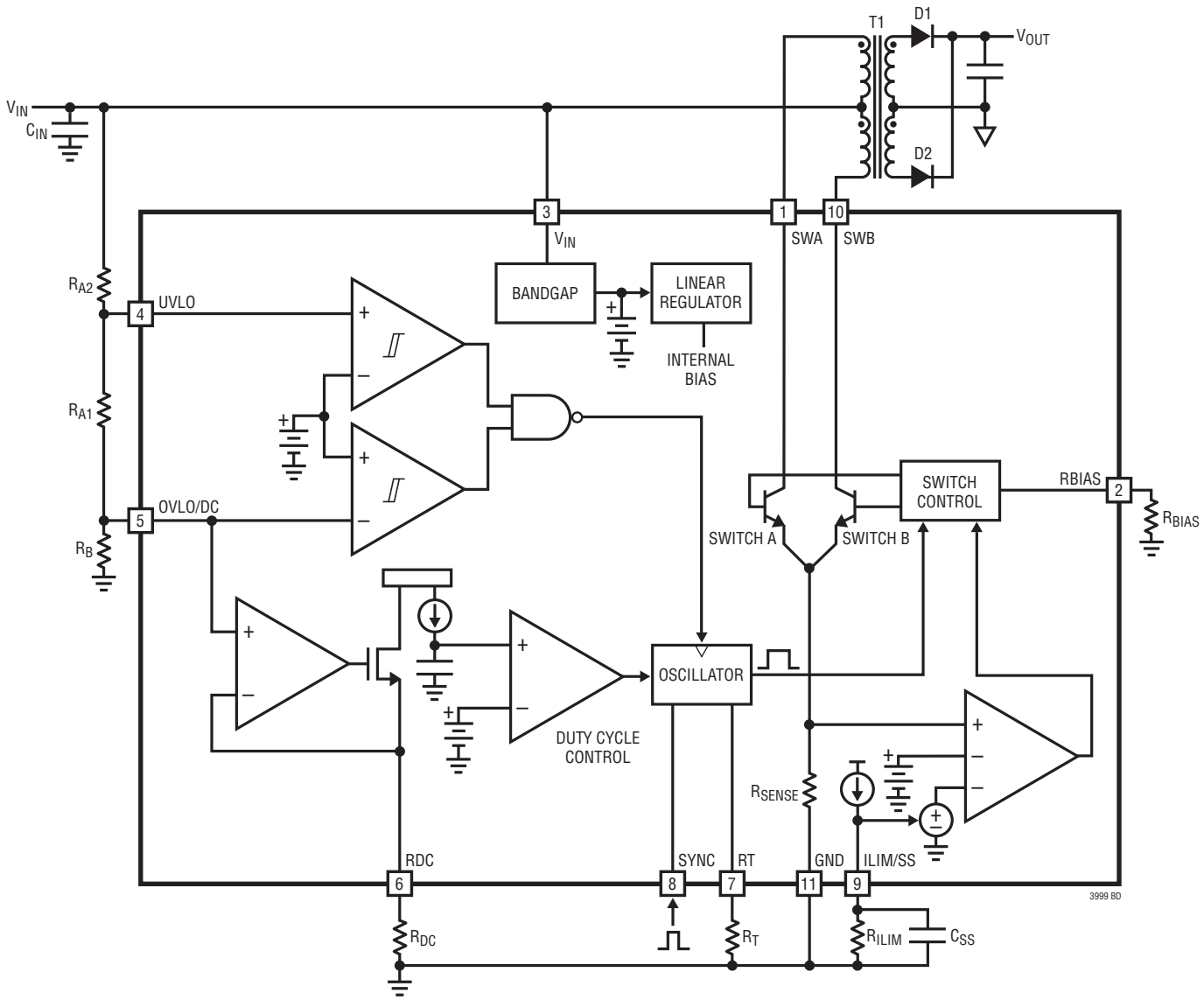
SYNC (Pin 8): The SYNC pin synchronizes the part to an external clock. Set the internal oscillator frequency below the external clock frequency. Synchronizing the clock to an external reference is useful for creating more stable positioning of the switcher voltage or current harmonics. Connect the SYNC pin to ground if not used.

ILIM/SS (Pin 9): The ILIM/SS pin sets a threshold level for the cycle by cycle maximum switch current. Implement soft-start with a capacitor, C_{SS}, placed on this pin to ground. An internal current source charges the capacitor. The R_{ILIM}, C_{SS} time constant sets the soft-start time and ramps the maximum switch current threshold at start-up.

If the ILIM/SS function is not used, float this pin and the current limit will default to the internal limit.

GND (Pin 11): The ground pin is the exposed pad of the package. Solder the exposed pad directly to the ground plane.

BLOCK DIAGRAM



OPERATION

Overview

The LT3999 is a monolithic isolated push-pull DC transformer driver. It includes functions such as duty cycle control, soft-start and protection features.

Push-Pull Topology

In a push-pull topology, a pair of switches operating out of phase generate a square wave voltage pulse on the primary side of a center tapped transformer. The diodes on the secondary side rectify the voltage and generate the output voltage. This voltage is simply V_{IN} times the transformer turns ratio.

Duty Cycle Control

The LT3999 duty cycle control provides, to a degree, line regulation. The duty cycle is programmed by a resistor on the RDC pin and the OVLO/DC voltage. By making the OVLO/DC voltage a function of V_{IN} the duty cycle will adjust with varying V_{IN} thereby keeping V_{OUT} constant.

This feature is useful in cases where an LDO is used to post regulate the output of the LT3999. By pseudo regulating the output with the duty cycle control the power dissipation in the LDO is minimized.

Leaving the RDC pin floating or connecting it to the OVLO/DC pin disables the duty cycle function and the LT3999 operates at close to 50% duty cycle.

Current Limit and Soft-Start

The LT3999 ILIM/SS pin programs the cycle-by-cycle switch current limit and the soft-start time. A resistor on the ILIM/SS pin sets the current limit. A capacitor on the pin in conjunction with the resistor sets the soft-start time.

When the programmed current limit is reached the switch is immediately turned off and remains off for the remainder of the cycle. Leaving the ILIM/SS pin unconnected will disable the programmable current limit and the LT3999 will default to its internal current limit.

The soft-start function ramps the maximum switch current over the programmed soft-start time. The purpose of the soft-start is to reduce inrush current from the input supply.

Other Features

The LT3999 protection features include overvoltage lockout (OVLO), undervoltage lockout (UVLO) and thermal shutdown.

The OVLO function is programmed with the OVLO/DC pin. Switching is disabled during an OVLO event. An internal overvoltage lockout on the V_{IN} pin is also provided to protect the LT3999.

The UVLO function is programmed with the UVLO pin. Switching is disabled during a UVLO event. The UVLO pin is also used to put the LT3999 into a low quiescent shutdown state.

At a junction temperature above the operating temperature range the thermal shutdown function turns off both switches.

APPLICATIONS INFORMATION

Switching Frequency

The LT3999 drives two output power switches out of phase, thus the oscillator frequency is two times the actual switching frequency of each power switch. The choice of switching frequency is a trade-off between power efficiency and the size of capacitive and inductive storage components.

Operating at low switching frequency reduces the switching losses (transient losses) and consequently improves the power converter efficiency. However, the lower switching frequency requires greater inductance for a given amount of ripple current, resulting in a larger design footprint and higher cost.

The LT3999 switching frequency is set in the range of 50kHz to 1MHz. The value of R_T for a given operating frequency is chosen from Table 1 or from the following equation:

Table 1. Recommended 1% Standard Values

R_T	f_{SW}
316kΩ	50kHz
158kΩ	100kHz
76.8kΩ	200kHz
49.9kΩ	300kHz
36.5kΩ	400kHz
28kΩ	500kHz
22.6kΩ	600kHz
19.1kΩ	700kHz
16.2kΩ	800kHz
14kΩ	900kHz
12.1kΩ	1000kHz

$$R_T\,(k\Omega) = \left(\frac{1}{2 \bullet f_{SW}} - 70ns\right) \bullet 3.25 \bullet 10^{10}$$

Oscillator Sync

In applications where a more precise frequency is desired to accurately place high frequency harmonics, the LT3999 oscillator can be synchronized to an external clock. Set the internal oscillator frequency 10% to 50% lower than the external sync frequency. The switching frequency is one-half the sync frequency.

Drive the SYNC pin with a 2V or greater square wave. The rising edge of the sync square wave will initiate clock discharge. If unused, connect the SYNC pin to ground.

Duty Cycle

To run the LT3999 at full duty cycle leave the RDC pin unconnected.

Variations in V_{IN} are, to a first order, compensated with the LT3999 duty cycle control function. The duty cycle function is implemented with a resistor divider on V_{IN} connected to the OVLO/DC pin and a resistor to ground on the RDC pin. Use the following formula to calculate the RDC resistor or duty cycle:

$$\text{Duty Cycle}\,(DC) = \frac{1.25 \bullet RDC}{V_{IN} \bullet \frac{R_B}{R_A + R_B} \bullet R_T \bullet 4}$$

$$RDC = \frac{V_{IN} \bullet \frac{R_B}{R_A + R_B} \bullet R_T \bullet DC \bullet 4}{1.25}$$

where R_A and R_B are the resistors from the V_{IN} to OVLO/DC resistor divider and R_T is the frequency setting resistor. See Figure 1. Setting the OVLO/DC pin to be 0.612V at the nominal V_{IN} voltage yields good line regulation over a wide input range.

The duty cycle refers to the duty cycle of the individual switch. Normally each switch operates at close to 50% duty cycle.

APPLICATIONS INFORMATION

Soft-Start and Current Limit

The LT3999 soft-start ramps the peak switch current over a time programmed by either a capacitor or a resistor and capacitor on the ILIM/SS pin.

When programming the soft-start time with a capacitor only the soft-start time is calculated with the following formula:

$$t_{SS}\ (ms) = C_{SS} \bullet 80$$

where C_{SS} is in µF.

The current limit defaults to the internally set value because there is no resistor on the pin.

When programming the soft-start time with a resistor and capacitor on the ILIM/SS pin the soft-start time is calculated with the following formula:

$$\tau = RC$$

where 3τ will be 95% of the maximum current.

The cycle-by-cycle current limit of the LT3999 is set with a resistor on the ILIM/SS pin. Use the following formula to calculate the value of the resistor:

$$R_{ILIM}\ (k\Omega) = I_{LIM} \bullet 86.4$$

OVLO/DC and UVLO

The UVLO pin has a precision voltage threshold with hysteresis to enable the LT3999. The pin is typically connected to V_{IN} through a resistor divider; however, it can be directly connected to V_{IN}.

The OVLO/DC pin has a precision voltage threshold with hysteresis to disable the LT3999 switching operation. The pin is typically connected to V_{IN} through a resistor divider. The OVLO/DC pin can be directly connected to GND to disable the function. It is possible to use two separate resistor divider strings for OVLO/DC and UVLO pins or combine them together and use one resistor divider string to drive both pins. See Figure 1.

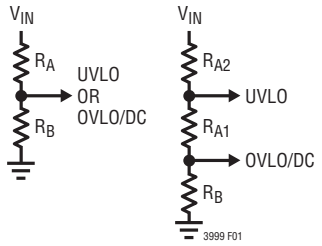


Figure 1. Precision UVLO and OVLO Resistor Divider

Resistors are chosen by first selecting R_B. Then calculate R_A with the following formula:

$$R_A = R_B\left(\frac{V_{TH}}{1.25V} - 1\right)$$

where V_{TH} is the V_{IN} referred voltage at which the supply is enabled (UVLO) or disabled (OVLO/DC).

Transformer Design

Table 3 lists recommended center tapped transformers for a variety of input voltage, output voltage and power combinations. These transformers will yield slightly high output voltages so that they can accommodate an LDO regulator on the output.

If your application is not listed, the LTC Applications group is available to assist in the choice and/or the design of the transformer. In the design/selection of the transformer the following characteristics are critical and should be considered:

Table 3. Recommended Center Tapped Transformers

NOMINAL INPUT VOLTAGE (V)	NOMINAL OUTPUT VOLTAGE (V)	OUTPUT POWER (W)	PART NUMBER
5	5	5	Coilcraft PA6383
5	12	1	Coilcraft PA6381
5	12	3	Cooper Bussmann CTX02-19064
12	12	10	Coilcraft PA6384
24	24	20	Cooper Bussmann CTX02-19061

APPLICATIONS INFORMATION

Turns Ratio

The turns ratio of the transformer determines the output voltage. The following equation is used as a first pass to calculate the turns ratio:

$$\frac{N_S}{N_P} = \frac{V_{OUT} + V_F}{2(V_{IN} - V_{SW})DC}$$

where V_F is the forward voltage of the output diode, V_{SW} is the voltage drop across the internal switches (see the Typical Performance curves) and DC is the duty cycle. Sufficient margin should be added to the turns ratio to account for voltage drops due to transformer winding resistance.

Magnetizing Current

The magnetizing inductance of the transformer causes a ripple current that is independent of load current. This ripple current is calculated by:

$$\Delta I = \frac{V_{IN} \bullet DC}{f_{SW} \bullet L_M}$$

where ΔI and L_M are primary ripple current and magnetizing inductance referred to the primary side of the transformer, respectively. Increasing the transformer magnetizing inductance, L_M, reduces the ripple current. The ripple current formula shows the effect of the switching frequency on the magnetizing inductance. Setting the LT3999 at high switching frequency reduces the ripple current for the same magnetizing inductance. Therefore, it is possible to reduce the transformer turns and still achieve low ripple current. This helps to reduce the power converter footprint as well. The transformer magnetizing inductance should be designed for the worst-case duty cycle and input line voltage combination.

A good rule of thumb is to set the primary current ripple amplitude 10% to 30% of the average primary current, I_P:

$$I_P = \frac{P_{OUT}}{V_{IN} \bullet eff}$$

where P_{OUT} is the output power of the converter and eff is the converter efficiency, typically around 85%.

Winding Resistance

Resistance in either the primary or secondary winding reduces overall efficiency and degrades load regulation. If efficiency or load regulation is unsatisfactory, verify that the voltage drops in the transformer windings are not excessive.

Capacitors

In applications with full duty cycle operation, the input supply current is approximately constant. Therefore, large input “hold-up type” capacitors are not necessary. A low value (>4.7µF), low ESR ceramic will be adequate to filter high frequency noise at the input. The output capacitors supply energy to the output load only during switch transitions. Therefore, large capacitance values are not necessary on the output.

Transformer winding capacitance between the isolated primary and secondary has parasitic currents that can cause noise on the grounds. Providing a high frequency, low impedance path between the primary and secondary gives the parasitic currents a local return path. A 2.2nF, 1kV ceramic capacitor is recommended.

Optional LC Filter

An optional LC filter, as shown on the Typical Application on the first page of this data sheet, should be included if ultralow noise and ripple are required. It is recommended that the corner frequency of the filter should be set a decade below the switching frequency so that the switch noise is attenuated by a factor of 100. For example, if the f_{OSC} = 100kHz, then f_{CORNER} = 10kHz where:

$$f_{CORNER} = \frac{1}{2 \bullet \pi \sqrt{LC}}$$

Switching Diode Selection

A fast recovery, surface mount diode such as a Schottky is recommended. The proximity of the diodes to the transformer outputs is important and should be as close as possible with short, wide traces connecting them.

APPLICATIONS INFORMATION

Output Voltage Regulation

The output voltage of the DC transformer topology is unregulated. Variations in the input voltage will cause the output voltage to vary because the output voltage is a function of the input voltage and the transformer turn ratio. Also, variations in the output load will cause the output voltage to change because of circuit parasitics, such as the transformer DC resistance and power switch on resistance. If regulation is necessary, a post regulator such as a linear regulator can be added to the output of the supply. See the Typical Applications for examples of adding a linear regulator.

Power Consideration

The current derived from the V_{IN} pin and the SWA and SWB switching currents are the sources of the LT3999 power dissipation. The power dissipation is the sum of:

1) The quiescent current and switch drive power dissipation:

$$P_{VIN} = V_{IN}\left(\frac{I_{SW} \bullet DC}{30} + 4mA\right)$$

where I_{SW} is the average switch current.

2) The conducting power dissipation of the switches during on state:

$P_{VCESAT} = V_{CESAT} \bullet I_{SW} \bullet 2DC$

where DC is the duty cycle and V_{CESAT} is the collector to emitter voltage drop during the switch saturation.

3) The dynamic power dissipation due to the switching transitions:

$P_{SW} = V_{IN} \bullet I_{SW} \bullet f_{OSC} \bullet (t_r + t_f)$

where t_r and t_f are the rise and fall times.

The junction temperature is computed as:

$T_J = T_{AMB} + P_D \bullet \theta_{JA}$

where:

$P_D = P_{VIN} + P_{VCESAT} + P_{SW}$ and θ_{JA} is the package thermal resistance.

Layout Consideration Check List

The following is a list of recommended layout considerations:

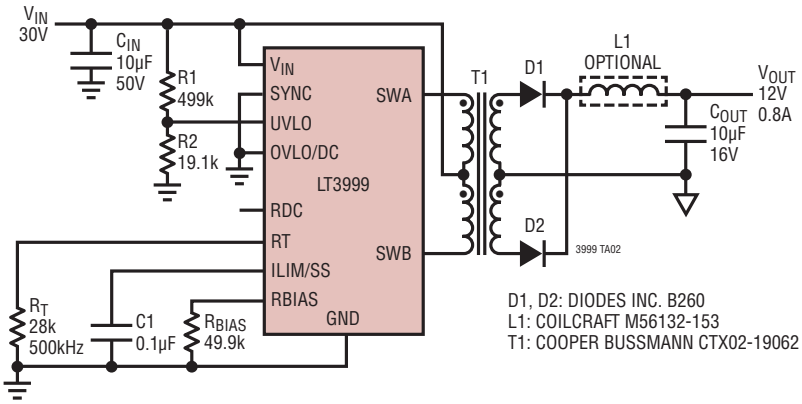
- Locate the bypass capacitor on the V_{IN} pin of the transformer close to the transformer.
- Create a solid GND plane, preferably on layer two of the PCB.
- Use short wide traces to connect to the transformer.
- The transformer and PCB routing should be carefully designed to maximize the symmetry between two switching half cycles.
- Solder the LT3999 exposed pad to the PCB. Add multiple vias to connect the exposed pad to the GND plane.

More Help

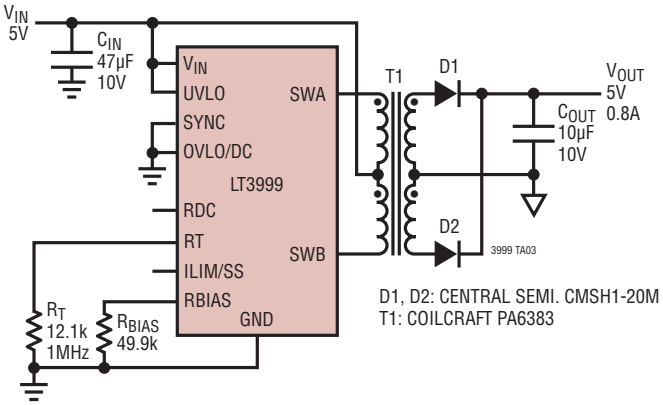
AN70: “A Monolithic Switching Regulator with 100mV Output Noise” contains much information concerning applications and noise measurement techniques.

TYPICAL APPLICATIONS

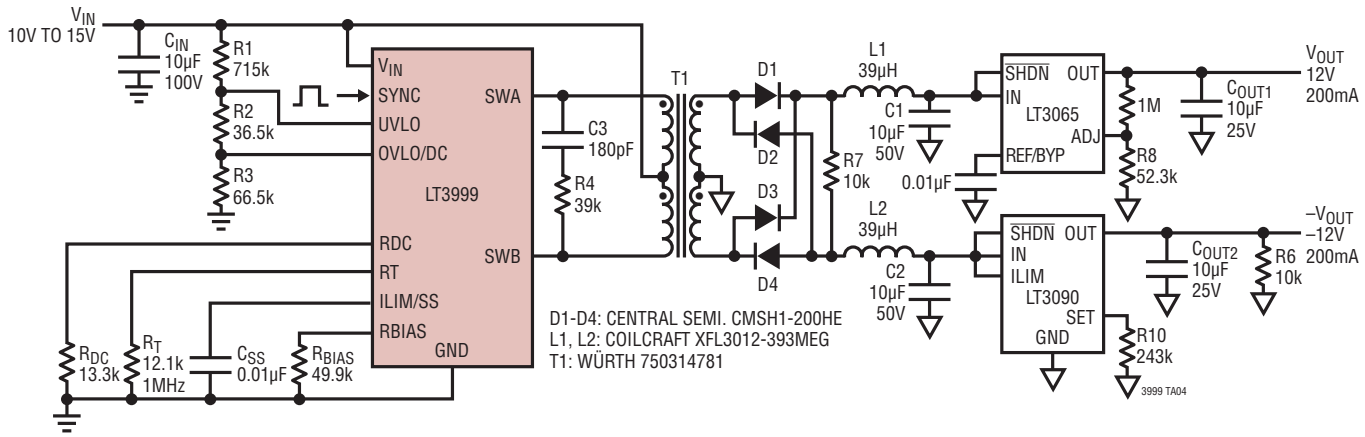
30V to 12V, 10W Push-Pull DC Transformer



5V to 5V, 4W Low Part Count Push-Pull DC Transformer



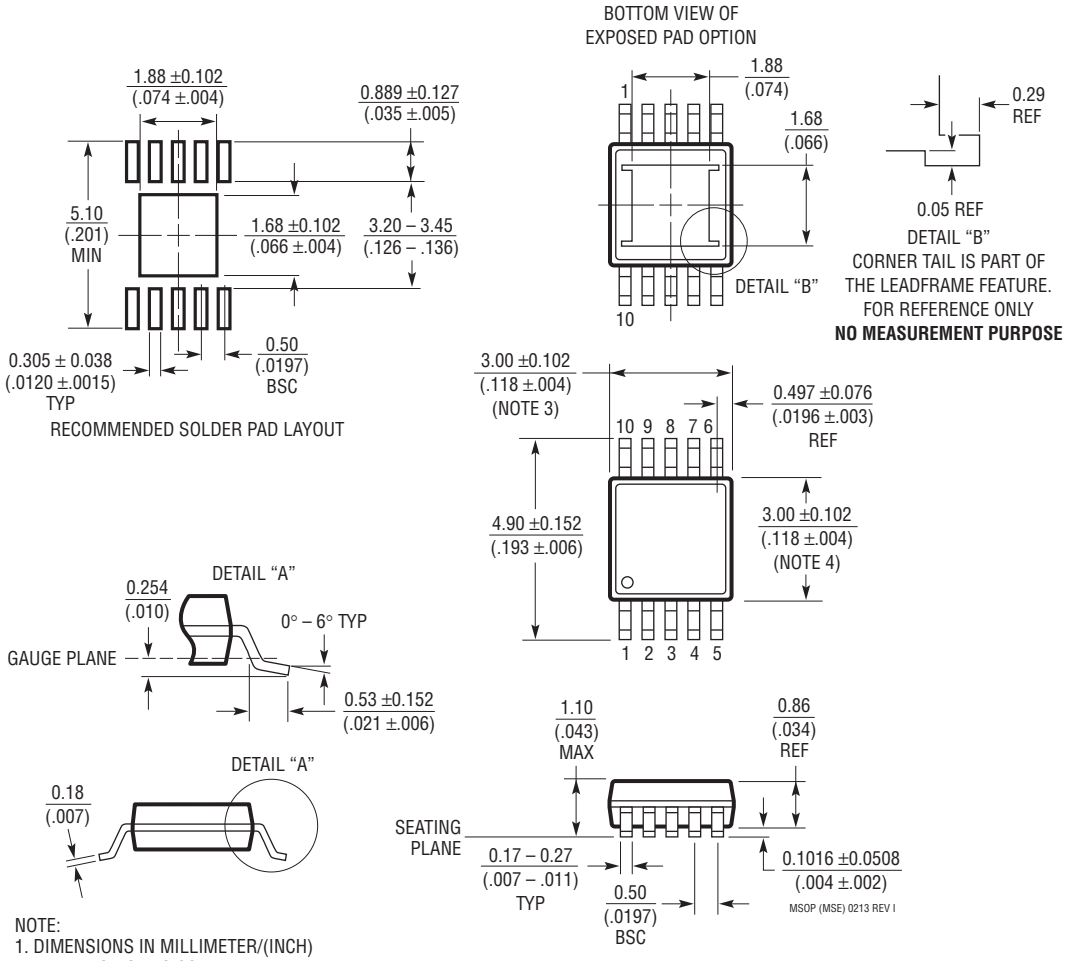
10V-15V to ±12V, 200mA Isolated Switching Regulator



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev I)

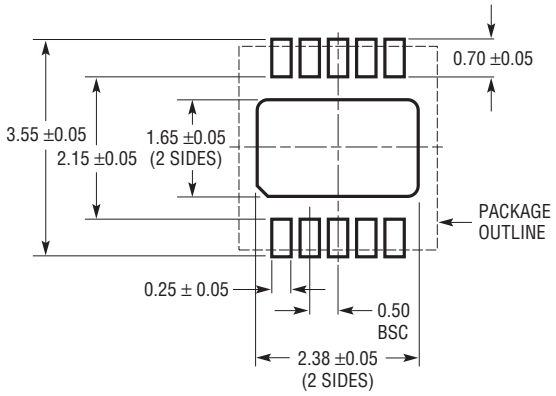


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

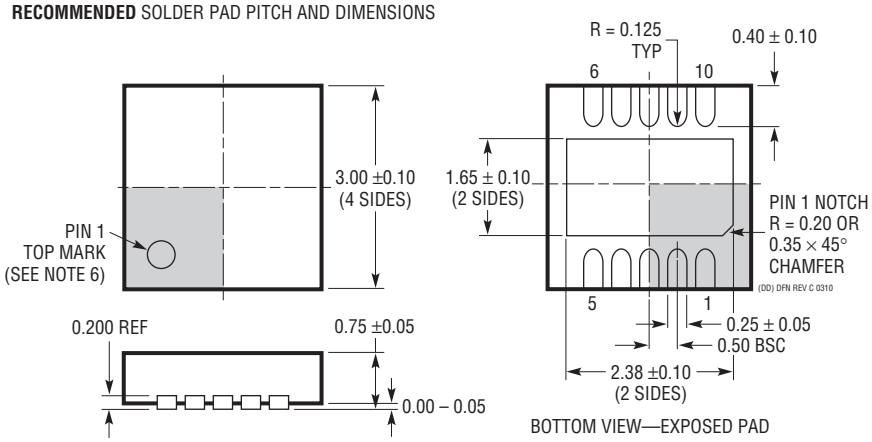
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



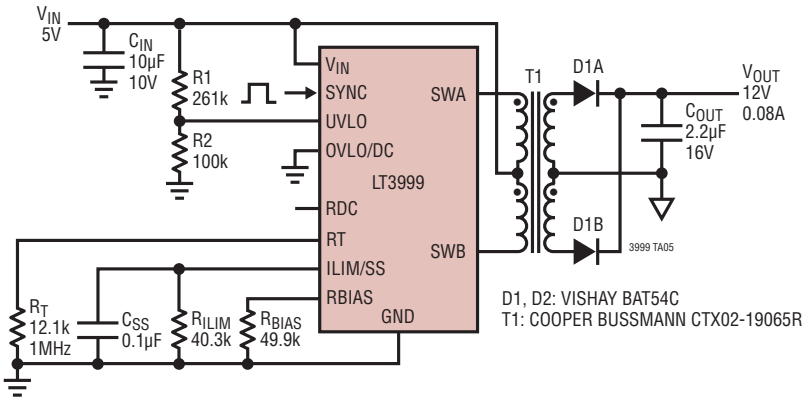
NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/15	Corrected pin assignments	5
		Revised schematics	13, 16

TYPICAL APPLICATION

5V to 12V, 1W Low Power Push-Pull DC Transformer



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3439	Slew Rate Controlled Ultralow Noise 1A Isolated DC/DC Transformer Driver	V_{IN}: 2.7V to 17.5V, I_Q (Supply) = 12mA, I_{SD} < 12mA, SO-16, Low Noise: <100mV_{P-P}, Independent Control of Switch Voltage and Current Slew Rates
LT1533	Slew Rate Controlled Ultralow Noise 1A Switching Regulator	V_{IN}: 2.7V to 23V, I_Q (Supply) = 12mA, I_{SD} < 12mA, SO-16, Low Noise: <100mV_{P-P}, Independent Control of Switch Voltage and Current Slew Rates
LT1683	Slew Rate Controlled Ultralow Noise Push-Pull Controller	V_{IN}: 2.7V to 20V, I_Q (Supply) = 25mA, I_{SD} < 24mA, SSOP-20, Low Noise: <200mV_{P-P}, Independent Control of Switch Voltage and Current Slew Rates
LT1738	Slew Rate Controlled Ultralow Noise DC/DC Controller	V_{IN}: 2.7V to 20V, I_Q (Supply) = 12mA, I_{SD} < 24mA, SSOP-20, Greatly Reduced Conducted and Radiated EMI, Independent Control of Switch Voltage and Current Slew Rates

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LT3999
LT 0415 REV A • PRINTED IN USA