ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltages

Input Supply Pin (V_{IN}) ..... –0.3V to 65V
Boosted Supply Pin (BOOST) ..... –0.3V to 80V
Boosted Supply Voltage (BOOST – SW) ... –0.3V to 24V
Boosted Supply Reference Pin (SW) ..... –2V to 65V
Local Supply Pin (V_{CC}) ..... –0.3V to 24V

Input Voltages

$SENSE^+$, $SENSE^-$ ..... –0.3V to 40V
$SENSE^+ – SENSE^-$ ..... –1V to 1V
BURST_EN Pin ..... –0.3V to 24V
Other Inputs ($\overline{SHDN}$, C_{SS}, V_{FB}, V_C) ..... –0.3V to 5.0V

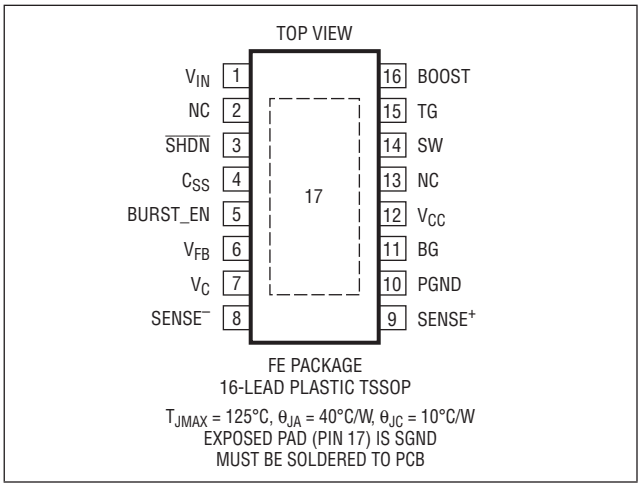
Input Currents

$\overline{SHDN}$, C_{SS} ..... –1mA to 1mA

Maximum Temperatures

Operating Junction Temperature Range (Note 2)
LT3800E (Note 3) ..... –40°C to 125°C
LT3800I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3800EFE#PBF	LT3800EFE#TRPBF	3800EFE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3800IFE#PBF	LT3800IFE#TRPBF	3800IFE	16-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 20V, V_{CC} = BOOST = BURST_EN = 10V, $\overline{SHDN}$ = 2V, $SENSE^-$ = $SENSE^+$ = 10V, SGND = PGND = SW = 0V, CTG = CBG = 3300pF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range (Note 4)		●	4		60	V
	Minimum Start Voltage		●	7.5			V
	UVLO Threshold (Falling)		●	3.65	3.80	3.95	V
	UVLO Hysteresis				670		mV
I_{VIN}	V_{IN} Supply Current	V_{CC} > 9V	●		20		µA
	V_{IN} Burst Mode Current	V_{BURST_EN} = 0V, V_{FB} = 1.35V			20		µA
	V_{IN} Shutdown Current	$V_{\overline{SHDN}}$ = 0V			8	15	µA
V_{BOOST}	Operating Voltage		●			75	V
	Operating Voltage Range (Note 5)	$V_{BOOST} – V_{SW}$	●			20	V
	UVLO Threshold (Rising)	$V_{BOOST} – V_{SW}$			5		V
	UVLO Hysteresis	$V_{BOOST} – V_{SW}$			0.4		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 20V, V_{CC} = BOOST = BURST_EN = 10V, $\overline{SHDN}$ = 2V, $SENSE^-$ = $SENSE^+$ = 10V, SGND = PGND = SW = 0V, CTG = CBG = 3300pF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{BOOST}	BOOST Supply Current (Note 6) BOOST Burst Mode Current BOOST Shutdown Current	 V_{BURST_EN} = 0V $V_{\overline{SHDN}}$ = 0V	 		1.4 0.1 0.1		mA µA µA
V_{CC}	Operating Voltage (Note 5) Output Voltage UVLO Threshold (Rising) UVLO Hysteresis	 	● ● 		 8.0 6.25 500	20 8.3 	V V V mV
I_{VCC}	V_{CC} Supply Current (Note 6) V_{CC} Burst Mode Current V_{CC} Shutdown Current Short-Circuit Current	 V_{BURST_EN} = 0V $V_{\overline{SHDN}}$ = 0V 	● ●	 –40	3 80 20 –120	3.6 	mA µA µA mA
$V_{\overline{SHDN}}$	Enable Threshold (Rising) Threshold Hysteresis	 	● 	1.30	1.35 120	1.40 	V mV
V_{SENSE}	Common Mode Range Current Limit Sense Voltage Reverse Protect Sense Voltage Reverse Current Offset	 $V_{SENSE^+} - V_{SENSE^-}$ $V_{SENSE^+} - V_{SENSE^-}$, $V_{BURST\_EN} = V_{CC}$ V_{BURST_EN} = 0V or $V_{BURST\_EN} = V_{FB}$	● ● 	0 140 	 150 –150 10	36 175 	 mV mV mV
I_{SENSE}	Input Current ($I_{SENSE^+} + I_{SENSE^-}$)	$V_{SENSE(CM)}$ = 0V $V_{SENSE(CM)}$ = 2.75V $V_{SENSE(CM)}$ > 4V	 		0.8 –20 –0.3		mA µA mA
f_O	Operating Frequency	 	 ●	190 175	200 	210 220	kHz kHz
V_{FB}	Error Amp Reference Voltage	Measured at V_{FB} Pin	 ●	1.224 1.215	1.231 	1.238 1.245	V V
I_{FB}	Feedback Input Current				25		nA
$V_{FB(SS)}$	Soft-Start Disable Voltage Soft-Start Disable Hysteresis	V_{FB} Rising			1.185 300		V mV
I_{CSS}	Soft-Start Capacitor Control Current				2		µA
g_m	Error Amp Transconductance		●	275	350	400	µmhos
A_V	Error Amp DC Voltage Gain				62		dB
V_C	Error Amp Output Range	Zero Current to Current Limit			1.2		V
I_{VC}	Error Amp Sink/Source Current				±30		µA
$V_{TG,BG}$	Gate Drive Output On Voltage (Note 7) Gate Drive Output Off Voltage				9.8 0.1		V V
$t_{TG,BG}$	Gate Drive Rise/Fall Time	10% to 90% or 90% to 10%			50		ns
$t_{TG(OFF)}$	Minimum Off Time				450		ns
$t_{TG(ON)}$	Minimum On Time		●		300	500	ns
t_{NOL}	Gate Drive Nonoverlap Time	TG Fall to BG Rise BG Fall to TG Rise			200 150		ns ns

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: The LT3800E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3800I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 4: V_{IN} voltages below the start-up threshold (7.5V) are only supported when V_{CC} is externally driven above 6.5V.

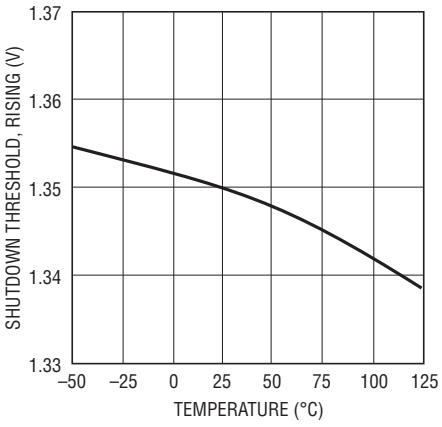
Note 5: Operating range dictated by MOSFET absolute maximum gate-source voltage ratings.

Note 6: Supply current specification does not include switch drive currents. Actual supply currents will be higher.

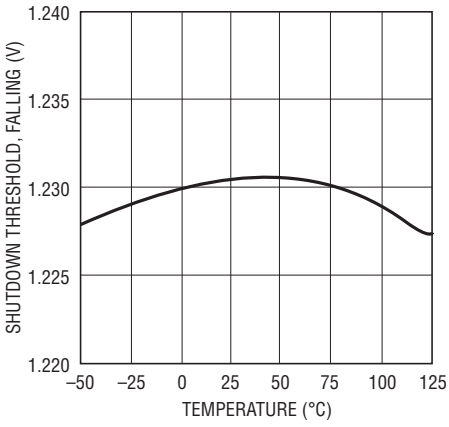
Note 7: DC measurement of gate drive output "ON" voltage is typically 8.6V. Internal dynamic bootstrap operation yields typical gate "ON" voltages of 9.8V during standard switching operation. Standard operation gate "ON" voltage is not tested but guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

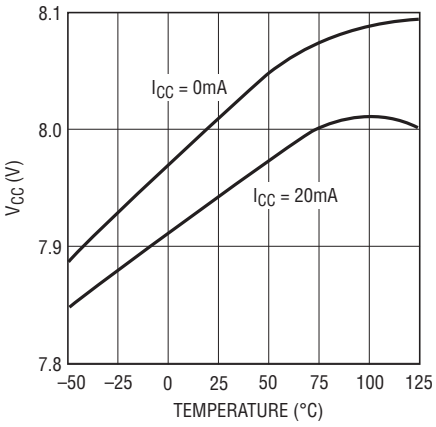
Shutdown Threshold (Rising) vs Temperature



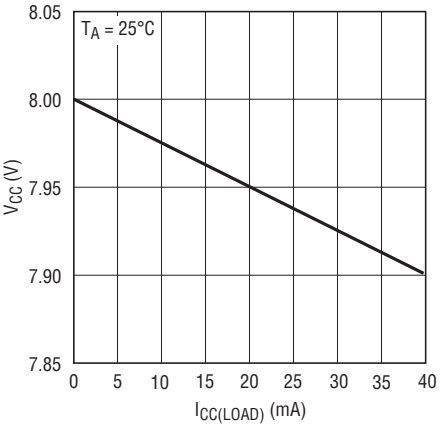
Shutdown Threshold (Falling) vs Temperature



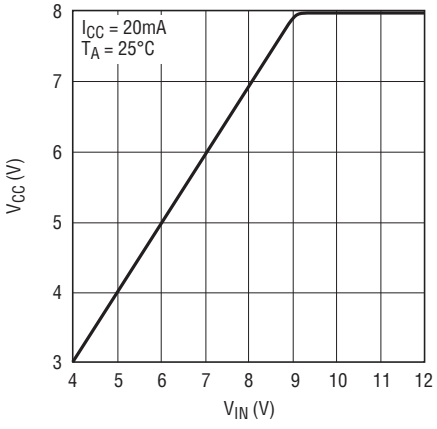
V_{CC} vs Temperature



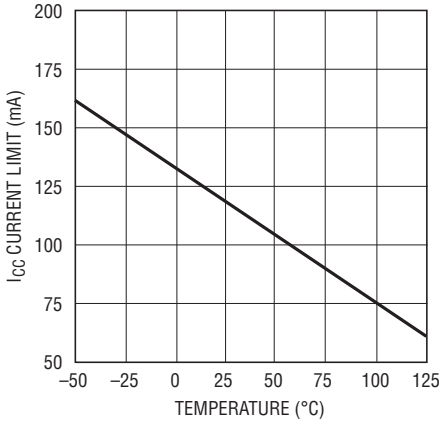
V_{CC} vs $I_{CC(LOAD)}$



V_{CC} vs V_{IN}

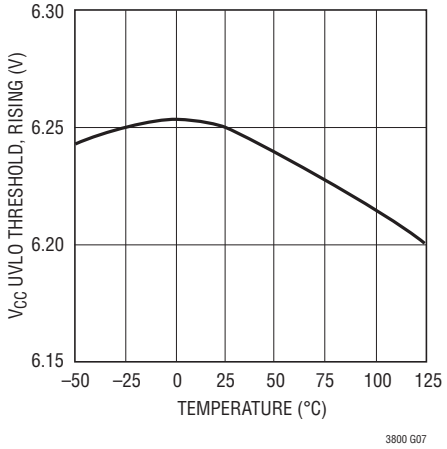


I_{CC} Current Limit vs Temperature

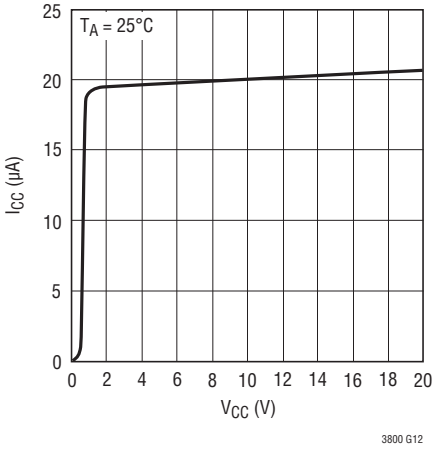


TYPICAL PERFORMANCE CHARACTERISTICS

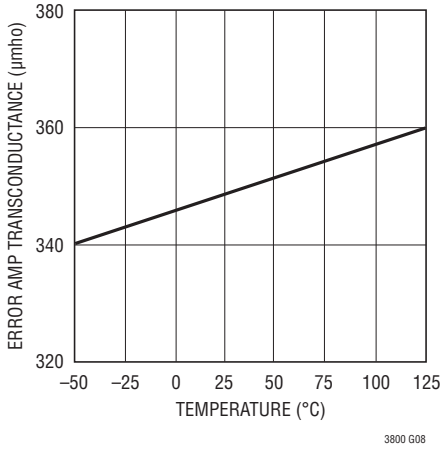
V_{CC} UVLO Threshold (Rising) vs Temperature



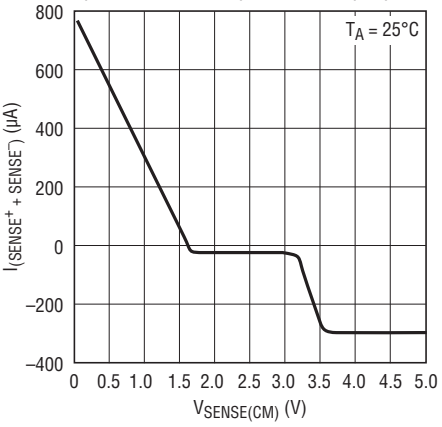
I_{CC} vs V_{CC} ($\overline{SHDN}$ = 0V)



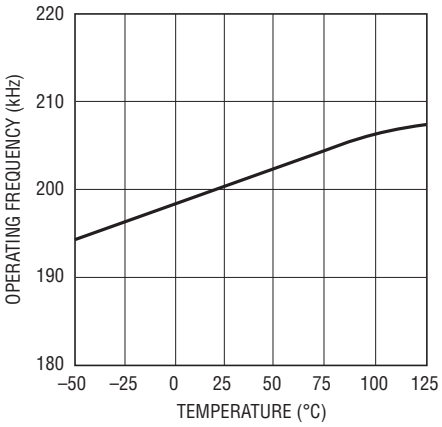
Error Amp Transconductance vs Temperature



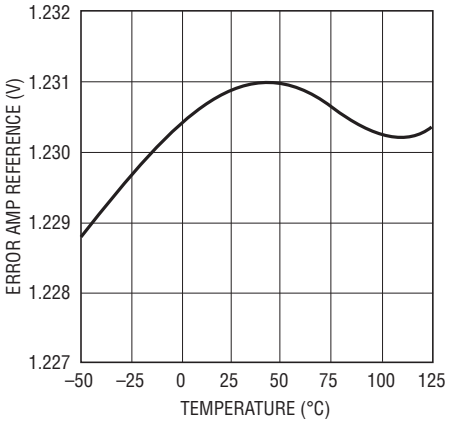
$I_{(SENSE^+ + SENSE^-)}$ vs $V_{SENSE(CM)}$



Operating Frequency vs Temperature



Error Amp Reference vs Temperature



PIN FUNCTIONS

V_{IN} (Pin 1): Converter Input Supply.

NC (Pin 2): No Connection.

$\overline{SHDN}$ (Pin 3): Precision Shutdown Pin. Enable threshold is 1.35V (rising) with 120mV of input hysteresis. When in shutdown mode, all internal IC functions are disabled. The precision threshold allows use of the $\overline{SHDN}$ pin to incorporate UVLO functions. If the $\overline{SHDN}$ pin is pulled below 0.7V, the IC enters a low current shutdown mode with I_{VIN} < 10µA. In low-current shutdown, the IC will sink 20µA from the V_{CC} pin until that local supply has collapsed. Typical pin input bias current is <10nA and the pin is internally clamped to 6V.

C_{SS} (Pin 4): Soft-Start AC Coupling Capacitor Input. Connect capacitor (C_{SS}) in series with a 200k resistor from pin to converter output (V_{OUT}). Controls converter start-up output voltage slew rate ($\Delta V_{OUT}/\Delta t$). Slew rate corresponds to 2µA average current through the soft-start coupling capacitor. The capacitor value for a desired output startup slew rate follows the relation:

$$C_{SS} = 2\mu A/(\Delta V_{OUT}/\Delta t)$$

Shorting this pin to SGND disables the soft-start function

BURST_EN (Pin 5): Burst Mode Operation Enable Pin. This pin also controls reverse-inhibit mode of operation. When the pin voltage is below 0.5V, Burst Mode operation

PIN FUNCTIONS

and reverse-current inhibit functions are enabled. When the pin voltage is above 0.5V, Burst Mode operation is disabled, but reverse-current inhibit operation is maintained. DC/DC converters operating with reverse-current inhibit operation (BURST_EN = V_{FB}) have a 1mA minimum load requirement. Reverse-current inhibit is disabled when the pin voltage is above 2.5V. This pin is typically shorted to ground to enable Burst Mode operation and reverse-current inhibit, shorted to V_{FB} to disable Burst Mode operation while enabling reverse-current inhibit, and connected to V_{CC} pin to disable both functions. See Applications Information section.

V_{FB} (Pin 6): Error Amplifier Inverting Input. The noninverting input of the error amplifier is connected to an internal 1.231V reference. Desired converter output voltage (V_{OUT}) is programmed by connecting a resistive divider from the converter output to the V_{FB} pin. Values for the resistor connected from V_{OUT} to V_{FB} (R2) and the resistor connected from V_{FB} to ground (R1) can be calculated via the following relationship:

$$R2 = R1 \bullet \left(\frac{V_{OUT}}{1.231} - 1 \right)$$

The V_{FB} pin input bias current is 25nA, so use of extremely high value feedback resistors could cause a converter output that is slightly higher than expected. Bias current error at the output can be estimated as:

$$\Delta V_{OUT(BIAS)} = 25nA \bullet R2$$

V_C (Pin 7): Error Amplifier Output. The voltage on the V_C pin corresponds to the maximum (peak) switch current per oscillator cycle. The error amplifier is typically configured as an integrator by connecting an RC network from this pin to ground. This network creates the dominant pole for the converter voltage regulation feedback loop. Specific integrator characteristics can be configured to optimize transient response. Connecting a 100pF or greater high frequency bypass capacitor from this pin to ground is also recommended. When Burst Mode operation is enabled (see Pin 5 description), an internal low impedance clamp on the V_C pin is set at 100mV below the burst threshold, which limits the negative excursion of the pin voltage. Therefore, this pin cannot be pulled low with a low-impedance source. If the V_C pin must be externally manipulated, do so through a 1kΩ series resistance.

SENSE⁻ (Pin 8): Negative Input for Current Sense Amplifier. Sensed inductor current limit set at ±150mV across SENSE inputs.

SENSE⁺ (Pin 9): Positive Input for Current Sense Amplifier. Sensed inductor current limit set at ±150mV across SENSE inputs.

PGND (Pin 10): High Current Ground Reference for Synchronous Switch. Current path from pin to negative terminal of V_{CC} decoupling capacitor must not corrupt SGND.

BG (Pin 11): Synchronous Switch Gate Drive Output.

V_{CC} (Pin 12): Internal Regulator Output. Most IC functions are powered from this pin. Driving this pin from an external source reduces V_{IN} pin current to 20µA. This pin is decoupled with a low ESR 1µF capacitor to PGND. In shutdown mode, this pin sinks 20µA until the pin voltage is discharged to 0V. See Typical Performance Characteristics.

NC (Pin 13): No Connection.

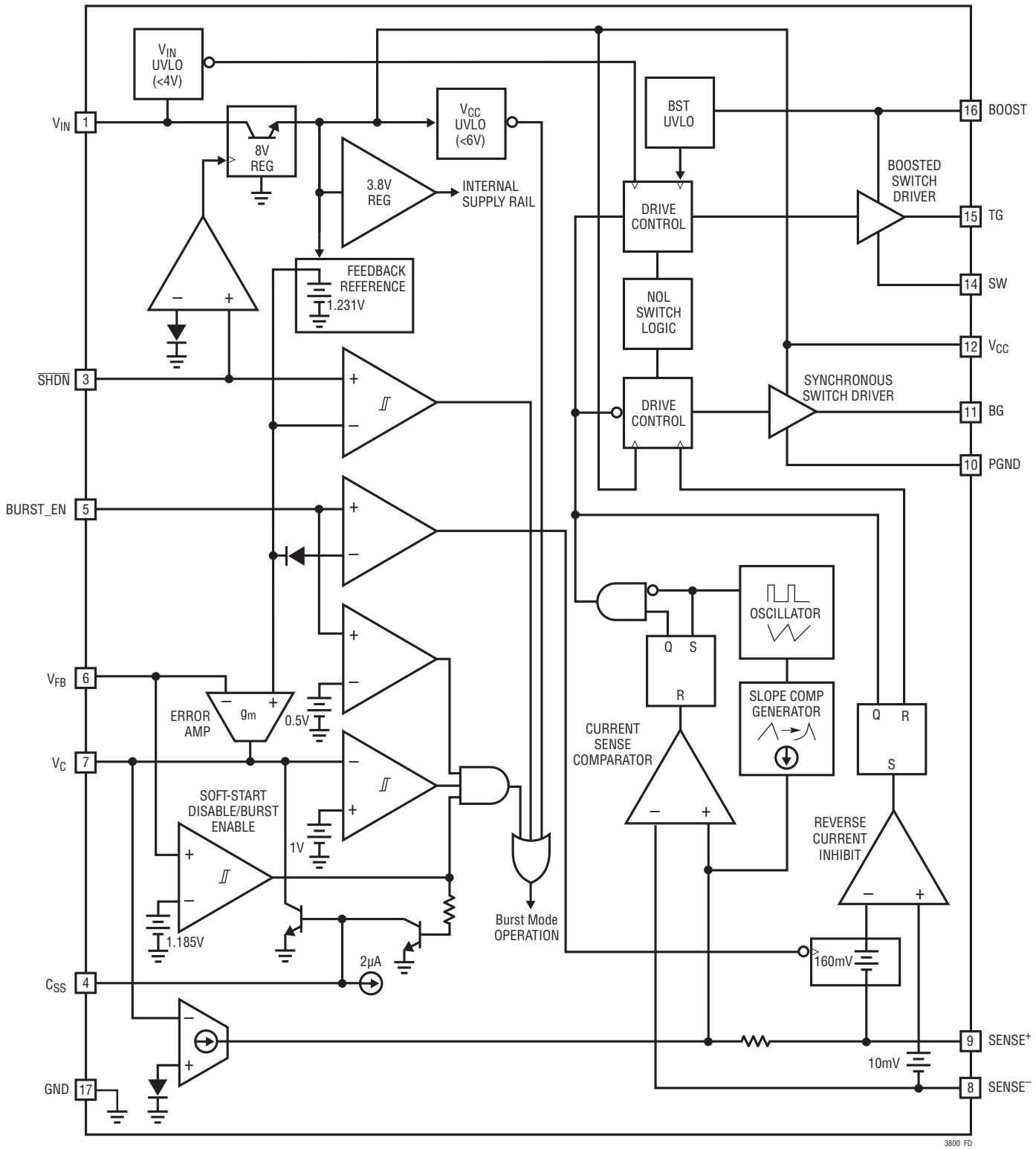
SW (Pin 14): Reference for V_{BOOST} Supply and High Current Return for Bootstrapped Switch.

TG (Pin 15): Bootstrapped Switch Gate Drive Output.

BOOST (Pin 16): Bootstrapped Supply – Maximum Operating Voltage (Ground Referred) to 75V. This pin is decoupled with a low ESR 1µF capacitor to pin SW. The voltage on the decoupling capacitor is refreshed through a rectifier from either V_{CC} or an external source.

Exposed Package Backside (SGND) (Pin 17): Low Noise Ground Reference. SGND connection is made through the exposed lead frame on back of TSSOP package which must be soldered to the PCB ground.

FUNCTIONAL DIAGRAM



APPLICATIONS INFORMATION

Overview

The LT3800 is a high input voltage range step-down synchronous DC/DC converter controller IC that uses a 200kHz constant frequency, current mode architecture with external N-channel MOSFET switches.

The LT3800 has provisions for high efficiency, low load operation for battery-powered applications. Burst Mode operation reduces total average input quiescent currents to 100µA during no load conditions. A low current shutdown mode can also be activated, reducing quiescent current to <10µA. Burst Mode operation can be disabled if desired.

The LT3800 also employs a reverse-current inhibit feature, allowing increased efficiencies during light loads through nonsynchronous operation. This feature disables the synchronous switch if inductor current approaches zero. If full time synchronous operation is desired, this feature can be disabled.

Much of the LT3800's internal circuitry is biased from an internal linear regulator. The output of this regulator is the V_{CC} pin, allowing bypassing of the internal regulator. The associated internal circuitry can be powered from the output of the converter, increasing overall converter efficiency. Using externally derived power also eliminates the IC's power dissipation associated with the internal V_{IN} to V_{CC} regulator.

Theory of Operation (See Block Diagram)

The LT3800 senses converter output voltage via the V_{FB} pin. The difference between the voltage on this pin and an internal 1.231V reference is amplified to generate an error voltage on the V_C pin which is, in turn, used as a threshold for the current sense comparator.

During normal operation, the LT3800 internal oscillator runs at 200kHz. At the beginning of each oscillator cycle, the switch drive is enabled. The switch drive stays enabled until the sensed switch current exceeds the V_C derived threshold for the current sense comparator and, in turn, disables the switch driver. If the current comparator threshold is not obtained for the entire oscillator cycle, the switch driver is disabled at the end of the cycle for 450ns. This minimum off-time mode of operation assures regeneration of the BOOST bootstrapped supply.

Power Requirements

The LT3800 is biased using a local linear regulator to generate internal operational voltages from the V_{IN} pin. Virtually all of the circuitry in the LT3800 is biased via an internal linear regulator output (V_{CC}). This pin is decoupled with a low ESR 1µF capacitor to PGND.

The V_{CC} regulator generates an 8V output provided there is ample voltage on the V_{IN} pin. The V_{CC} regulator has approximately 1V of dropout, and will follow the V_{IN} pin with voltages below the dropout threshold.

The LT3800 has a start-up requirement of $V_{IN} > 7.5V$. This assures that the onboard regulator has ample headroom to bring the V_{CC} pin above its UVLO threshold. The V_{CC} regulator can only source current, so forcing the V_{CC} pin above its 8V regulated voltage allows use of externally derived power for the IC, minimizing power dissipation in the IC. Using the onboard regulator for start-up, then deriving power for V_{CC} from the converter output maximizes conversion efficiencies and is common practice. If V_{CC} is maintained above 6.5V using an external source, the LT3800 can continue to operate with V_{IN} as low as 4V.

The LT3800 operates with 3mA quiescent current from the V_{CC} supply. This current is a fraction of the actual V_{CC} quiescent currents during normal operation. Additional current is produced from the MOSFET switching currents for both the boosted and synchronous switches and are typically derived from the V_{CC} supply.

Because the LT3800 uses a linear regulator to generate V_{CC}, power dissipation can become a concern with high V_{IN} voltages. Gate drive currents are typically in the range of 5mA to 15mA per MOSFET, so gate drive currents can create substantial power dissipation. It is advisable to derive V_{CC} and V_{BOOST} power from an external source whenever possible.

APPLICATIONS INFORMATION

The onboard V_{CC} regulator will provide gate drive power for start-up under all conditions with total MOSFET gate charge loads up to 180nC. The regulator can operate the LT3800 continuously, provided the V_{IN} voltage and/or MOSFET gate charge currents do not create excessive power dissipation in the IC. Safe operating conditions for continuous regulator use are shown in Figure 1. In applications where these conditions are exceeded, V_{CC} must be derived from an external source after start-up.

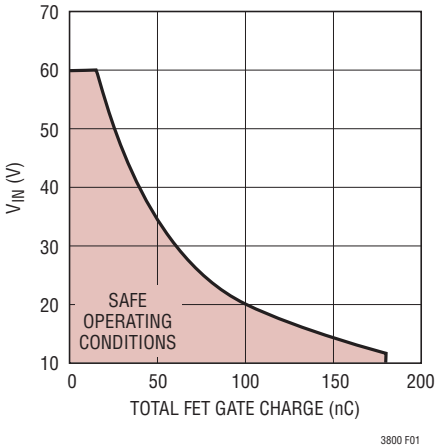
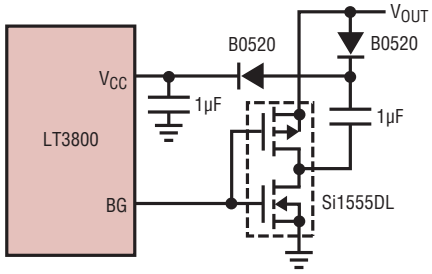


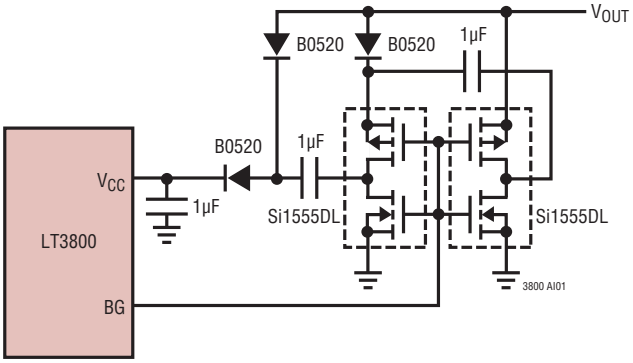
Figure 1. V_{CC} Regulator Continuous Operating Conditions

In LT3800 converter applications with output voltages in the 9V to 20V range, back-feeding V_{CC} and V_{BOOST} from the converter output is trivial, accomplished by connecting diodes from the output to these supply pins. Deriving these supplies from output voltages greater than 20V will require additional regulation to reduce the feedback voltage. Outputs lower than 9V will require step-up techniques to increase the feedback voltage to something greater than the 8V V_{CC} regulated output. Low power boost switchers are sometimes used to provide the step-up function, but a simple charge-pump can perform this function in many instances.

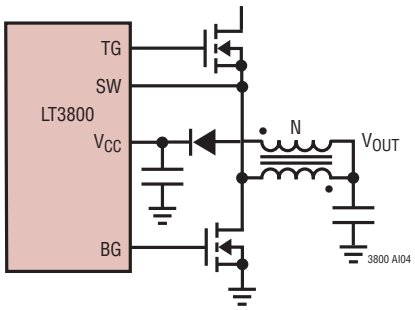
Charge Pump Doubler



Charge Pump Tripler



Inductor Auxiliary Winding



APPLICATIONS INFORMATION

Burst Mode

The LT3800 employs low current Burst Mode functionality to maximize efficiency during no load and low load conditions. Burst Mode operation is enabled by shorting the BURST_EN pin to SGND. Burst Mode operation can be disabled by shorting BURST_EN to either V_{FB} or V_{CC}.

When the required switch current, sensed via the V_C pin voltage, is below 15% of maximum, the Burst Mode operation is employed and that level of sense current is latched onto the IC control path. If the output load requires less than this latched current level, the converter will overdrive the output slightly during each switch cycle. This overdrive condition is sensed internally and forces the voltage on the V_C pin to continue to drop. When the voltage on V_C drops 150mV below the 15% load level, switching is disabled and the LT3800 shuts down most of its internal circuitry, reducing total quiescent current to 100µA. When the converter output begins to fall, the V_C pin voltage begins to climb. When the voltage on the V_C pin climbs back to the 15% load level, the IC returns to normal operation and switching resumes. An internal clamp on the V_C pin is set at 100mV below the switch disable threshold, which limits the negative excursion of the pin voltage, minimizing the converter output ripple during Burst Mode operation.

During Burst Mode operation, V_{IN} pin current is 20µA and V_{CC} current is reduced to 80µA. If no external drive is provided for V_{CC}, all V_{CC} bias currents originate from the V_{IN} pin, giving a total V_{IN} current of 100µA. Burst current can be reduced further when V_{CC} is driven using an output derived source, as the V_{CC} component of V_{IN} current is then reduced by the converter buck ratio.

Reverse-Current Inhibit

The LT3800 contains a reverse-current inhibit feature to maximize efficiency during light load conditions. This mode of operation allows discontinuous operation, and is sometimes referred to as “pulse-skipping” mode. Refer to Figure 2.

This feature is enabled with Burst Mode operation, and can also be enabled while Burst Mode operation is disabled by shorting the BURST_EN pin to V_{FB}.

When reverse-current inhibit is enabled, the LT3800 sense amplifier detects inductor currents approaching zero and disables the synchronous switch for the remainder of the switch cycle. If the inductor current is allowed to go negative before the synchronous switch is disabled, the switch node could inductively kick positive with a high dv/dt. The LT3800 prevents this by incorporating a 10mV positive offset at the sense inputs.

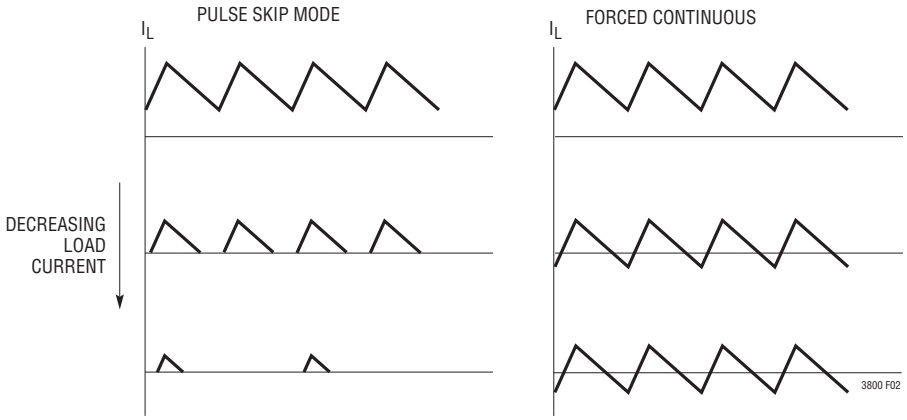


Figure 2. Inductor Current vs Mode

APPLICATIONS INFORMATION

With the reverse-current inhibit feature enabled, an LT3800 converter will operate much like a nonsynchronous converter during light loads. Reverse-current inhibit reduces resistive losses associated with inductor ripple currents, which improves operating efficiencies during light-load conditions.

An LT3800 DC/DC converter that is operating in reverse-inhibit mode has a minimum load requirement of 1mA (BURST_EN = V_{FB}). Since most applications use output-generated power for the LT3800, this requirement is met by the bias currents of the IC, however, for applications that do not derive power from the output, this requirement is easily accomplished by using a 1.2k resistor connected from V_{FB} to ground as one of the converter output voltage programming resistors (R1). There are no minimum load restrictions when in Burst Mode operation (BURST_EN < 0.5V) or continuous conduction mode (BURST_EN > 2.5V).

Soft-Start

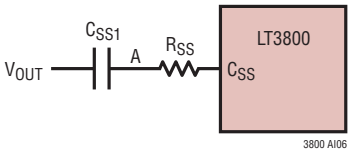
The LT3800 incorporates a programmable soft-start function to control start-up surge currents, limit output overshoot and for use in supply sequencing. The soft-start function directly monitors and controls output voltage slew rate during converter start-up.

As the output voltage of the converter rises, the soft-start circuit monitors $\delta V/\delta t$ current through a coupling capacitor and adjusts the voltage on the V_C pin to maintain an average value of 2µA. The soft-start function forces the programmed slew rate while the converter output rises to 95% regulation, which corresponds to 1.185V on the V_{FB} pin. Once 95% regulation is achieved, the soft-start circuit is disabled. The soft-start circuit will re-enable when the V_{FB} pin drops below 70% regulation, which corresponds to 300mV of control hysteresis on the V_{FB} pin, which allows for a controlled recovery from a 'brown-out' condition.

The desired soft-start rise time (t_{SS}) is programmed via a programming capacitor C_{SS1}, using a value that corresponds to 2µA average current during the soft-start interval. This capacitor value follows the relation:

$$C_{SS1} = \frac{2E^{-6} \bullet t_{SS}}{V_{OUT}}$$

R_{SS} is typically set to 200k for most applications.



Considerations for Low Voltage Output Applications

The LT3800 C_{SS} pin biases to 220mV during the soft-start cycle, and this voltage is increased at network node "A" by the 2µA signal current through R_{SS}, so the output has to reach this value before the soft-start function is engaged. The value of this output soft-start start-up voltage offset ($V_{OUT(SS)}$) follows the relation:

$$V_{OUT(SS)} = 220mV + R_{SS} \bullet 2E^{-6}$$

which is typically 0.64V for R_{SS} = 200k.

In some low voltage output applications, it may be desirable to reduce the value of this soft-start start-up voltage offset. This is possible by reducing the value of R_{SS}. With reduced values of R_{SS}, the signal component caused by voltage ripple on the output must be minimized for proper soft-start operation.

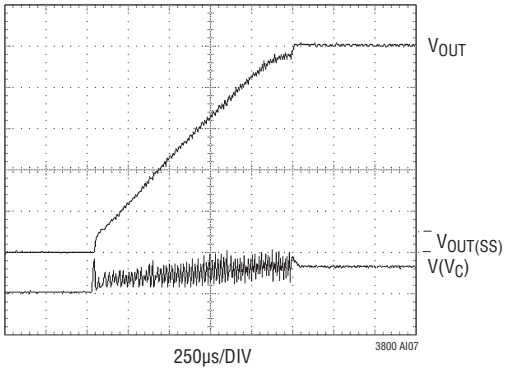
Peak-to-peak output voltage ripple (ΔV_{OUT}) will be imposed on node "A" through the capacitor C_{SS1}. The value of R_{SS} can be set using the following equation:

$$R_{SS} = \frac{\Delta V_{OUT}}{1.3E^{-6}}$$

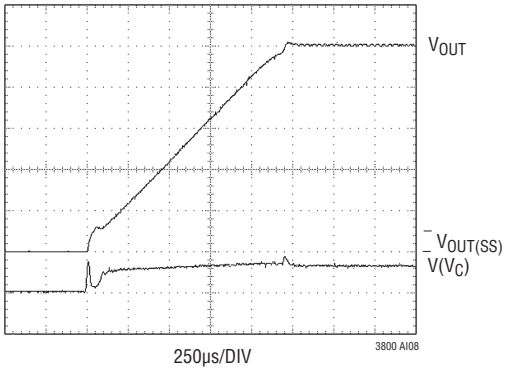
It is important to use low ESR output capacitors for LT3800 voltage converter designs to minimize this ripple voltage component. A design with an excessive ripple component can be evidenced by observing the V_C pin during the start cycle.

APPLICATIONS INFORMATION

Soft-Start Characteristic Showing Excessive Ripple Component



Desirable Soft-Start Characteristic



The soft-start cycle should be evaluated to verify that the reduced R_{SS} value allows operation without excessive modulation of the V_C pin before finalizing the design.

If the V_C pin has an excessive ripple component during the soft-start cycle, converter output ripple should be reduced or R_{SS} increased. Reduction in converter output ripple is typically accomplished by increasing output capacitance and/or reducing output capacitor ESR.

External Current Limit Foldback Circuit

An additional start-up voltage offset can occur during the period before the LT3800 soft-start circuit becomes active. Before the soft-start circuit throttles back the V_C pin in response to the rising output voltage, current as high as the peak programmed current limit (I_{MAX}) can flow in the inductor. Switching will stop once the soft-start circuit takes hold and reduces the voltage on the V_C pin, but the output voltage will continue to increase as the stored energy in the inductor is transferred to the output capacitor. With I_{MAX} flowing in the inductor, the resulting leading-edge rise on V_{OUT} due to energy stored in the inductor follows the relationship:

$$\Delta V_{OUT} = I_{MAX} \bullet \left(\frac{L}{C_{OUT}} \right)^{1/2}$$

Inductor current typically doesn't reach I_{MAX} in the few cycles that occur before soft-start becomes active, but can with high input voltages or small inductors, so the above relation is useful as a worst-case scenario.

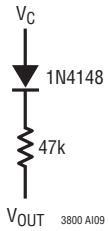
This energy transfer increase in output voltage is typically small, but for some low voltage applications with relatively small output capacitors, it can become significant. The voltage rise can be reduced by increasing output capacitance, which puts additional limitations on C_{OUT} for these low voltage supplies. Another approach is to add an external current limit foldback circuit which reduces the value of I_{MAX} during start-up.

An external current limit foldback circuit can be easily incorporated into an LT3800 DC/DC converter application by placing a 1N4148 diode and a 47k resistor from the converter output (V_{OUT}) to the LT3800's V_C pin. This limits the peak current to 0.25 • I_{MAX} when V_{OUT} = 0V. A current limit foldback circuit also has the added advantage of providing a reduced output current in the DC/DC converter during short-circuit fault conditions, so a foldback circuit may be useful even if the soft-start function is disabled.

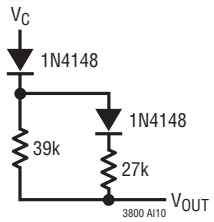
If the soft-start circuit is disabled by shorting the C_{SS} pin to ground, the external current limit fold-back circuit must be modified by adding an additional diode and resistor. The 2-diode, 2-resistor network shown also provides 0.25 • I_{MAX} when V_{OUT} = 0V.

APPLICATIONS INFORMATION

Current Limit Foldback Circuit for Applications That Use Soft-Start



Alternative Current Limit Foldback Circuit for Applications That Have Soft-Start Disabled



Adaptive Nonoverlap (NOL) Output Stage

The FET driver output stages implement adaptive nonoverlap control. This feature maintains a constant dead time, preventing shoot-through switch currents, independent of the type, size or operating conditions of the external switch elements.

Each of the two switch drivers contains a NOL control circuit, which monitors the output gate drive signal of the other switch driver. The NOL control circuits interrupt the "turn on" command to their associated switch driver until the other switch gate is fully discharged.

Antislope Compensation

Most current mode switching controllers use slope compensation to prevent current mode instability. The LT3800 is no exception. A slope-compensation circuit imposes an artificial ramp on the sensed current to increase the rising slope as duty cycle increases. Unfortunately, this additional ramp corrupts the sensed current value, reducing the achievable current limit value by the same amount as the added ramp represents. As such, current limit is typically reduced as duty cycles increase. The LT3800 contains circuitry to eliminate the current limit reduction typically associated with slope compensation. As the slope-compensation ramp is added to the sensed current, a similar ramp is added to the current limit threshold reference. The end result is that current limit is not compromised, so a LT3800 converter can provide full power regardless of required duty cycle.

Shutdown

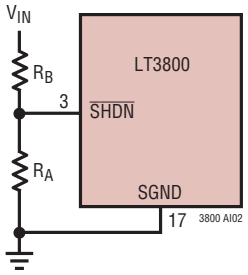
The LT3800 $\overline{SHDN}$ pin uses a bandgap generated reference threshold of 1.35V. This precision threshold allows use of the $\overline{SHDN}$ pin for both logic-level controlled applications and analog monitoring applications such as power supply sequencing.

The LT3800 operational status is primarily controlled by a UVLO circuit on the V_{CC} regulator pin. When the IC is enabled via the $\overline{SHDN}$ pin, only the V_{CC} regulator is enabled. Switching remains disabled until the UVLO threshold is achieved at the V_{CC} pin, when the remainder of the IC is enabled and switching commences.

Because an LT3800 controlled converter is a power transfer device, a voltage that is lower than expected on the input supply could require currents that exceed the sourcing capabilities of that supply, causing the system to lock up in an undervoltage state. Input supply start-up protection can be achieved by enabling the $\overline{SHDN}$ pin using a resistive divider from the V_{IN} supply to ground. Setting the divider output to 1.35V when that supply is at an adequate voltage prevents an LT3800 converter from drawing large currents until the input supply is able to provide the required power. 120mV of input hysteresis on the $\overline{SHDN}$ pin allows for almost 10% of input supply droop before disabling the converter.

APPLICATIONS INFORMATION

Programming LT3800 V_{IN} UVLO



The UVLO voltage, $V_{IN(UVLO)}$, is set using the following relation:

$$R_A = R_B \bullet \frac{V_{IN(UVLO)} - 1.35V}{1.35V}$$

If additional hysteresis is desired for the enable function, an external positive feedback resistor can be used from the LT3800 regulator output.

The shutdown function can be disabled by connecting the $\overline{SHDN}$ pin to V_{IN} through a large value pull-up resistor. This pin contains a low impedance clamp at 6V, so the $\overline{SHDN}$ pin will sink current from the pull-up resistor (R_{PU}):

$$I_{\overline{SHDN}} = \frac{V_{IN} - 6V}{R_{PU}}$$

Because this arrangement will pull the $\overline{SHDN}$ pin to the 6V clamp voltage, it will violate the 5V absolute maximum voltage rating of the pin. This is permitted, however, as long as the absolute maximum input current rating of 1mA is not exceeded. Input $\overline{SHDN}$ pin currents of <100µA are recommended; a 1MΩ or greater pull-up resistor is typically used for this configuration.

Inductor Selection

The primary criterion for inductor value selection in LT3800 applications is ripple current created in that inductor. Basic design considerations for ripple current are output voltage ripple, and the ability of the internal slope compensation waveform to prevent current mode instability. Once the value is determined, an inductor must also have a saturation current equal to or exceeding the maximum peak current in the inductor.

Ripple current (ΔI_L) in an inductor for a given value (L) can be approximated using the relation:

$$\Delta I_L = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \bullet \frac{V_{OUT}}{f_O \bullet L}$$

The typical range of values for ΔI is 20% to 40% of $I_{OUT(MAX)}$, where $I_{OUT(MAX)}$ is the maximum converter output load current. Ripple currents in this range typically yield a good design compromise between inductor performance versus inductor size and cost, and values in this range are generally a good starting point. A starting point inductor value can thus be determined using the relation:

$$L = V_{OUT} \bullet \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f_O \bullet 0.3 \bullet I_{OUT(MAX)}}$$

Use of smaller inductors increase output ripple currents, requiring more capacitance on the converter output. Also, with converter operation with duty cycles greater than 50%, the slope compensation criterion, described later, must be met. Designing for smaller ripple currents requires larger inductor values, which can increase converter cost and/or footprint.

APPLICATIONS INFORMATION

Some magnetics vendors specify a volt-second product in their data sheet. If they do not, consult the vendor to make sure the specification is not being exceeded by your design. The required volt-second product is calculated as follows:

$$\text{Volt-Second} \geq \frac{V_{OUT}}{f_O} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Magnetics vendors specify either the saturation current, the RMS current, or both. When selecting an inductor based on inductor saturation current, the peak current through the inductor, $I_{OUT(MAX)} + (\Delta I/2)$, is used. When selecting an inductor based on RMS current the maximum load current, $I_{OUT(MAX)}$, is used.

The requirement for avoiding current mode instability is keeping the rising slope of sensed inductor ripple current (S1) greater than the falling slope (S2). During continuous-current switcher operation, the rising slope of the current waveform in the switched inductor is less than the falling slope when operating at duty cycles (DC) greater than 50%. To avoid the instability condition during this operation, a false signal is added to the sensed current, increasing the perceived rising slope. To prevent current mode instability, the slope of this false signal (Sx) must be sufficient such that the sensed rising slope exceeds the falling slope, or S1 + Sx ≥ S2. This leads to the following relations:

$$Sx \geq S2\ (2DC - 1)/DC$$

where:

$$S2 \sim V_{OUT}/L$$

Solving for L yields a relation for the minimum inductance that will satisfy slope compensation requirements:

$$L_{MIN} = V_{OUT} \bullet \frac{2DC - 1}{DC \bullet Sx}$$

The LT3800 maximizes available dynamic range using a slope compensation generator that continuously increases the additional signal slope as duty cycle increases. The slope compensation waveform is calibrated at an 80% duty cycle, to generate an equivalent slope of at least $1E^5 \bullet I_{LIMIT}$ A/sec, where I_{LIMIT} is the programmed converter current limit. Current limit is programmed by using a sense resistor (R_S) such that $I_{LIMIT} = 150mV/R_S$, so the equation for the minimum inductance to meet the current mode instability criterion can be reduced to:

$$L_{MIN} = (5E^{-5})(V_{OUT})(R_S)$$

For example, with $V_{OUT} = 5V$ and $R_S = 20m\Omega$:

$$L_{MIN} = (5E^{-5})(5)(0.02) = 5\mu H$$

After calculating the minimum inductance value, the volt-second product, the saturation current and the RMS current for your design, an off the shelf inductor can be selected from a magnetics vendor. A list of magnetics vendors can be found at http://www.linear.com/ezone/vlinks or by contacting the Linear Technology Applications department.

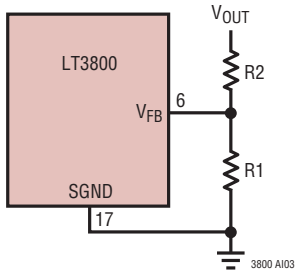
Output Voltage Programming

Output voltage is programmed through a resistor feedback network to V_{FB} (Pin 6) on the LT3800. This pin is the inverting input of the error amplifier, which is internally referenced to 1.231V. The divider is ratioed to provide 1.231V at the V_{FB} pin when the output is at its desired value. The output voltage is thus set following the relation:

$$R2 = R1 \bullet \left(\frac{V_{OUT}}{1.231} - 1\right)$$

when an external resistor divider is connected to the output as shown.

Programming LT3800 Output Voltage



APPLICATIONS INFORMATION

Power MOSFET Selection

External N-channel MOSFET switches are used with the LT3800. The positive gate-source drive voltage of the LT3800 for both switches is roughly equivalent to the V_{CC} supply voltage, for use of standard threshold MOSFETs.

Selection criteria for the power MOSFETs include the "ON" resistance ($R_{DS(ON)}$), total gate charge (Q_G), reverse transfer capacitance (C_{RSS}), maximum drain-source voltage (V_{DSS}) and maximum current.

The power FETs selected must have a maximum operating V_{DSS} exceeding the maximum V_{IN}. V_{GS} voltage maximum must exceed the V_{CC} supply voltage.

Total gate charge (Q_G) is used to determine the FET gate drive currents required. Q_G increases with applied gate voltage, so the Q_G for the maximum applied gate voltage must be used. A graph of Q_G vs. V_{GS} is typically provided in MOSFET data sheets.

In a configuration where the LT3800 linear regulator is providing V_{CC} and V_{BOOST} currents, the V_{CC} 8V output voltage can be used to determine Q_G. Required drive current for a given FET follows the simple relation:

$$I_{GATE} = Q_{G(8V)} \bullet f_O$$

$Q_{G(8V)}$ is the total FET gate charge for V_{GS} = 8V, and f_0 = operating frequency. If these currents are externally derived by backdriving V_{CC}, use the backfeed voltage to determine Q_G. Be aware, however, that even in a backfeed configuration, the drive currents for both boosted and synchronous FETs are still typically supplied by the LT3800 internal V_{CC} regulator during start-up. The LT3800 can start using FETs with a combined $Q_{G(8V)}$ up to 180nC.

Once voltage requirements have been determined, $R_{DS(ON)}$ can be selected based on allowable power dissipation and required output current.

In an LT3800 buck converter, the average inductor current is equal to the DC load current. The average currents through the main (bootstrapped) and synchronous (ground-referred) switches are:

$$I_{MAIN} = (I_{LOAD})(DC)$$

$$I_{SYNC} = (I_{LOAD})(1 - DC)$$

The $R_{DS(ON)}$ required for a given conduction loss can be calculated using the relation:

$$P_{LOSS} = I_{SWITCH}^2 \bullet R_{DS(ON)}$$

In high voltage applications (V_{IN} > 20V), the main switch is required to slew very large voltages. MOSFET transition losses are proportional to V_{IN}^2 and can become the dominant power loss term in the main switch. This transition loss takes the form:

$$P_{TR} \approx (k)(V_{IN})^2(I_{SWITCH})(C_{RSS})(f_O)$$

where k is a constant inversely related to the gate drive current, approximated by k = 2 in LT3800 applications, and I_{SWITCH} is the converter output current. The power loss terms for the switches are thus:

$$P_{MAIN}=(DC)(I_{SWITCH})^2(1+d)(R_{DS(ON)})+ 2(V_{IN})^2(I_{SWITCH})(C_{RSS})(f_O)$$

$$P_{SYNC} = (1 - DC)(I_{SWITCH})^2(1 + d)(R_{DS(ON)})$$

The (1 + d) term in the above relations is the temperature dependency of $R_{DS(ON)}$, typically given in the form of a normalized $R_{DS(ON)}$ vs Temperature curve in a MOSFET data sheet.

The C_{RSS} term is typically smaller for higher voltage FETs, and it is often advantageous to use a FET with a higher V_{DS} rating to minimize transition losses at the expense of additional $R_{DS(ON)}$ losses.

In some applications, parasitic FET capacitances couple the negative going switch node transient onto the bottom gate drive pin of the LT3800, causing a negative voltage in excess of the Absolute Maximum Rating to be imposed on that pin. Connection of a catch Schottky diode from this pin to ground will eliminate this effect. A 1A current rating is typically sufficient for the diode.

Input Capacitor Selection

The large currents typical of LT3800 applications require special consideration for the converter input and output supply decoupling capacitors. Under normal steady state buck operation, the source current of the main switch MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. Most of this current is provided by the input bypass capacitor.

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To prevent large input voltage transients and avoid bypass capacitor heating, a low ESR input capacitor sized for the maximum RMS current must be used. This maximum capacitor RMS current follows the relation:

$$I_{RMS} = \frac{I_{MAX}\left(V_{OUT}\left(V_{IN} - V_{OUT}\right)\right)^{\frac{1}{2}}}{V_{IN}}$$

which peaks at a 50% duty cycle, when $I_{RMS} = I_{MAX}/2$.

The bulk capacitance is calculated based on an acceptable maximum input ripple voltage, ΔV_{IN}, which follows the relation:

$$C_{IN(BULK)} = I_{OUT(MAX)} \bullet \frac{\frac{V_{OUT}}{V_{IN}}}{\Delta V_{IN} \bullet f_O}$$

ΔV is typically on the order of 100mV to 200mV. Aluminum electrolytic capacitors are a good choice for high voltage, bulk capacitance due to their high capacitance per unit area.

The capacitor voltage rating must be rated greater than $V_{IN(MAX)}$. The combination of aluminum electrolytic capacitors and ceramic capacitors is a common approach to meeting supply input capacitor requirements. Multiple capacitors are also commonly paralleled to meet size or height requirements in a design.

Capacitor ripple current ratings are often based on only 2000 hours (three months) lifetime; it is advisable to derate either the ESR or temperature rating of the capacitor for increased MTBF of the regulator.

Output Capacitor Selection

The output capacitor in a buck converter generally has much less ripple current than the input capacitor. Peak-to-peak ripple current is equal to that in the inductor (ΔI_L), typically a fraction of the load current. C_{OUT} is selected to reduce output voltage ripple to a desirable value given an expected output ripple current. Output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L(ESR + [(8)(f_O) \bullet C_{OUT}]^{-1})$$

where f_O = operating frequency.

ΔV_{OUT} increases with input voltage, so the maximum operating input voltage should be used for worst-case calculations. Multiple capacitors are often paralleled to meet ESR requirements. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the required RMS current rating. An additional ceramic capacitor in parallel is commonly used to reduce the effect of parasitic inductance in the output capacitor, which reduces high frequency switching noise on the converter output.

Increasing inductance is an option to reduce ESR requirements. For extremely low ΔV_{OUT}, an additional LC filter stage can be added to the output of the supply. Application Note 44 has information on sizing an additional output LC filter.

Layout Considerations

The LT3800 is typically used in DC/DC converter designs that involve substantial switching transients. The switch drivers on the IC are designed to drive large capacitances and, as such, generate significant transient currents themselves. Careful consideration must be made regarding supply bypass capacitor locations to avoid corrupting the ground reference used by IC.

Typically, high current paths and transients from the input supply and any local drive supplies must be kept isolated from SGND, to which sensitive circuits such as the error amp reference and the current sense circuits are referred.

Effective grounding can be achieved by considering switch current in the ground plane, and the return current paths of each respective bypass capacitor. The V_{IN} bypass return, V_{CC} bypass return, and the source of the synchronous FET carry PGND currents. SGND originates at the negative terminal of the V_{OUT} bypass capacitor, and is the small signal reference for the LT3800.

Don't be tempted to run small traces to separate ground paths. A good ground plane is important as always, but PGND referred bypass elements must be oriented such that transient currents in these return paths do not corrupt the SGND reference.

During the dead-time between switch conduction, the body diode of the synchronous FET conducts inductor

APPLICATIONS INFORMATION

current. Commutating this diode requires a significant charge contribution from the main switch. At the instant the body diode commutates, a current discontinuity is created and parasitic inductance causes the switch node to fly up in response to this discontinuity. High currents and excessive parasitic inductance can generate extremely fast dV/dt rise times. This phenomenon can cause avalanche breakdown in the synchronous FET body diode, significant inductive overshoot on the switch node, and shoot-through currents via parasitic turn-on of the synchronous FET. Layout practices and component orientations that minimize parasitic inductance on this node is critical for reducing these effects.

Ringing waveforms in a converter circuit can lead to device failure, excessive EMI, or instability. In many cases, you can damp a ringing waveform with a series RC network across the offending device. In LT3800 applications, any ringing will typically occur on the switch node, which can usually be reduced by placing a snubber across the synchronous FET. Use of a snubber network, however, should be considered a last resort. Effective layout practices typically reduce ringing and overshoot, and will eliminate the need for such solutions.

Effective grounding techniques are critical for successful DC/DC converter layouts. Orient power path components such that current paths in the ground plane do not cross through signal ground areas. Signal ground refers to the Exposed Pad on the backside of the LT3800 IC. SGND is referenced to the (–) terminal of the V_{OUT} decoupling capacitor and is used as the converter voltage feedback reference. Power ground currents are controlled on the LT3800 via the PGND pin, and this ground references the high current synchronous switch drive components, as well as the local V_{CC} supply. It is important to keep PGND and SGND voltages consistent with each other, so separating these grounds with thin traces is not recommended. When the synchronous FET is turned on, gate drive surge currents return to the LT3800 PGND pin from the FET source. The BOOST supply refresh surge currents also return through this same path. The synchronous FET must be oriented such that these PGND return currents do not corrupt the SGND reference. Problems caused by the PGND return path are generally recognized during heavy load conditions, and are typically evidenced as multiple switch pulses occurring during a single 5µs switch cycle. This behavior indicates that SGND is being corrupted and grounding should be improved. SGND corruption can often be eliminated, however, by adding a small capacitor (100pF-200pF) across the synchronous switch FET from drain to source.

The high di/dt loop formed by the switch MOSFETs and the input capacitor (C_{IN}) should have short wide traces to minimize high frequency noise and voltage stress from inductive ringing. Surface mount components are preferred to reduce parasitic inductances from component leads. Connect the drain of the main switch MOSFET directly to the (+) plate of C_{IN}, and connect the source of the synchronous switch MOSFET directly to the (–) terminal of C_{IN}. This capacitor provides the AC current to the switch MOSFETs. Switch path currents can be controlled by orienting switch FETs, the switched inductor, and input and output decoupling capacitors in close proximity to each other.

Locate the V_{CC} and BOOST decoupling capacitors in close proximity to the IC. These capacitors carry the MOSFET drivers' high peak currents. Locate the small-signal components away from high frequency switching nodes (BOOST, SW, TG, V_{CC} and BG). Small-signal nodes are oriented on the left side of the LT3800, while high current switching nodes are oriented on the right side of the IC to simplify layout. This also helps prevent corruption of the SGND reference.

Connect the V_{FB} pin directly to the feedback resistors independent of any other nodes, such as the $SENSE^-$ pin. The feedback resistors should be connected between the (+) and (–) terminals of the output capacitor (C_{OUT}).

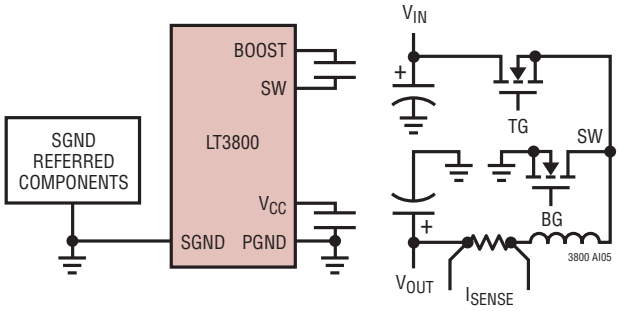
Locate the feedback resistors in close proximity to the LT3800 to minimize the length of the high impedance V_{FB} node.

The $SENSE^-$ and $SENSE^+$ traces should be routed together and kept as short as possible.

APPLICATIONS INFORMATION

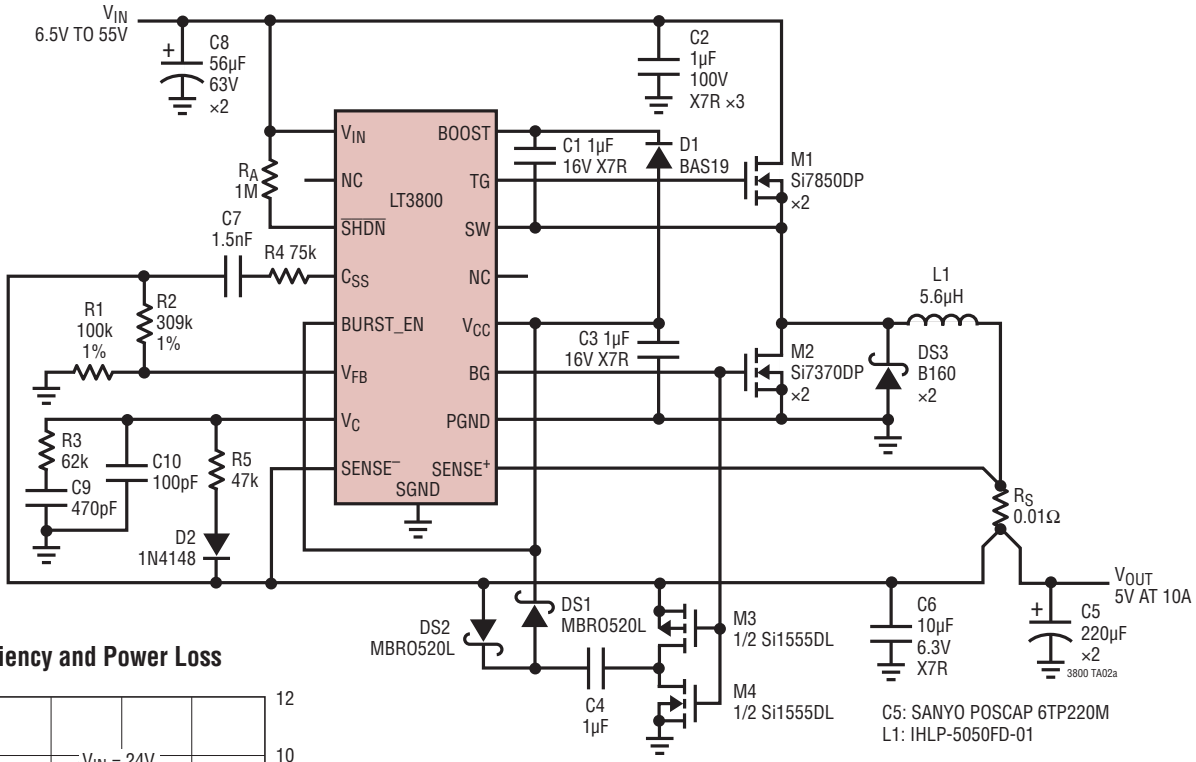
The LT3800 packaging has been designed to efficiently remove heat from the IC via the Exposed Pad on the backside of the package. The Exposed Pad is soldered to a copper footprint on the PCB. This footprint should be made as large as possible to reduce the thermal resistance of the IC case to ambient air.

Orientation of Components Isolates Power Path and PGND Currents, Preventing Corruption of SGND Reference

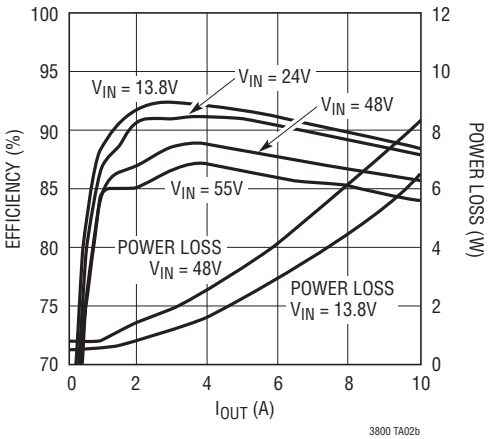


TYPICAL APPLICATIONS

6.5V-55V to 5V 10A DC/DC Converter with Charge Pump Doubler V_{CC} Refresh and Current Limit Foldback



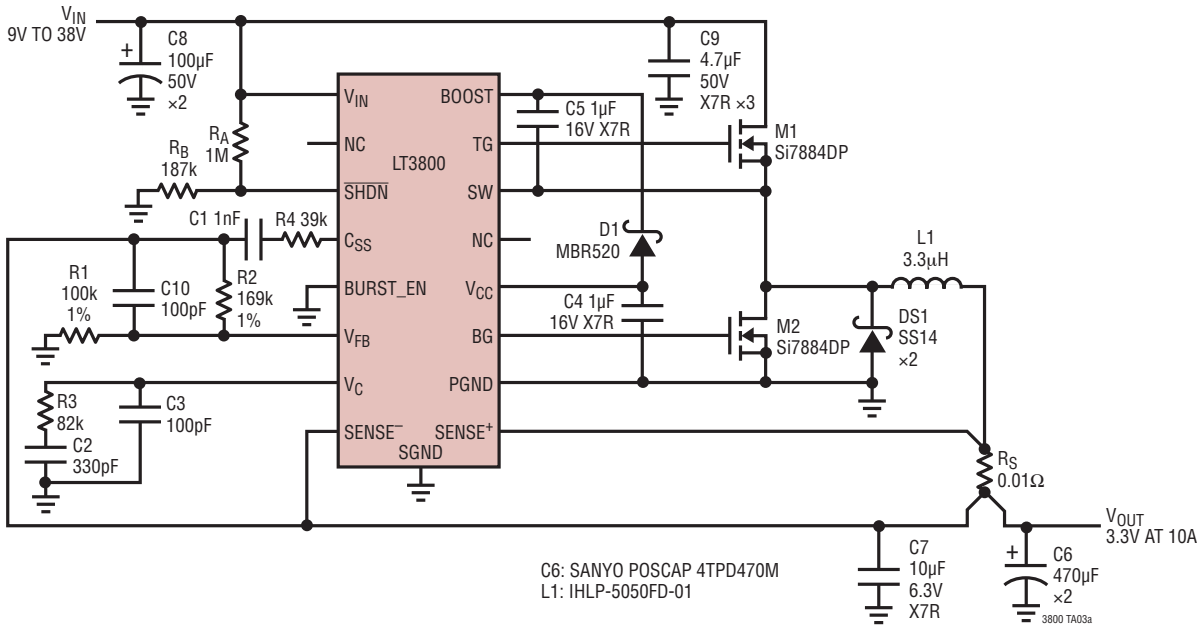
Efficiency and Power Loss



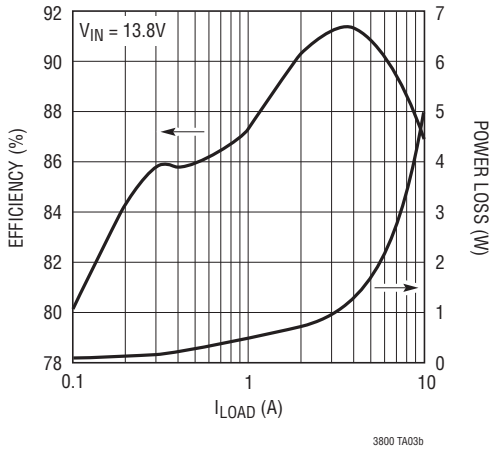
3800 TA02b

TYPICAL APPLICATIONS

9V-38V to 3.3V 10A DC/DC Converter with Input UVLO and Burst Mode Operation
No Load I(V_{IN}) = 100µA

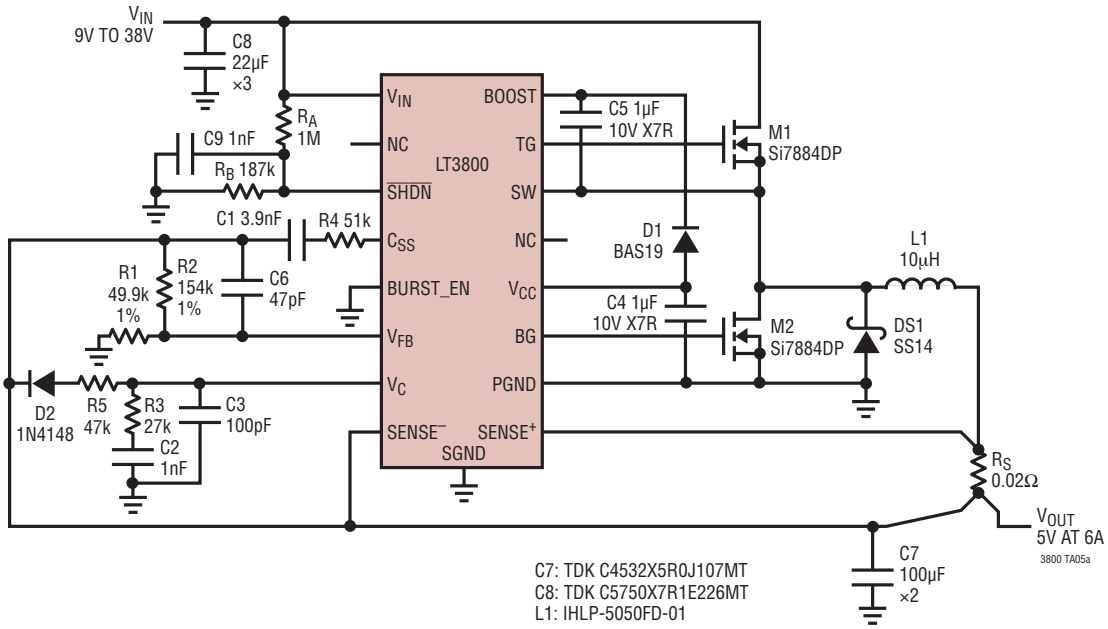


Efficiency and Power Loss

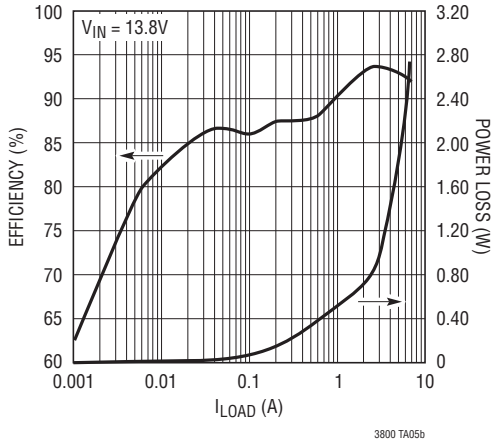


TYPICAL APPLICATIONS

9V-38V to 5V 6A DC/DC Converter with All Ceramic Capacitors, Input UVLO, Burst Mode Operation and Current Limit Foldback



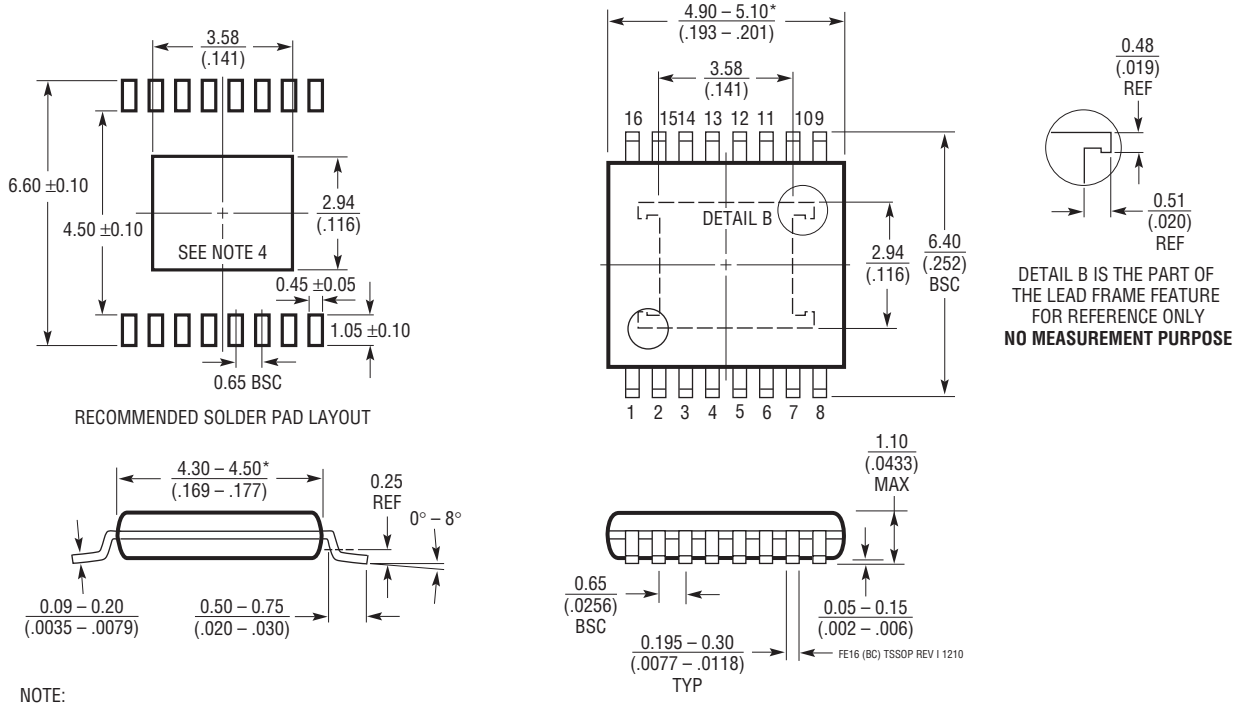
Efficiency and Power Loss



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev I)
Exposed Pad Variation BC



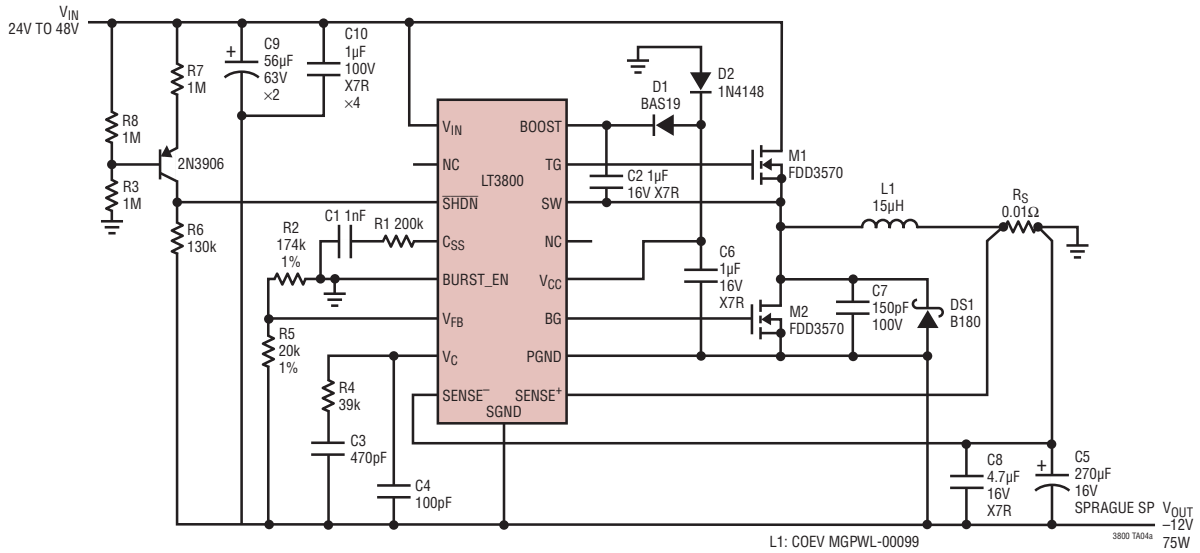
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY (Revision history begins at Rev C)

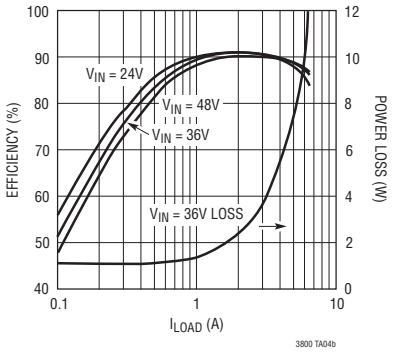
REV	DATE	DESCRIPTION	PAGE NUMBER
C	9/11	Minor correction to TA04a schematic	24

TYPICAL APPLICATION

24V-48V to –12V 75W Inverting DC/DC Converter with V_{IN} UVLO



Efficiency and Power Loss



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1735	Synchronous Step-Down Controller	4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 6V, I_{OUT} ≤ 20A
LTC1778	No R_{SENSE}™ Synchronous Step-Down Controller	Current Mode Without Using Sense Resistor, 4V ≤ V_{IN} ≤ 36V
LT®1934	Micropower Step-Down Switching Regulator	3.2V ≤ V_{IN} ≤ 34V, 300mA Switch, ThinSOT™ Package
LT1952	Synchronous Single Switch Forward Converter	25W to 500W Isolated Power Supplies, Small Size, High Efficiency
LT1976	60V Switching Regulator	3.2V ≤ V_{IN} ≤ 60V, 1.5A Switch, 16-Lead TSSOP
LT3010	3V to 80V LDO	50mA Output Current, 1.275V ≤ V_{OUT} ≤ 60V
LT3430/LT3431	3A, 60V Switching Regulators	5.5V ≤ V_{IN} ≤ 60V, 200kHz, 16-Lead TSSOP
LTC3703	100V Synchronous Step-Down Controller	Large 1Ω Gate Drivers, No R_{SENSE}
LTC3703-5	60V Synchronous Step-Down Controller	Large 1Ω Gate Drivers, No R_{SENSE}
LTC3727-1	High V_{OUT} 2-Phase Dual Step-Down Controller	0.8V ≤ V_{OUT} ≤ 14V, PLL: 250kHz to 550kHz
LTC3728L	2-Phase, Dual Synchronous Step-Down Controller	550kHz, PLL: 250kHz to 550kHz, 4V ≤ V_{IN} ≤ 36V

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