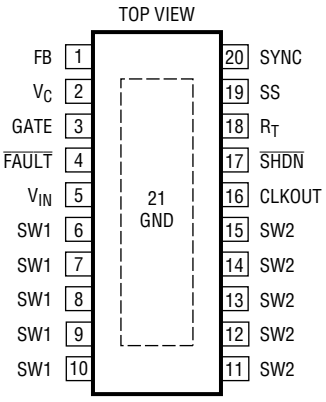
ABSOLUTE MAXIMUM RATINGS

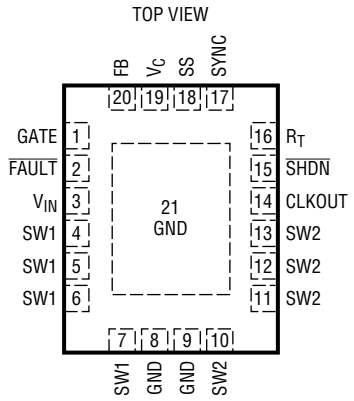
(Note 1)

V_{IN} Voltage ..... –0.3V to 40V
SW1/SW2 Voltage ..... –0.4V to 42V
R_T Voltage ..... –0.3V to 5V
SS, FB Voltage ..... –0.3V to 2.5V
V_C Voltage ..... –0.3V to 2V
$\overline{SHDN}$ Voltage ..... –0.3V to 40V
SYNC Voltage ..... –0.3V to 5.5V
GATE Voltage ..... –0.3V to 80V
$\overline{FAULT}$ ..... –0.3V to 40V
$\overline{FAULT}$ Current ..... ±0.5mA
CLKOUT ..... –0.3V to 3V
CLKOUT Current ..... ±1mA
Operating Junction Temperature Range
LT3579E (Notes 2, 4) ..... –40°C to 125°C
LT3579I (Notes 2, 4) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 38°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB



UFD PACKAGE
20-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 2.7°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3579EFE#PBF	LT3579EFE#TRPBF	LT3579FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT3579IFE#PBF	LT3579IFE#TRPBF	LT3579FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT3579EUFD#PBF	LT3579EUFD#TRPBF	3579	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3579IUFD#PBF	LT3579IUFD#TRPBF	3579	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3579EFE-1#PBF	LT3579EFE-1#TRPBF	LT3579FE-1	20-Lead Plastic TSSOP	–40°C to 125°C
LT3579IFE-1#PBF	LT3579IFE-1#TRPBF	LT3579FE-1	20-Lead Plastic TSSOP	–40°C to 125°C
LT3579EUFD-1#PBF	LT3579EUFD-1#TRPBF	35791	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3579IUFD-1#PBF	LT3579IUFD-1#TRPBF	35791	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{\overline{SHDN}} = V_{IN}$, $V_{\overline{FAULT}} = V_{IN}$ unless otherwise noted. (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●		2.3	2.5	V
V_{IN} Overvoltage Lockout			16.2	18.7	21.2	V
Positive Feedback Voltage		●	1.195	1.215	1.230	V
Negative Feedback Voltage		●	3	9	16	mV
Positive FB Pin Bias Current	V_{FB}=Positive Feedback Voltage, Current into Pin	●	80.5	83.3	85	µA
Negative FB Pin Bias Current	V_{FB}=Negative Feedback Voltage, Current out of Pin	●	81	83.3	85.5	µA
Error Amp Transconductance	ΔI=10µA			250		µmhos
Error Amp Voltage Gain				70		V/V
Quiescent Current	Not Switching			1.9	2.4	mA
Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V			0	1	µA
Reference Line Regulation	2.5V ≤ V_{IN} ≤ 15V			0.01	0.05	%/V
Switching Frequency, f_{OSC}	R_T = 34kΩ	●	2.2	2.5	2.8	MHz
	R_T = 432kΩ	●	175	200	225	kHz
Switching Frequency in Foldback	Compared to Normal f_{OSC}			1/6		ratio
Switching Frequency Range	Free-Running or Synchronizing	●	200		2500	kHz
SYNC High Level for Sync		●	1.3			V
SYNC Low Level for Sync		●			0.4	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V		20		80	%
Recommended Minimum SYNC Ratio f_{SYNC}/f_{OSC}				3/4		
Minimum Off-Time				45		nS
Minimum On-Time				55		nS
SW1 Current Limit	At All Duty Cycles (Note 3)	●	3.4	4.2	5.1	A
SW Current Sharing, I_{SW2}/I_{SW1}	SW1 and SW2 Tied Together			0.78		A/A
SW1 + SW2 Current Limit	I_{SW2}/I_{SW1} = 0.78, At All Duty Cycles (Note 3)	●	6	7.5	9.4	A
Switch V_{CESAT}	SW1 and SW2 Tied Together, $I_{SW1} + I_{SW2}$ = 5.5A (Note 5)			250	350	mV
SW1 Leakage Current	V_{SW1} = 5V			0.01	1	µA
SW2 Leakage Current	V_{SW2} = 5V			0.01	1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{\overline{SHDN}} = V_{IN}$, $V_{\overline{FAULT}} = V_{IN}$ unless otherwise noted. (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Soft-Start Charge Current	V_{SS} = 30mV, Current Flows Out of SS pin	●	5.7	8.7	11.3	µA
Soft-Start Discharge Current	Part in FAULT V_{SS} = 2.1V, Current Flows into SS Pin	●	5.7	8.7	11.3	µA
Soft-Start High Detection Voltage	Part in FAULT	●	1.65	1.8	1.95	V
Soft-Start Low Detection Voltage	Part Exiting FAULT	●	30	50	85	mV
$\overline{SHDN}$ Minimum Input Voltage High	Active Mode, $\overline{SHDN}$ Rising Active Mode, $\overline{SHDN}$ Falling	● ●	1.27 1.24	1.33 1.3	1.41 1.38	V V
$\overline{SHDN}$ Input Voltage Low	Shutdown Mode	●			.3	V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 1.3V $V_{\overline{SHDN}}$ = 0V		 9.5	40 11.4 0	60 13.4 0.1	µA µA µA
CLKOUT Output Voltage High	C_{CLKOUT} = 50pF		1.9	2.1	2.3	V
CLKOUT Output Voltage Low	C_{CLKOUT} = 50pF			100	200	mV
CLKOUT Duty Cycle	LT3579, T_J = 25°C			42		%
	LT3579-1, All T_J			50		%
CLKOUT Rise Time	C_{CLKOUT} = 50pF			12		ns
CLKOUT Fall Time	C_{CLKOUT} = 50pF			8		ns
GATE Pull Down Current	V_{GATE} = 3V V_{GATE} = 80V	● ●	800 800	933 933	1100 1100	µA µA
GATE Leakage Current	V_{GATE} = 50V, GATE Off			0.01	1	µA
$\overline{FAULT}$ Output Voltage Low	50µA into $\overline{FAULT}$ Pin	●		100	300	mV
$\overline{FAULT}$ Leakage Current	$V_{\overline{FAULT}}$ = 40V, $\overline{FAULT}$ Off			0.01	1	µA
$\overline{FAULT}$ Input Voltage Low Threshold		●	700	750	800	mV
$\overline{FAULT}$ Input Voltage High Threshold		●	950	1000	1050	mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3579E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3579I is guaranteed over the full –40°C to 125°C operating junction temperature range.

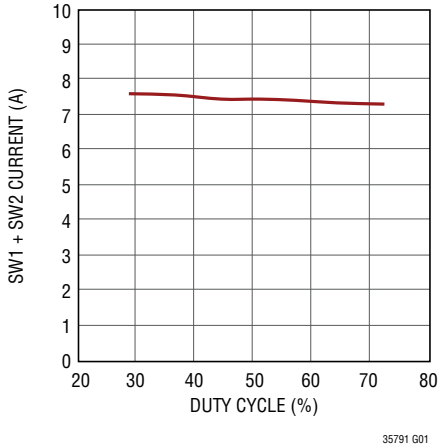
Note 3: Current limit guaranteed by design and/or correlation to static test.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation over the specified maximum operating junction temperature may impair device reliability.

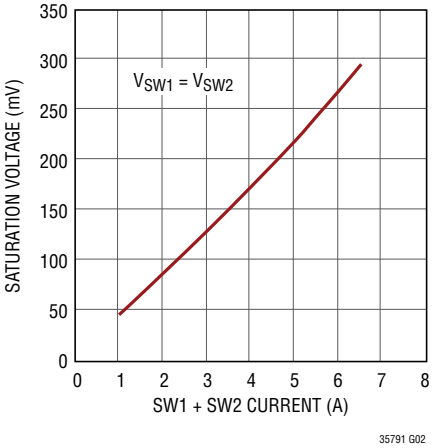
Note 5: The UFD package switch V_{CESAT} is guaranteed by design, characterization and bench correlation.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

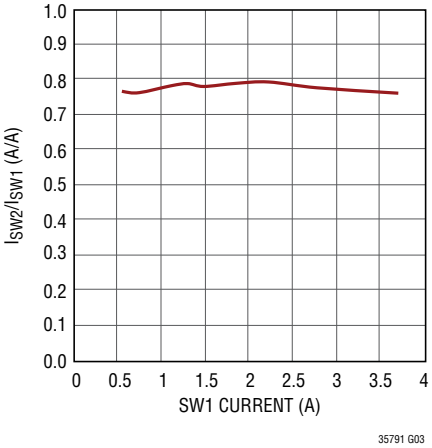
Switch Current Limit



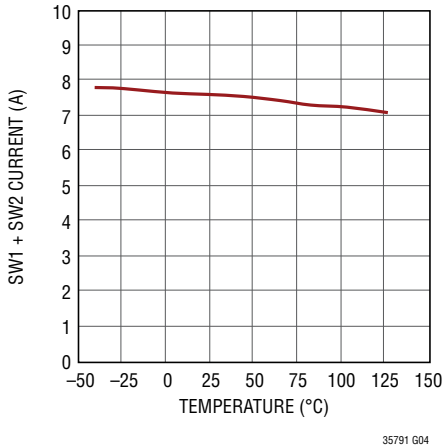
Switch Saturation Voltage



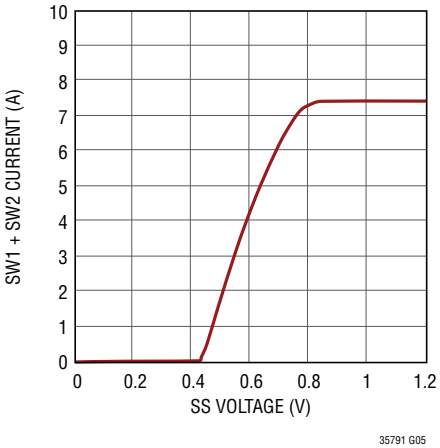
Switch Current Sharing



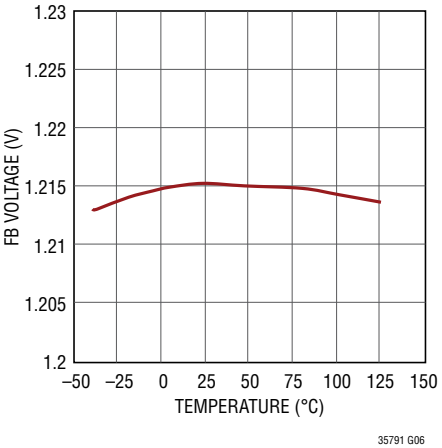
Switch Current Limit vs Temperature



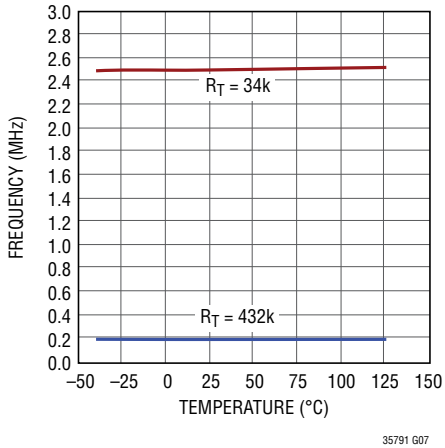
Commanded Switch Current vs SS



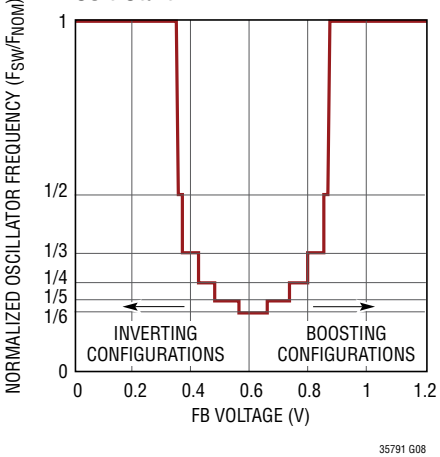
Positive Feedback Voltage



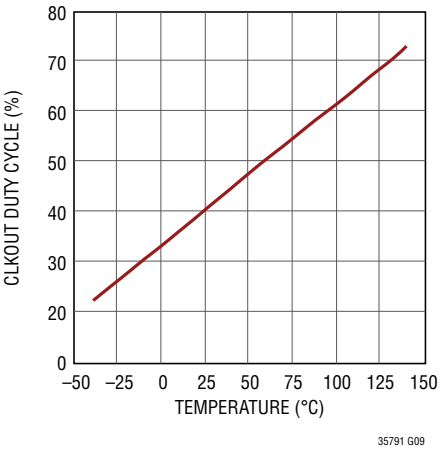
Oscillator Frequency



Oscillator Frequency During Soft-Start

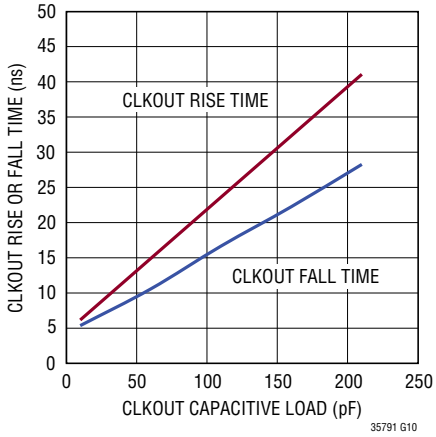


CLKOUT Duty Cycle



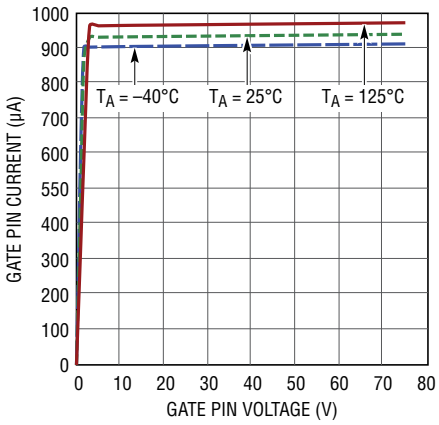
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

CLKOUT Rise Time at 1MHz



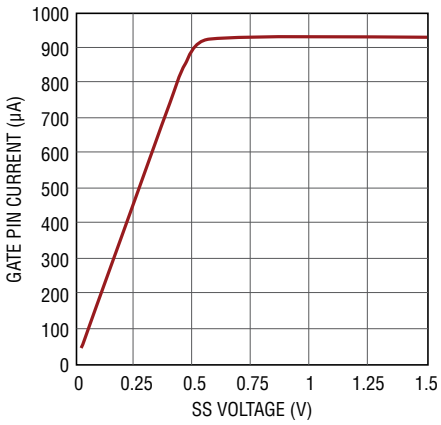
35791 G10

Gate Pin Current (V_{SS} = 2.1V)



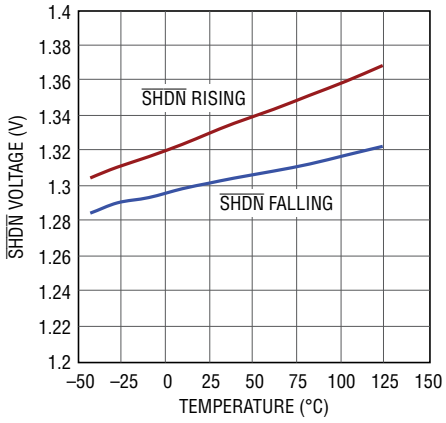
35791 G11

Gate Pin Current (V_{GATE} = 5V)



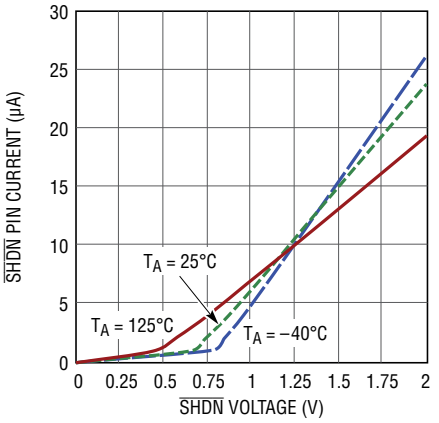
35791 G12

Active/Lockout Threshold



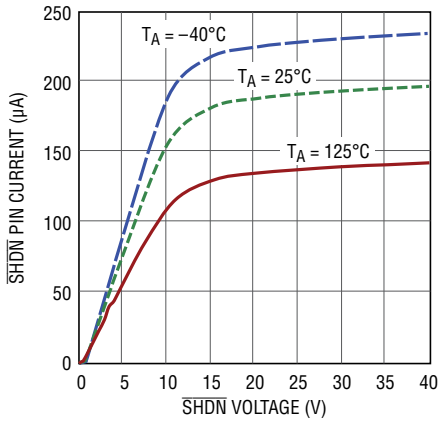
35791 G13

SHDN Pin Current



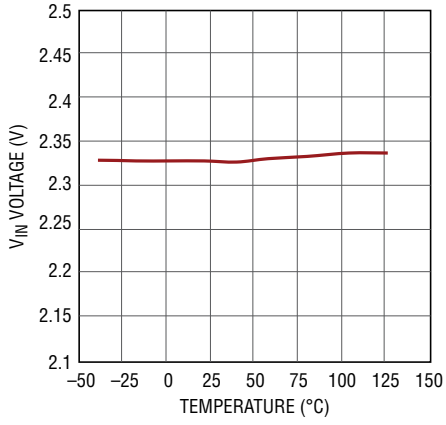
35791 G14

SHDN Pin Current



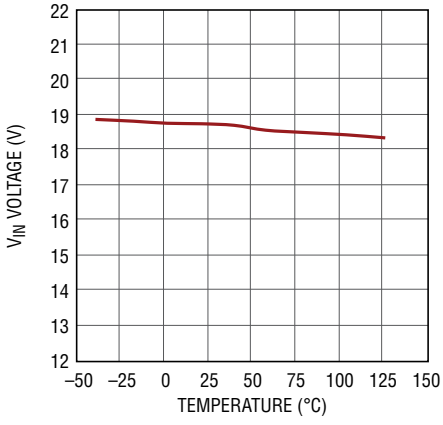
35791 G15

Internal UVLO



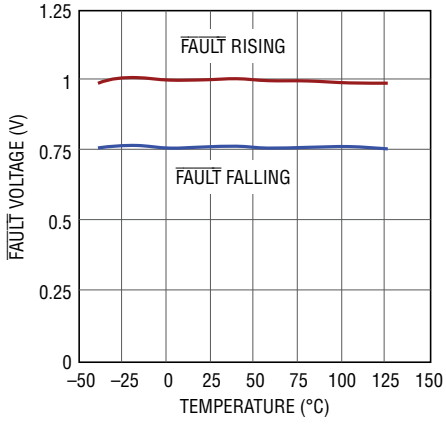
35791 G16

V_{IN} OVLO



35791 G17

FAULT Input Threshold



35791 G18

PIN FUNCTIONS (QFN/TSSOP)

GATE (Pin 1/Pin 3): PMOS Gate Drive Pin. The GATE pin is a pull-down current source, and can be used to drive the gate of an external PMOS transistor for output short circuit protection or output disconnect. The GATE pin current increases linearly with the SS pin's voltage, with a maximum pull-down current of 933µA at SS voltages exceeding 500mV. Note that if the SS voltage is greater than 500mV, and the GATE pin voltage is less than 2V, the GATE pin looks like a 2kΩ impedance to ground. See the Appendix for more information.

$\overline{\text{FAULT}}$ (Pin 2/Pin 4): Fault Indication Pin. This active low, bidirectional pin can either be pulled low (below 750mV) by an external source, or internally by the chip to indicate a fault. When pulled low, this pin causes the power switches to turn off, the GATE pin to become high impedance, the CLKOUT pin to become disabled, and the SS pin to go through a charge/discharge sequence. The end/absence of a fault is indicated when the voltage on this pin exceeds 1V. A pull-up resistor or some other form of pull-up network needs to exist on this pin to pull it above 1V in the absence of a fault.

V_{IN} (Pin 3/Pin 5): Input Supply Pin. Must be locally bypassed.

SW1 (Pins 4 - 7/Pins 6 - 10): Master Switch Pin. This is the collector of the internal master NPN power switch. SW1 is designed to handle a peak collector current of 3.4A (minimum). Minimize the metal trace area connected to this pin to minimize EMI.

GND (Pins 8, 9, Exposed Pad Pin 21/Exposed Pad Pin 21): Ground. Must be soldered directly to local ground plane.

SW2 (Pins 10-13/Pins 11-15): Slave Switch Pin. This is the collector of the internal slave NPN power switch. SW2 is designed to handle a peak collector current of 2.6A (minimum). Minimize the metal trace area connected to this pin to minimize EMI.

CLKOUT (Pin 14/Pin 16): Clock Output Pin. Use this pin to synchronize one or more other ICs to the LT3579. This pin oscillates at the same frequency as the internal oscillator of the part or as the SYNC pin. CLKOUT may also be used as a temperature monitor since the CLKOUT pin's duty cycle varies linearly with the part's junction temperature. The CLKOUT pin signal of the LT3579-1 is 180° out of phase with the internal oscillator or SYNC pin, and the duty cycle is fixed at ~50%. The LT3579-1 is useful for multiphase switching regulators.

$\overline{\text{SHDN}}$ (Pin 15/Pin 17): Shutdown Pin. In conjunction with the UVLO (undervoltage lockout) circuit, this pin is used to enable/disable the chip and restart the soft-start sequence. Drive below 0.3V to disable the chip with very low quiescent current. Drive above 1.33V (typical) to activate the chip and restart the soft-start sequence. Do not float this pin.

RT (Pin 16/Pin 18): Timing Resistor Pin. Adjusts the LT3579's switching frequency. Place a resistor from this pin to ground to set the frequency to a fixed free running level. Do not float this pin.

SYNC (Pin 17/Pin 20): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock must exceed 1.3V, and the low level must be less than 0.4V. Drive this pin to less than 0.4V to revert to the internal free running clock. See the Applications Information section for more information.

SS (Pin 18/Pin 19): Soft-Start Pin. Place a soft-start capacitor here. Upon start-up, the SS pin will be charged by a (nominally) 250kΩ resistor to ~2.1V. During a fault, the SS pin will be slowly charged up and discharged as part of a timeout sequence.

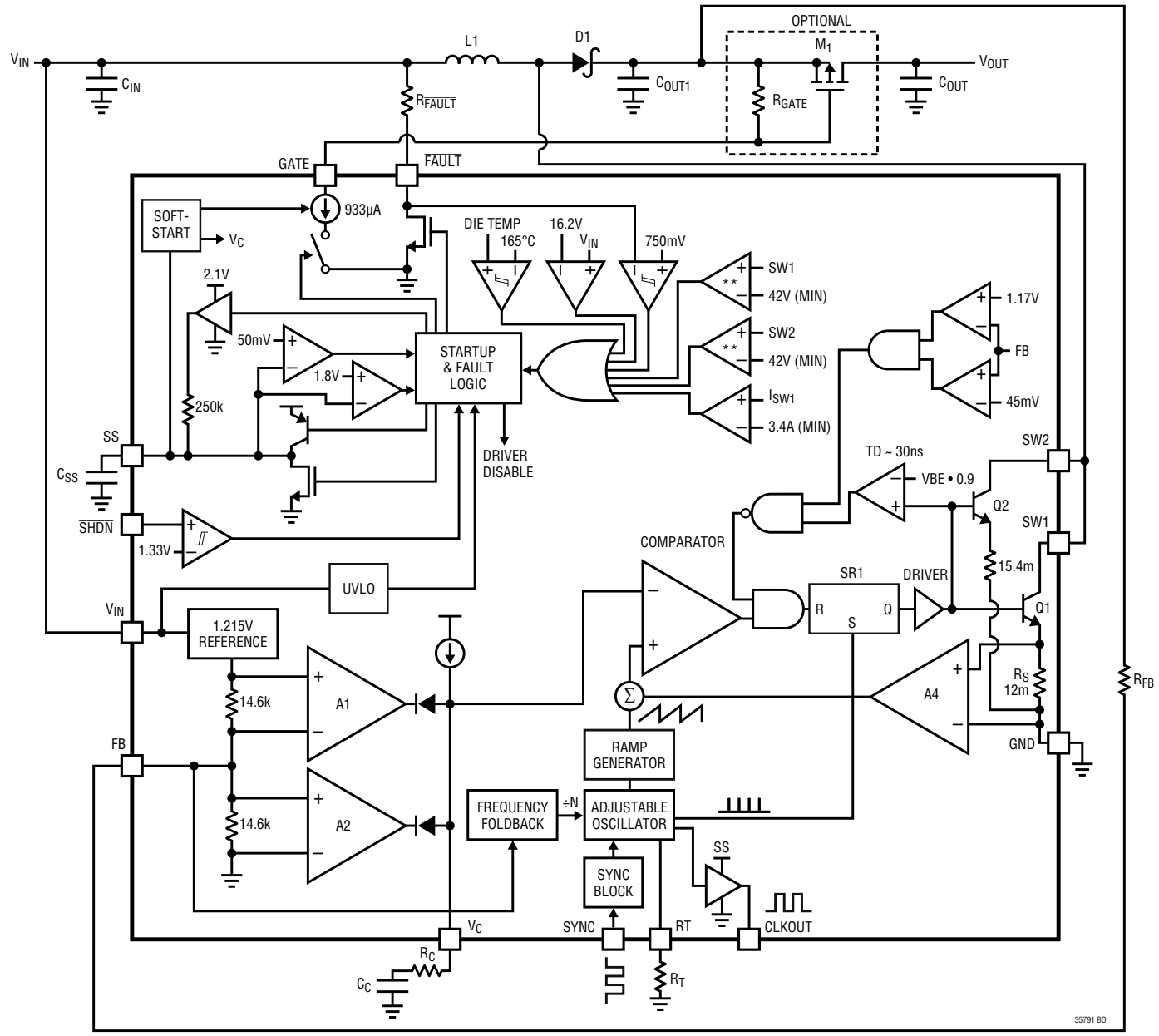
V_C (Pin 19/Pin 2): Error Amplifier Output Pin. Tie external compensation network to this pin.

FB (Pin 20/Pin 1): Positive and Negative Feedback Pin. For a Boost or Inverting Converter, tie a resistor from the FB pin to V_{OUT} according to the following equations:

$$R_{FB} = \left(\frac{V_{OUT} - 1.215V}{83.3\mu A}\right); \text{Boost or SEPIC Converter}$$

$$R_{FB} = \left(\frac{|V_{OUT}| + 9mV}{83.3\mu A}\right); \text{Inverting Converter}$$

BLOCK DIAGRAM



** SW OVERVOLTAGE PROTECTION IS NOT GUARANTEED TO PROTECT THE LT3579/LT3579-1 DURING SW OVERVOLTAGE EVENTS.

Figure 1. Block Diagram

STATE DIAGRAM

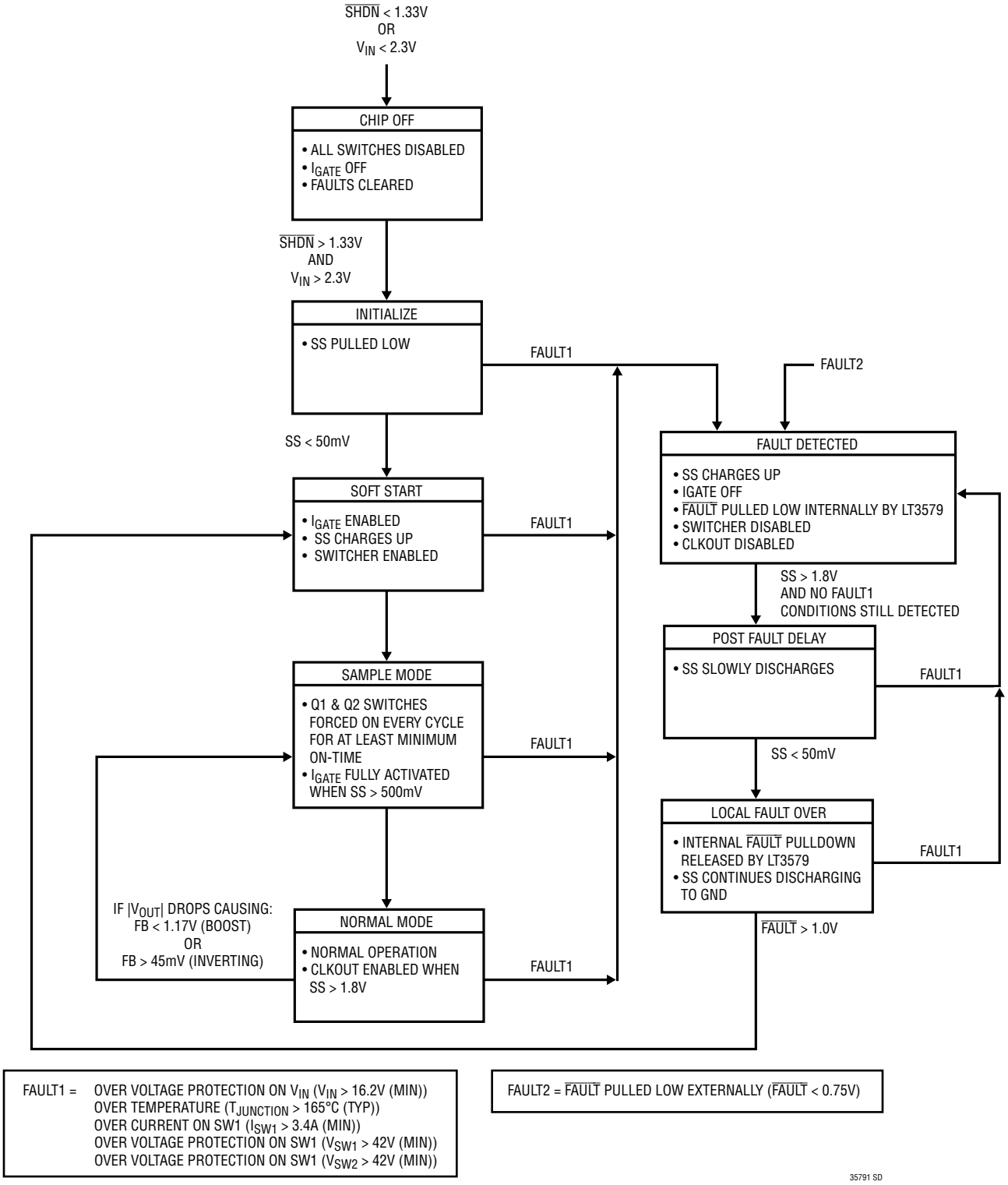


Figure 2. State Diagram

OPERATION

OPERATION – OVERVIEW

The LT3579 uses a constant-frequency, current mode control scheme to provide excellent line and load regulation. The part's undervoltage lockout (UVLO) function, together with soft-start and frequency foldback, offers a controlled means of starting up. Fault features are incorporated in the LT3579 to aid in the detection of output shorts, over-voltage, and overtemperature conditions. Refer to the Block Diagram (Figure 1) and the State Diagram (Figure 2) for the following description of the part's operation.

OPERATION – START-UP

Several functions are provided to enable a very clean start-up for the LT3579.

Precise Turn-On Voltage

The $\overline{SHDN}$ pin compares to an internal voltage reference to give a precise turn on voltage level. Taking the $\overline{SHDN}$ pin above 1.33V (typical) enables the part. Taking the $\overline{SHDN}$ pin below 0.3V shuts down the chip, resulting in extremely low quiescent current. The $\overline{SHDN}$ pin has 30mV of hysteresis to protect against glitches and slow ramping.

Undervoltage-Lockout (UVLO)

The $\overline{SHDN}$ pin can also be used to create a configurable UVLO. The UVLO function sets the turn on/off of the LT3579 at a desired input voltage (VIN_{UVLO}). Figure 3 shows how a resistor divider (or single resistor) from V_{IN} to the $\overline{SHDN}$ pin can be used to set VIN_{UVLO}. R_{UVLO2} is optional. It may be left out, in which case set it to infinite in the equation below. For increased accuracy, set $R_{UVLO2} \leq 10k\Omega$. Pick R_{UVLO1} as follows:

$$R_{UVLO1} = \frac{VIN_{UVLO} - 1.33V}{\left(\frac{1.33V}{R_{UVLO2}}\right) + 11.6\mu A}$$

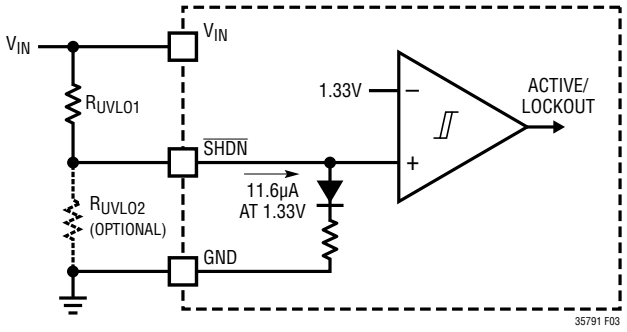


Figure 3. Configurable UVLO

The LT3579 also has internal UVLO circuitry that disables the chip when $V_{IN} < 2.3V$ (typical).

Soft-Start of Switch Current

The soft-start circuitry provides for a gradual ramp-up of the switch current (refer to *Commanded Switch Current vs. SS* in Typical Performance Characteristics). When the part is brought out of shutdown, the external SS capacitor is first discharged which resets the states of the logic circuits in the chip. Then an integrated 250k resistor pulls the SS pin to ~1.8V at a ramp rate set by the external capacitor connected to the pin. Once SS gets to 1.8V, the CLKOUT pin is enabled, and an internal regulator pulls the pin up quickly to ~2.1V. Typical values for the external soft-start capacitor range from 100nF to 1µF.

Soft-Start of External PMOS (if used)

The soft-start circuitry also gradually ramps up the GATE pin pull-down current which allows an external PMOS to slowly turn on (M1 in Block Diagram). The GATE pin current increases linearly with SS voltage, with a maximum current of 933µA when the SS voltage gets above 500mV. Note that if the GATE pin voltage is less than 2V for SS voltages exceeding 500mV, then the GATE pin impedance to ground is 2kΩ. The soft turn on of the external PMOS helps limit inrush current at start-up, making hot plugs of the LT3579 feasible and safe.

OPERATION

Sample Mode

Sample Mode is the mechanism used by the LT3579 to aid in the detection of output shorts. It refers to a state of the LT3579 where the master and slave power switches (Q1 and Q2) are turned on for a minimum period of time every clock cycle (or every few clock cycles in frequency foldback) in order to "sample" the inductor current. If the sampled current through Q1 exceeds the master switch current limit of 3.4A (minimum), the LT3579 triggers an overcurrent fault internally (see Operation-Fault section for details). Sample Mode exists when FB is out of regulation by more than 3.7% or 45mV < FB < 1.17V (typical). The LT3579's power switches are designed to handle a total peak current of 6A (minimum).

Frequency Foldback

The frequency foldback circuit reduces the switching frequency when 350mV < FB < 900mV (typical). This feature lowers the minimum duty cycle that the part can achieve, thus allowing better control of the inductor current during start-up. When the FB voltage is pulled outside of this range, the switching frequency returns to normal.

Note that the peak inductor current at start-up is a function of many variables including load profile, output capacitance, target V_{OUT}, V_{IN}, switching frequency, etc. **Test the application's performance at start-up to ensure that the peak inductor current does not exceed the minimum current limit.**

OPERATION – REGULATION

The following description of the LT3579's operation assumes the FB voltage is close enough to its regulation target so that the part is not in Sample Mode. Use the Block Diagram as a reference when stepping through the following description of the LT3579 operating in regulation. At the start of each oscillator cycle, the SR latch (SR1) is set, which turns on the power switches Q1 and Q2. The collector current through the master switch, Q1, is ~1.3 times the collector current through the slave switch, Q2, when the collectors of the two switches are tied together. Q1's emitter current flows through a current sense resistor (R_S) generating a voltage proportional to the total switch current. This voltage (amplified by A4) is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator A3. When the voltage on the positive input of A3 exceeds the voltage on the negative input, the SR latch is reset, turning off the master and slave power switches. The voltage on the negative input of A3 (V_C pin) is set by A1 (or A2), which is simply an amplified difference between the FB pin voltage and the reference voltage (1.215V if the LT3579 is configured as a boost converter, or 9mV if configured as an inverting converter). In this manner, the error amplifier sets the correct peak current level to maintain output regulation.

As long as the part is not in fault (see Operation – FAULT section) and the SS pin exceeds 1.8V, the LT3579 drives its CLKOUT pin at the frequency set by the RT pin or the SYNC pin. The CLKOUT pin can synchronize other compatible switching regulator ICs (including additional LT3579s) with the LT3579. Additionally, the duty cycle of CLKOUT varies linearly with the part's junction temperature and may be used as a temperature monitor. The CLKOUT signal on the LT3579-1 is ~180° out of phase with the internal oscillator and has a fixed duty cycle of ~50%.

OPERATION – FAULT

The LT3579's $\overline{FAULT}$ pin is an active low, bidirectional pin (refer to Block Diagram) that pulls low to indicate a fault. Each of the following events can trigger a fault in the LT3579:

A. FAULT1 Events:
   1. SW Overcurrent
      a. I_{SW1} > 3.4A (minimum)
      b. (I_{SW1} + I_{SW2}) > 6A (minimum)
   2. V_{IN} Voltage > 16.2V (minimum)
   3. SW1 Voltage and/or SW2 Voltage > 42V (minimum)
   4. Die Temperature > 165°C

B. FAULT2 Events:
   1. Pulling the $\overline{FAULT}$ pin low externally

OPERATION

When a fault is detected, in addition to the $\overline{\text{FAULT}}$ pin being pulled low internally, the LT3579 also disables its CLKOUT pin, turns off its power switches, and the GATE pin becomes high impedance (refer to the State Diagram). The external PMOS, M1, turns off when the gate of M1 is pulled up to its source by the external R_{GATE} resistor (see Block Diagram) With the external PMOS turned off, the power path from V_{IN} to V_{OUT} is cut off, protecting power components downstream.

At the same time, a timeout sequence commences where the SS pin is charged up to 1.8V (the SS pin will continue charging up to ~2.1V and be held there in the case of a FAULT1 event still existing), and then discharged to 50mV. This timeout period relieves the part, the PMOS, and other downstream power components from electrical and thermal stress for a minimum amount of time as set by the voltage ramp rate on the SS pin.

In the absence of faults, the $\overline{\text{FAULT}}$ pin is pulled high by the external $R_{\overline{\text{FAULT}}}$ resistor (typically 100k). Figure 4 and Figure 5 show the events that accompany the detection of an output short on the LT3579.

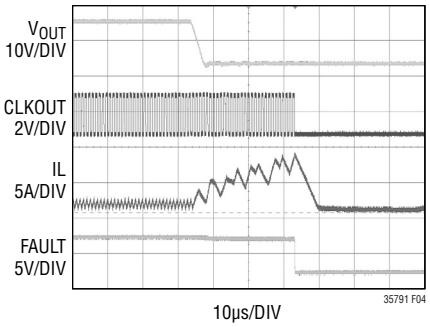


Figure 4. Output Short Circuit Protection of the LT3579

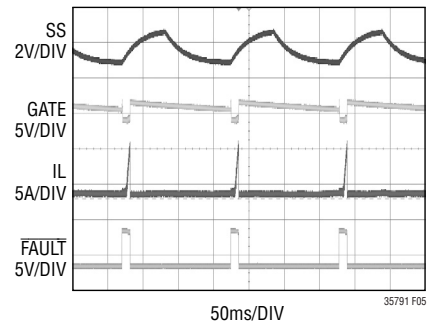


Figure 5. Continuous Output Short Showing $\overline{\text{FAULT}}$ Timeout Cycle

APPLICATIONS INFORMATION

BOOST CONVERTER COMPONENT SELECTION

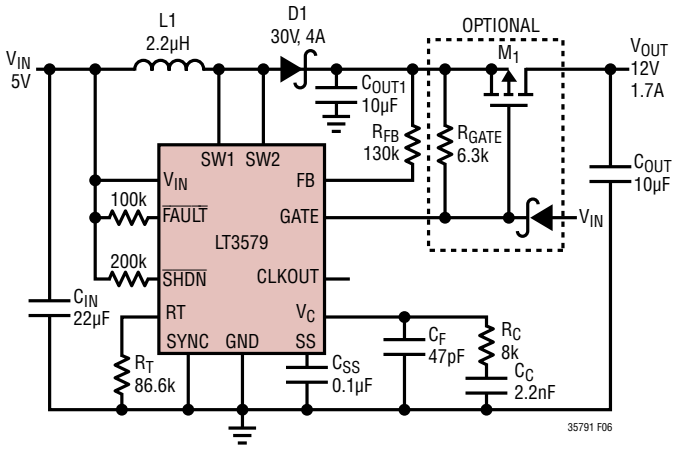


Figure 6. Boost Converter – The Component Values Given Are Typical Values for a 1MHz, 5V to 12V Boost

The LT3579 can be configured as a Boost converter as in Figure 6. This topology allows for positive output voltages that are higher than the input voltage. An external PMOS (optional) driven by the GATE pin of the LT3579 can achieve input or output disconnect during a $\overline{\text{FAULT}}$ event. A single feedback resistor sets the output voltage. For output voltages higher than 40V, see the Charge Pump topology in the Charge Pump Aided Regulators section.

Table 1 is a step-by-step set of equations to calculate component values for the LT3579 when operating as a Boost converter. Input parameters are input and output voltage, and switching frequency (V_{IN}, V_{OUT} and f_{OSC} respectively). Refer to the Appendix for further information on the design equations presented in Table 1.

Variable Definitions:

V_{IN} = Input Voltage
V_{OUT} = Output Voltage
DC = Power Switch Duty Cycle
f_{OSC} = Switching Frequency
I_{OUT} = Maximum Output Current
I_{RIPPLE} = Inductor Ripple Current
R_{DSON_PMOS} = R_{DSON} of External PMOS (set to 0 if not using PMOS)

Table 1. Boost Design Equations

	PARAMETERS/EQUATIONS
Step 1: Inputs	Pick V_{IN}, V_{OUT}, and f_{OSC} to calculate equations below.
Step 2: DC	$DC \cong \frac{V_{OUT} - V_{IN} + 0.5V}{V_{OUT} + 0.5V - 0.27V}$
Step 3: L1	$L_{TYP} = \frac{(V_{IN} - 0.27V) \bullet DC}{f_{OSC} \bullet 1.8A}$ (1) $L_{MIN} = \frac{(V_{IN} - 0.27V) \bullet (2 \bullet DC - 1)}{4A \bullet f_{OSC} \bullet (1 - DC)}$ (2) $L_{MAX} = \frac{(V_{IN} - 0.27V) \bullet DC}{f_{OSC} \bullet 0.5A}$ (3) • Solve equations 1, 2, and 3 for a range of L1 values. • The minimum of the L1 value range is the higher of L_{TYP} and L_{MIN}. • The maximum of the L1 value range is L_{MAX}.
Step 4: I_{RIPPLE}	$I_{RIPPLE} = \frac{(V_{IN} - 0.27V) \bullet DC}{f_{OSC} \bullet L1}$
Step 5: I_{OUT}	$I_{OUT} = \left(6A - \frac{I_{RIPPLE}}{2}\right) \bullet (1 - DC)$
Step 6: D1	$V_R > V_{OUT}$; $I_{AVG} > I_{OUT}$
Step 7: C_{OUT}, C_{OUT1}	$C_{OUT} = C_{OUT1} = \frac{I_{OUT} \bullet DC}{f_{OSC} \bullet (0.01 \bullet V_{OUT} - 0.5 \bullet I_{OUT} \bullet R_{DSON\_PMOS})}$
Step 8: C_{IN}	$C_{IN} = C_{PWR} + C_{VIN}$ $C_{IN} = \frac{I_{RIPPLE}}{8 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}} + \frac{6A \bullet DC}{40 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}}$
Step 9: R_{FB}	$R_{FB} = \frac{V_{OUT} - 1.215V}{83.3\mu A}$
Step 10: R_T	$R_T = \frac{87.6}{f_{OSC}} - 1$; f_{OSC} in MHz and R_T in kΩ
Step 11: PMOS	Only needed for input or output disconnect. See PMOS Selection in the Appendix for information on sizing the PMOS and the biasing resistor, R_{GATE}.

Note: The maximum design target for peak switch current is 6A and is used in this table. The final values for C_{OUT} and C_{IN} may deviate from the above equations in order to obtain desired load transient performance for a particular application.

APPLICATIONS INFORMATION

SEPIC CONVERTER COMPONENT SELECTION – COUPLED OR UNCOUPLED INDUCTORS

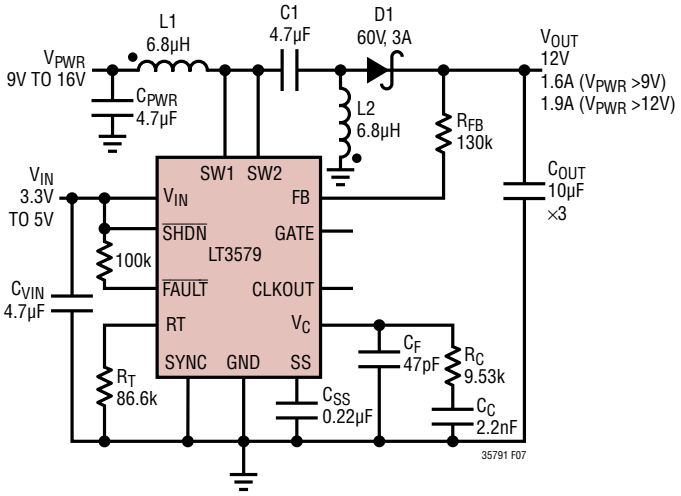


Figure 7. SEPIC Converter – The Component Values Given Are Typical Values for a 1MHz, 9V–16V to 12V SEPIC Topology Using Coupled Inductors

The LT3579 can also be configured as a SEPIC as in Figure 7. This topology allows for positive output voltages that are lower, equal, or higher than the input voltage. Output disconnect is inherently built into the SEPIC topology, meaning no DC path exists between the input and output due to capacitor C1. This implies that a PMOS controlled by the GATE pin is not required in the power path.

Table 2 is a step-by-step set of equations to calculate component values for the LT3579 when operating as a SEPIC converter using coupled inductors. Input parameters are input and output voltage, and switching frequency (V_{IN}, V_{OUT} and f_{OSC} respectively). Refer to the Appendix for further information on the design equations presented in Table 2.

Variable Definitions:

V_{IN} = Input Voltage
V_{OUT} = Output Voltage
DC = Power Switch Duty Cycle
f_{OSC} = Switching Frequency
I_{OUT} = Maximum Output Current
I_{RIPPLE} = Inductor Ripple Current

Table 2. SEPIC Design Equations

	PARAMETERS/EQUATIONS
Step 1: Inputs	Pick V_{IN}, V_{OUT}, and f_{OSC} to calculate equations below.
Step 2: DC	$DC \cong \frac{V_{OUT} + 0.5V}{V_{IN} + V_{OUT} + 0.5V - 0.27V}$
Step 3: L	$L_{TYP} = \frac{(V_{IN} - 0.27V) \bullet DC}{f_{OSC} \bullet 1.8A}$ (1) $L_{MIN} = \frac{(V_{IN} - 0.27V) \bullet (2 \bullet DC - 1)}{4A \bullet f_{OSC} \bullet (1 - DC)}$ (2) $L_{MAX} = \frac{(V_{IN} - 0.27V) \bullet DC}{f_{OSC} \bullet 0.5A}$ (3) • Solve equations 1, 2, and 3 for a range of L values. • The minimum of the L value range is the higher of L_{TYP} and L_{MIN}. • The maximum of the L value range is L_{MAX}. • L = L1 = L2 for coupled inductors. • L = L1‖L2 for uncoupled inductors.
Step 4: I_{RIPPLE}	$I_{RIPPLE} = \frac{(V_{IN} - 0.27V) \bullet DC}{f_{OSC} \bullet L}$
Step 5: I_{OUT}	$I_{OUT} = \left(6A - \frac{I_{RIPPLE}}{2}\right) \bullet (1 - DC)$
Step 6: D1	$V_R > V_{IN} + V_{OUT}$; $I_{AVG} > I_{OUT}$
Step 7: C1	4.7µF (typical) ; $V_{RATING} > V_{IN}$
Step 8: C_{OUT}	$C_{OUT} = \frac{I_{OUT} \bullet DC}{f_{OSC} \bullet 0.005 \bullet V_{OUT}}$
Step 9: C_{PWR}	$C_{PWR} = \frac{I_{RIPPLE}}{8 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}}$
Step 10: C_{VIN}	$C_{VIN} = \frac{6A \bullet DC}{40 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}}$
Step 11: R_{FB}	$R_{FB} = \frac{V_{OUT} - 1.215V}{83.3\mu A}$
Step 12: R_T	$R_T = \frac{87.6}{f_{OSC}} - 1$; f_{OSC} in MHz and R_T in kΩ

Note: The maximum design target for peak switch current is 6A and is used in this table. The final values for C_{OUT}, C_{PWR}, and C_{VIN} may deviate from the above equations in order to obtain desired load transient performance for a particular application.

APPLICATIONS INFORMATION

DUAL INDUCTOR INVERTING CONVERTER COMPONENT SELECTION – COUPLED OR UNCOUPLED INDUCTORS

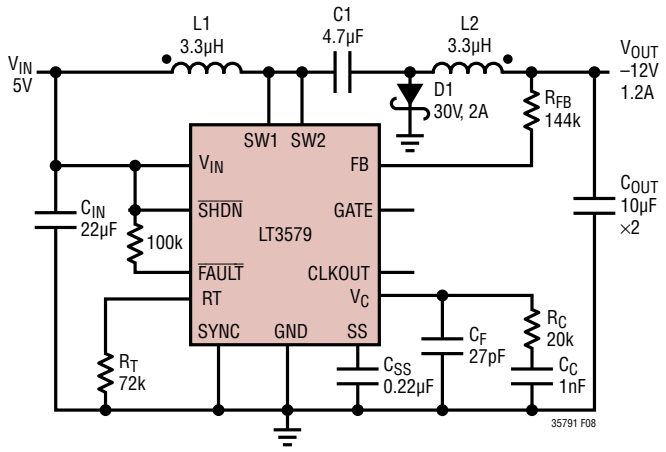


Figure 8. Dual Inductor Inverting Converter – The Component Values Given Are Typical Values for a 1.2MHz, 5V to –12V Inverting Topology Using Coupled Inductors

Due to its unique FB pin, the LT3579 can work in a Dual Inductor Inverting configuration as in Figure 8. Changing the connections of L2 and the Schottky diode in the SEPIC topology, results in generating negative output voltages. This solution results in very low output voltage ripple due to inductor L2 in series with the output. Output disconnect is inherently built into this topology due to the capacitor C1.

Table 3 is a step-by-step set of equations to calculate component values for the LT3579 when operating as a Dual Inductor Inverting converter using coupled inductors. Input parameters are input and output voltage, and switching frequency (V_{IN}, V_{OUT} and f_{OSC} respectively). Refer to the Appendix for further information on the design equations presented in Table 3.

Variable Definitions:

V_{IN} = Input Voltage
V_{OUT} = Output Voltage
DC = Power Switch Duty Cycle
f_{OSC} = Switching Frequency
I_{OUT} = Maximum Output Current
I_{RIPPLE} = Inductor Ripple Current

Table 3. Dual Inductor Inverting Design Equations

	PARAMETERS/EQUATIONS
Step 1: Inputs	Pick V_{IN}, V_{OUT}, and f_{OSC} to calculate equations below.
Step 2: DC	$DC \cong \frac{\lvert V_{OUT}\rvert + 0.5V}{V_{IN} + \lvert V_{OUT}\rvert + 0.5V - 0.27V}$
Step 3: L	$L_{TYP} = \frac{(V_{IN} - 0.27V) \bullet DC}{f_{OSC} \bullet 1.8A}$ (1) $L_{MIN} = \frac{(V_{IN} - 0.27V) \bullet (2 \bullet DC - 1)}{4A \bullet f_{OSC} \bullet (1 - DC)}$ (2) $L_{MAX} = \frac{(V_{IN} - 0.27V) \bullet DC}{f_{OSC} \bullet 0.5A}$ (3) • Solve equations 1, 2, and 3 for a range of L values. • The minimum of the L value range is the higher of L_{TYP} and L_{MIN}. • The maximum of the L value range is L_{MAX}. • L = L1 = L2 for coupled inductors. • L = L1‖L2 for uncoupled inductors.
Step 4: I_{RIPPLE}	$I_{RIPPLE} = \frac{(V_{IN} - 0.27V) \bullet DC}{f_{OSC} \bullet L}$
Step 5: I_{OUT}	$I_{OUT} = \left(6A - \frac{I_{RIPPLE}}{2}\right) \bullet (1 - DC)$
Step 6: D1	$V_R > V_{IN} + \lvert V_{OUT}\rvert ; I_{AVG} > I_{OUT}$
Step 7: C1	$4.7\mu F$ (typical) ; $V_{RATING} > V_{IN} + \lvert V_{OUT}\rvert$
Step 8: C_{OUT}	$C_{OUT} = \frac{I_{RIPPLE}}{8 \bullet f_{OSC} \bullet 0.005 \bullet \lvert V_{OUT}\rvert}$
Step 9: C_{IN}	$C_{IN} = C_{PWR} + C_{VIN}$ $C_{IN} = \frac{I_{RIPPLE}}{8 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}} + \frac{6A \bullet DC}{40 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}}$
Step 10: R_{FB}	$R_{FB} = \frac{\lvert V_{OUT}\rvert + 9mV}{83.3\mu A}$
Step 11: R_T	$R_T = \frac{87.6}{f_{OSC}} - 1$; f_{OSC} in MHz and R_T in kΩ

Note: The maximum design target for peak switch current is 6A and is used in this table. The final values for C_{OUT} and C_{IN} may deviate from the above equations in order to obtain desired load transient performance for a particular application.

APPLICATIONS INFORMATION

LAYOUT GUIDELINES FOR BOOST, SEPIC, AND DUAL INDUCTOR INVERTING TOPOLOGIES

General Layout Guidelines

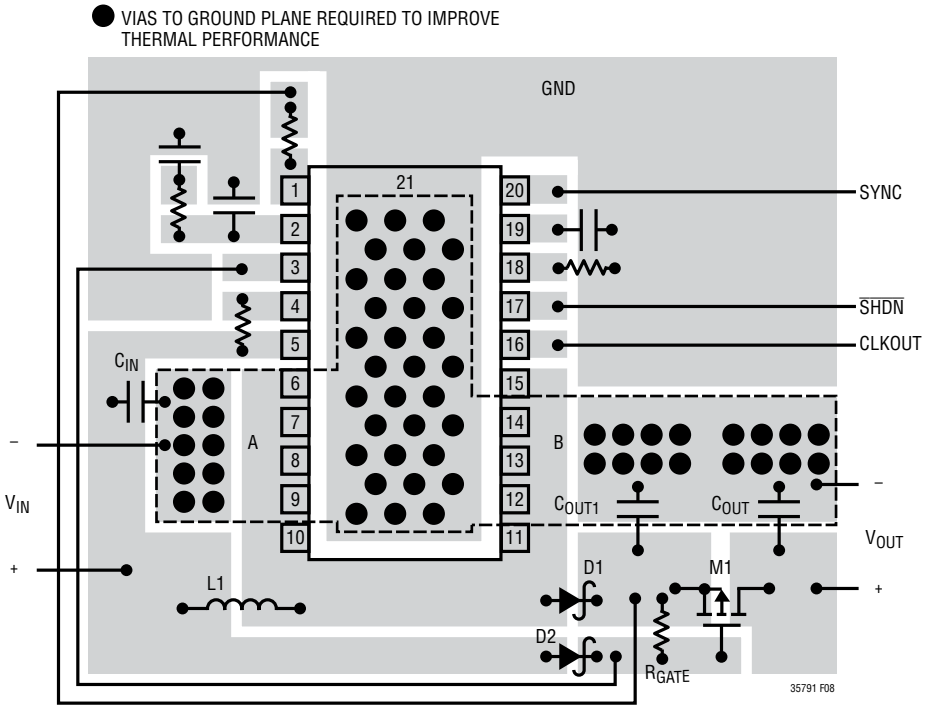
- To optimize thermal performance, solder the exposed ground pad of the LT3579 to the ground plane with multiple vias around the pad connecting to additional ground planes.
- A ground plane should be used under the switcher circuitry to prevent interplane coupling and overall noise.
- High speed switching path (see specific topology below for more information) must be kept as short as possible.
- The V_C, FB, and RT components should be placed as close to the LT3579 as possible, while being as far away as practically possible from the switch node. The ground for these components should be separated from the switch current path.
- Place the bypass capacitor for the V_{IN} pin (C_{VIN}) as close as possible to the LT3579.
- Place the bypass capacitor for the inductor (C_{PWR}) as close as possible to the inductor.
- Bypass capacitors, C_{PWR} and C_{VIN}, may be combined into a single bypass capacitor, C_{IN}, if the input side of the inductor can be close to the V_{IN} pin of the LT3579.
- The load should connect directly to the positive and negative terminals of the output capacitor for best load regulation.

Boost Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing switch, diode D1, output capacitor C_{OUT}, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

SEPIC Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing switch, flying capacitor C1, diode D1, output capacitor C_{OUT}, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.



A– RETURN C_{IN} GROUND DIRECTLY TO LT3579 EXPOSED PAD PIN 21. IT IS ADVISED TO NOT COMBINE C_{IN} GROUND WITH GND EXCEPT AT THE EXPOSED PAD.
B– RETURN C_{OUT} AND C_{OUT1} GROUND DIRECTLY TO LT3579 EXPOSED PAD PIN 21. IT IS ADVISED TO NOT COMBINE C_{OUT} AND C_{OUT1} GROUND WITH GND EXCEPT AT THE EXPOSED PAD.

Figure 9. Suggested Component Placement for Boost Topology in FE20 Package

APPLICATIONS INFORMATION

Inverting Topology Specific Layout Guidelines

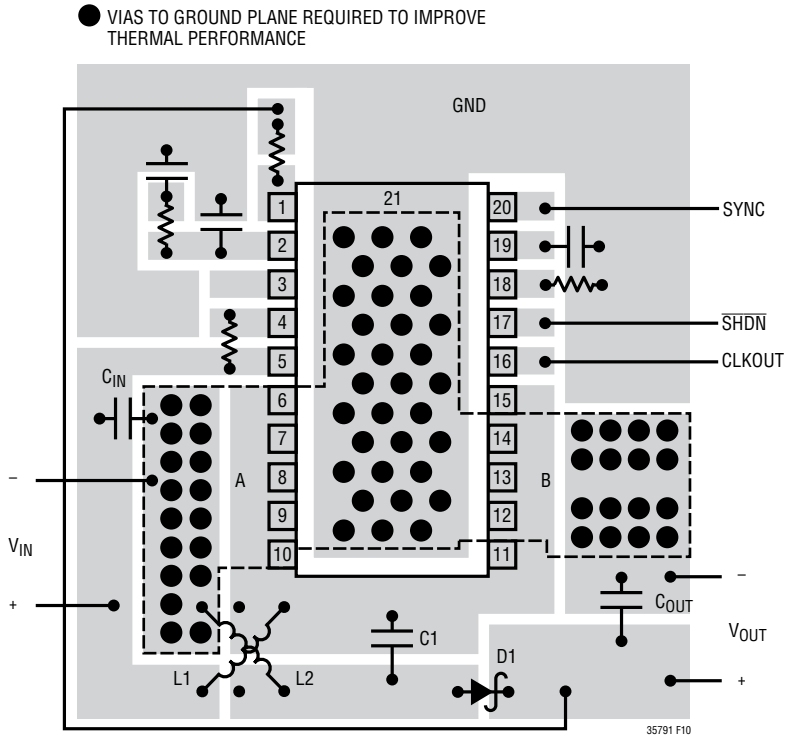
- Keep ground return path from the cathode of D1 (to chip) separated from output capacitor C_{OUT}'s ground return path (to chip) in order to minimize switching noise coupling into the output. Notice the separate ground return for D1's cathode in Figure 11.
- Keep length of loop (high speed switching path) governing switch, flying capacitor C1, diode D1, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

THERMAL CONSIDERATIONS

For the LT3579 to deliver its full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible.

Power & Thermal Calculations

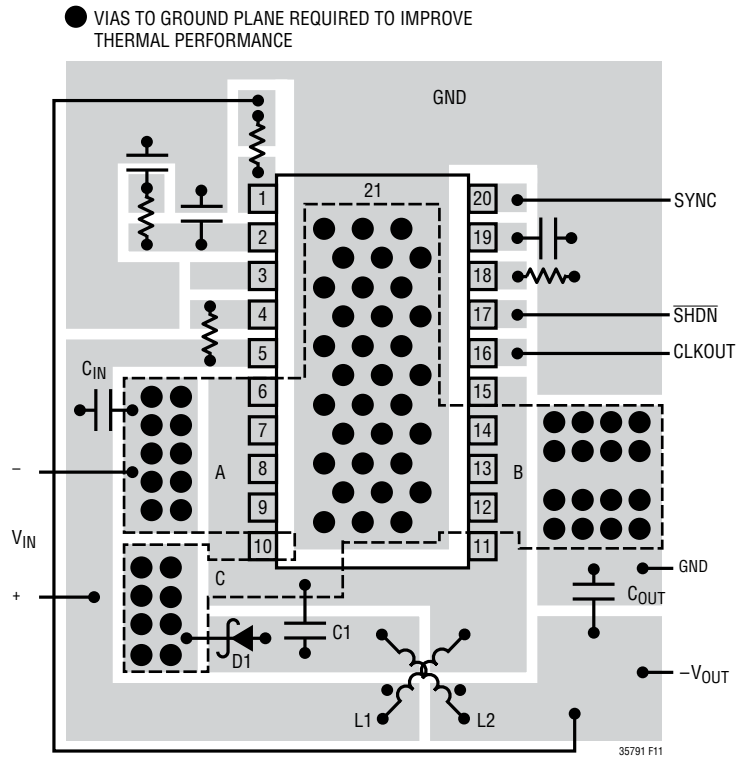
Power dissipation in the LT3579 chip comes from four primary sources: switch I^2R loss, NPN base drive loss (AC), NPN base drive loss (DC), and additional V_{IN} pin current. These formulas assume continuous mode operation, so they should not be used for calculating thermal losses or efficiency in discontinuous mode or at light load currents.



A– RETURN C_{IN} AND L2 GROUND DIRECTLY TO LT3579 EXPOSED PAD PIN 21. IT IS ADVISED TO NOT COMBINE C_{IN} AND L2 GROUND WITH GND EXCEPT AT THE EXPOSED PAD.
B– RETURN C_{OUT} GROUND DIRECTLY TO LT3579 EXPOSED PAD PIN 21. IT IS ADVISED TO NOT COMBINE C_{OUT} GROUND WITH GND EXCEPT AT THE EXPOSED PAD.
L1, L2 –MOST COUPLED INDUCTOR MANUFACTURERS USE CROSS PINOUT FOR IMPROVED PERFORMANCE.

Figure 10. Suggested Component Placement for SEPIC Topology in FE20 Package

APPLICATIONS INFORMATION



A– RETURN C_{IN} GROUND DIRECTLY TO LT3579 EXPOSED PAD PIN 21. IT IS ADVISED TO NOT COMBINE C_{IN} GROUND WITH GND EXCEPT AT THE EXPOSED PAD.
B– RETURN C_{OUT} GROUND DIRECTLY TO LT3579 EXPOSED PAD PIN 21. IT IS ADVISED TO NOT COMBINE C_{OUT} GROUND WITH GND EXCEPT AT THE EXPOSED PAD.
C– RETURN D1 GROUND DIRECTLY TO LT3579 EXPOSED PAD PIN 21. IT IS ADVISED TO NOT COMBINE D1 GROUND WITH GND EXCEPT AT THE EXPOSED PAD.
L1, L2 – MOST COUPLED INDUCTOR MANUFACTURERS USE CROSS PINOUT FOR IMPROVED PERFORMANCE.

Figure 11. Suggested Component Placement for Inverting Topology in FE20 Package. Note Separate Ground Path for D1's Cathode

APPLICATIONS INFORMATION

The following example calculates the power dissipation in the LT3579 for a particular boost application: (V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 1.5A, f_{OSC} = 1MHz, V_D = 0.5V, V_{CESAT} = 0.185V).

To calculate die junction temperature, use the appropriate thermal resistance number and add in worst-case ambient temperature:

$$T_J = T_A + \theta_{JA} \bullet P_{TOTAL}$$

where T_J=Die Junction Temperature, T_A=Ambient Temperature, P_{TOTAL} is the final result from the calculations shown in Table 4, and θ_{JA} is the thermal resistance from the silicon junction to the ambient air.

Table 4. Boost Power Calculations Example with V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 1.5A, f_{OSC} = 1MHz, V_D = 0.5V, V_{CESAT} = 0.185V

DEFINITION OF VARIABLES	EQUATIONS	DESIGN EXAMPLE	VALUE
DC = Switch Duty Cycle	$DC = \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D - V_{CESAT}}$	$DC = \frac{12V - 5V + 0.5V}{12V + 0.5V - .185V}$	DC = 60.9%
I_{IN} = Average Input Current η = Power Conversion Efficiency (typically 90% at high currents)	$I_{IN} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta}$	$I_{IN} = \frac{12V \bullet 1.5A}{5V \bullet 0.9}$	I_{IN} = 4A
P_{SW} = Switch I^2R Loss R_{SW} = Switch Resistance (typically 45mΩ combined SW1 and SW2)	$P_{SW} = DC \bullet I_{IN}^2 \bullet R_{SW}$	$P_{SW} = 0.609 \bullet (4A)^2 \bullet 45m\Omega$	P_{SW} = 438mW
P_{BAC} = Base Drive Loss (AC)	$P_{BAC} = 13ns \bullet I_{IN} \bullet V_{OUT} \bullet f_{OSC}$	$P_{BAC} = 13ns \bullet 4A \bullet 12V \bullet 1MHz$	P_{BAC} = 624mW
P_{BDC} = Base Drive Loss (DC)	$P_{BDC} = \frac{V_{IN} \bullet I_{IN} \bullet DC}{40}$	$P_{BDC} = \frac{5V \bullet 4A \bullet 0.609}{40}$	P_{BDC} = 305mW
P_{INP} = Input Power Loss	$P_{INP} = 14mA \bullet V_{IN}$	$P_{INP} = 14mA \bullet 5V$	P_{INP} = 70mW
			P_{TOTAL} = 1.437W

APPLICATIONS INFORMATION

The published (http://www.linear.com/designtools/packaging/Linear_Technology_Thermal_Resistance_Table.pdf) θ_{JA} value is 38°C/W for the TSSOP Exposed Pad package and 34°C/W for the 4mm × 5mm QFN package. In practice, lower θ_{JA} values are realizable if board layout is performed with appropriate grounding (accounting for heat sinking properties of the board) and other considerations listed in the Layout Guidelines section. For instance, a θ_{JA} value of ~22°C/W was consistently achieved for both TSSOP and QFN packages of the LT3579 (at V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 1.7A, f_{OSC} = 1MHz) when board layout was optimized as per the suggestions in the Layout Guidelines section.

Junction Temperature Measurement

The duty cycle of the CLKOUT signal on the LT3579 is linearly proportional to die junction temperature, T_J (the CLKOUT duty cycle on the LT3579-1 is fixed at ~50%). To get an accurate reading, measure the duty cycle of the CLKOUT signal and use the following equation to approximate the junction temperature:

$$T_J = \frac{DC_{CLKOUT} - 35\%}{0.3\%}$$

where DC_{CLKOUT} is the CLKOUT duty cycle in % and T_J is the die junction temperature in °C. Although the absolute die temperature can deviate from the above equation by ±15°C, the relationship between change in CLKOUT duty cycle and change in die temperature is well defined. A 3% increase in CLKOUT duty cycle corresponds to ~10°C increase in die temperature:

Note that the CLKOUT pin is only meant to drive capacitive loads up to 50pF.

Thermal Lockout

A fault condition occurs when the die temperature exceeds ~165°C (see Operation – FAULT Section), and the part goes into thermal lockout. The fault condition ceases when the die temperature drops by ~5°C (nominal).

SWITCHING FREQUENCY

There are several considerations in selecting the operating frequency of the converter. The first is staying clear of sensitive frequency bands, which cannot tolerate any spectral noise. For example, in products incorporating RF communications, the 455kHz IF frequency is sensitive to any noise, therefore switching above 600kHz is desired. Some communications have sensitivity to 1.1MHz and in that case a 1.5MHz switching converter frequency may be employed. The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter capacitors go down in value and size. The trade-off is efficiency, since the switching losses due to NPN base charge (see Thermal Considerations), Schottky diode charge, and other capacitive loss terms increase proportionally with frequency.

Oscillator Timing Resistor (R_T)

The operating frequency of the LT3579 can be set by the internal free-running oscillator. When the SYNC pin is driven low (< 0.4V), the frequency of operation is set by a resistor from the RT pin to ground. An internally trimmed timing capacitor resides inside the IC. The oscillator frequency is calculated using the following formula:

$$f_{OSC} = \frac{87.6}{R_T + 1}$$

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where f_{OSC} is in MHz and R_T is in kΩ. Conversely, R_T (in kΩ) can be calculated from the desired frequency (in MHz) using:

$$R_T = \frac{87.6}{f_{OSC}} - 1$$

Clock Synchronization

An external source can set the operating frequency of the LT3579 by providing a digital clock signal into the SYNC pin (R_T resistor still required). The LT3579 will operate at the SYNC clock frequency. The LT3579 will revert to its internal free-running oscillator clock when the SYNC pin is driven below 0.4V for a few free-running clock periods.

Driving SYNC high for an extended period of time effectively stops the operating clock and prevents latch SR1 from becoming set (see Block Diagram). As a result, the switching operation of the LT3579 will stop and the CLKOUT pin will be held at ground.

The duty cycle of the SYNC signal must be between 20% and 80% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

1. SYNC may not toggle outside the frequency range of 200kHz-2.5MHz unless it is stopped below 0.4V to enable the free-running oscillator.
2. The SYNC frequency can always be higher than the free-running oscillator frequency (as set by the R_T resistor), f_{OSC}, but should not be less than 25% below f_{OSC}.

CLOCK SYNCHRONIZATION OF ADDITIONAL REGULATORS

The CLKOUT pin of the LT3579 can synchronize additional switching regulators and/or additional LT3579s as shown in Figure 12.

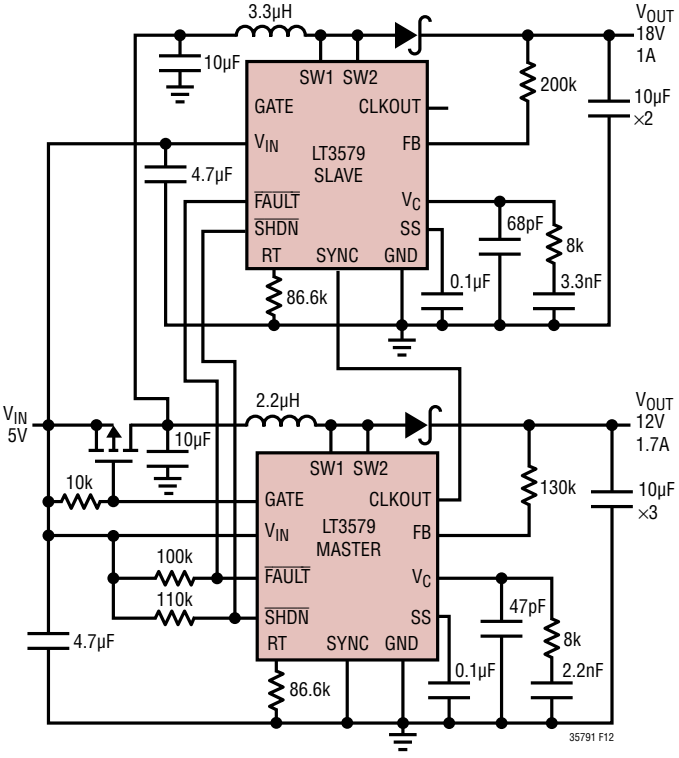

Figure 12. Synchronize Multiple LT3579s. The External PMOS Disconnects the Input from Both Power Paths During FAULT Events

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The frequency of the master LT3579 is set by the external R_T resistor. The SYNC pin of the slave LT3579 is driven by the CLKOUT pin of the master LT3579. Note that the RT pin of the slave LT3579 must have a resistor tied to ground. It takes a few clock cycles for the CLKOUT signal to begin oscillating, and it's preferable for all LT3579s to have the same internal free-running frequency. Therefore, in general, use the same value R_T resistor for all of the synchronized LT3579s.

Also, the $\overline{FAULT}$ pins can be tied together so that a fault condition from one LT3579 causes all of the LT3579s to enter fault, until the fault condition disappears.

2-Phase Converters using LT3579-1

The CLKOUT pin on the LT3579-1 is ~180° out of phase with the internal oscillator, which allows two LT3579-1s to operate in parallel for a high current, high power output. The advantage of multiphase converters is that the ripple current flowing into the output node is divided by the number of phases or ICs used to generate the output voltage. The V_{IN}, $\overline{SHDN}$, $\overline{FAULT}$, FB, and V_C pins of all the LT3579-1s should be connected together. Figure 13 shows a typical application of a 2-phase 12V to 24V boost with output disconnect.

Use the following equations to calculate the FB resistor for 2-phase converters:

$$R_{FB} = \left(\frac{V_{OUT} - 1.215V}{2 \bullet 83.3\mu A}\right)$$; Boost or SEPIC Multiphase Converter

$$R_{FB} = \left(\frac{|V_{OUT}| + 9mV}{2 \bullet 83.3\mu A}\right)$$; Inverting Multiphase Converter

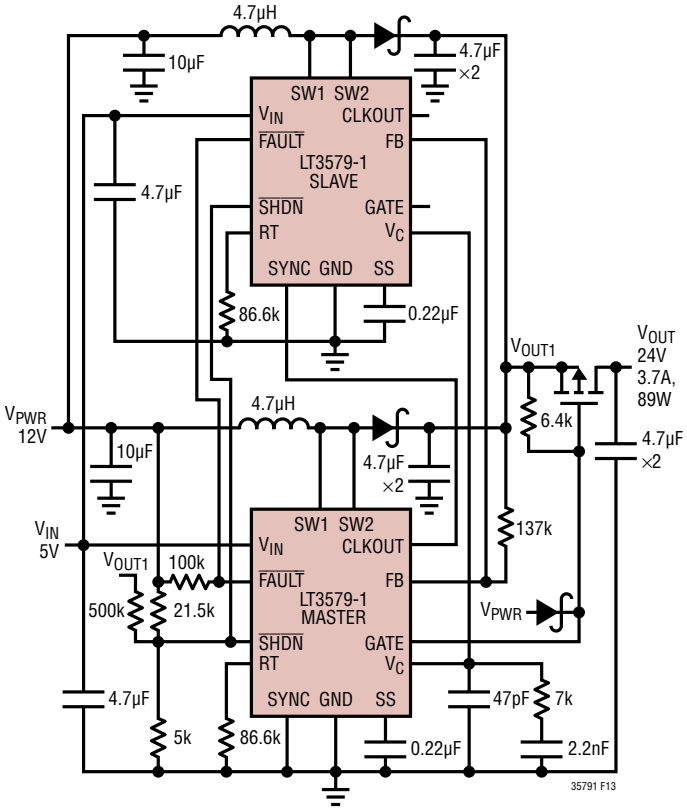

Figure 13. 2-Phase Converters Using LT3579-1

Note that the CLKOUT pin on the LT3579-1 runs at a fixed duty cycle of ~50%. If monitoring the die temperature is desired, the slave IC can be a LT3579.

It is possible to use the LT3579-1 in a multiphase converter of more than 2 phases. Consult the LTC Applications Engineering Department for more information.

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CHARGE PUMP AIDED REGULATORS

Designing charge pumps with the LT3579 can offer efficient solutions with fewer components than traditional circuits because of the master/slave switch configuration on the IC. The current in the master switch (SW1) is sensed by the current comparator (A4 in Block Diagram), but the current in the slave switch (SW2) is not. Note that the slave switch, SW2, operates in phase with SW1. This method of operation by the master/slave switches can offer the following benefits to charge pump designs:

- The slave switch, by not performing a current sense operation like the master switch, can sustain fairly large current spikes when the flying capacitors charge up. Since this current spike flows through SW2, it does not affect the operation of the current comparator (A4 in Block Diagram).
- The master switch, immune from the capacitor current spike, can sense the inductor current more accurately.
- Since the slave switch can sustain large current spikes, the diodes that feed current into the flying capacitors do not need current limiting resistors, leading to efficiency and thermal improvements.

High V_{OUT} Charge Pump Topology

The LT3579 can be used in a charge-pump topology (refer to Figure 16), multiplying the output of an inductive boost converter. The master switch (SW1) can be used to drive the inductive boost converter, while the slave switch (SW2) can be used to drive one or more charge pump stages. This topology is useful for high voltage applications including VFD Bias Supplies.

Single Inductor Inverting Topology

If there is a need to use just 1 inductor to generate a negative output voltage whose magnitude is greater than V_{IN}, the Single Inductor Inverting topology (shown in Figure 15) can be used. Since the master and slave switches are isolated by an external Schottky diode, the current spike through C1 will flow through the slave switch, thereby preventing the current comparator (A4 in Block Diagram) from falsely tripping. Output disconnect is inherently built into the single inductor topology.

HOT PLUG

The high inrush current associated with hot-plugging V_{IN} can be largely rejected with the use of an external PMOS. A simple hot-plug controller can be designed by connecting an external PMOS in series with V_{IN}, with the gate of the PMOS being driven by the GATE pin of the LT3579. Since the GATE pin pull-down current is linearly proportional to the SS voltage, and the SS charge up time is relatively slow, the GATE pin pull-down current will increase gradually, thereby turning on the external PMOS slowly. Controlled in this manner, the PMOS acts as an input current limiter when V_{IN} hot-plugs or ramps up sharply.

Likewise, when the PMOS is connected in series with the output, inrush currents into the output capacitor can be limited during a hot-plug event. To illustrate this, the circuit in Figure 6 was re-configured by adding a large 1500µF capacitor to the output. An 18Ω resistive load was used and a 2.2µF capacitor was placed on SS. Figure 14 shows the result of hot-plugging this re-configured circuit. The inductor current is well behaved and V_{OUT} comes up once V_{IN} settles out.

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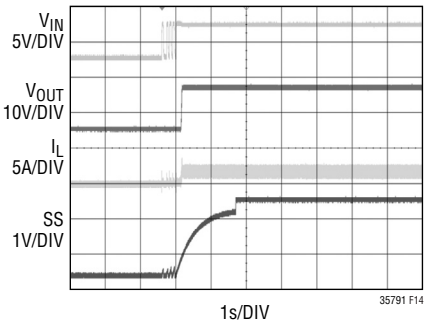

Figure 14. V_{IN} Hot-Plug Control. Inrush Current is Well Controlled

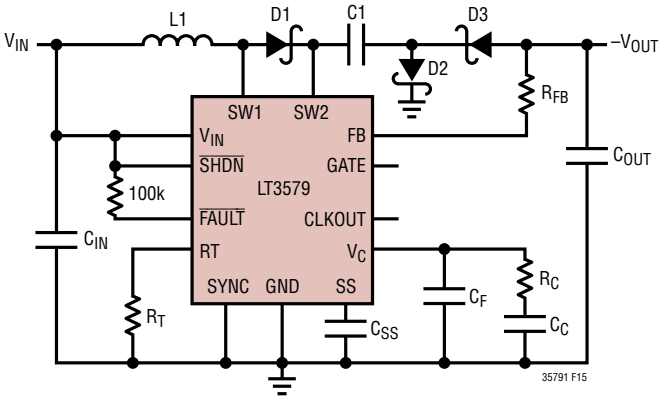

Figure 15. Single Inductor Inverting Topology

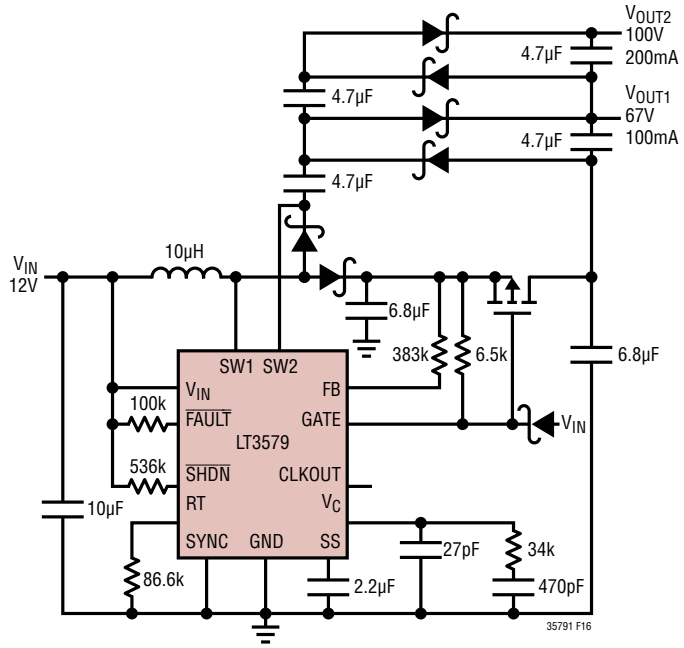

Figure 16. High V_{OUT} Charge Pump Topology

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SETTING THE OUTPUT VOLTAGE

The output voltage is set by connecting a resistor (R_{FB}) from V_{OUT} to the FB pin. R_{FB} is determined from the following equation:

$$R_{FB} = \frac{|V_{OUT} - V_{FB}|}{83.3\mu A}$$

where V_{FB} is 1.215V (typical) for non-inverting topologies (i.e. boost and SEPIC regulators) and 9mV (typical) for inverting topologies (see Electrical Characteristics).

POWER SWITCH DUTY CYCLE

In order to maintain loop stability and deliver adequate current to the load, the power NPNs (Q1 and Q2 in the Block Diagram) cannot remain "on" for 100% of each clock cycle. The maximum allowable duty cycle is given by:

$$DC_{MAX} = \frac{(T_P - MinOffTime)}{T_P} \bullet 100\%$$

where T_P is the clock period and MinOffTime (found in the Electrical Characteristics) is typically 45nS.

Conversely, the power NPNs (Q1 and Q2 in the Block Diagram) cannot remain "off" for 100% of each clock cycle, and will turn on for a minimum time (MinOnTime) when in regulation. This MinOnTime governs the minimum allowable duty cycle given by:

$$DC_{MIN} = \frac{(MinOnTime)}{T_P} \bullet 100\%$$

where T_P is the clock period and MinOnTime (found in the Electrical Characteristics) is typically 55nS.

The application should be designed such that the operating duty cycle is between DC_{MIN} and DC_{MAX}.

Duty cycle equations for several common topologies are given below where V_D is the diode forward voltage drop and V_{CESAT} is typically 250mV at 5.5A for a combined SW1 and SW2 current.

For the boost topology (see Figure 6):

$$DC_{BOOST} \cong \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D - V_{CESAT}}$$

For the SEPIC or Dual Inductor Inverting topology (see Figure 7 and Figure 8):

$$DC_{SEPIC\_\&\_INVERT} \cong \frac{V_D + |V_{OUT}|}{V_{IN} + |V_D| + V_{OUT} - V_{CESAT}}$$

For the Single Inductor Inverting topology (see Figure 14):

$$DC_{SI\_INVERT} \cong \frac{|V_{OUT}| - V_{IN} + V_{CESAT} + 3 \bullet V_D}{|V_{OUT}| + 3 \bullet V_D}$$

The LT3579 can be used in configurations where the duty cycle is higher than DC_{MAX}, but it must be operated in the discontinuous conduction mode so that the effective duty cycle is reduced.

INDUCTOR SELECTION

The high frequency operation of the LT3579 allows for the use of small surface mount inductors. For high efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. Also to improve efficiency, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper-wire resistance) to reduce I^2R losses, and must be able to handle the peak inductor current without saturating. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology where each inductor only carries one half of the total switch current. Multilayer chokes or chip inductors usually do not have enough core volume to support peak inductor currents in the 4A to 7A range. To minimize radiated noise, use a toroidal or shielded inductor. See Table 5 for a list of inductor manufacturers.

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Table 5. Inductor Manufacturers

Vishay	IHLP-2020BZ-01 and IHLP-2525CZ-01 Series	www.vishay.com
Coilcraft	XLP, MLC and MSS Series	www.coilcraft.com
Cooper Bussmann	DRQ125 and DRQ127 Series	www.cooperbussmann.com
Sumida	CDRH series	www.sumida.com
TDK	RLF and SLF series	www.tdk.com
Würth	WE-PD, WE-PDF, WE-HC and WE-DD Series	www.we-online.com

Minimum Inductance

Although there can be a trade-off with efficiency, it is often desirable to minimize board space by choosing smaller inductors. When choosing an inductor, there are three conditions that limit the minimum inductance; (1) providing adequate load current, (2) avoidance of subharmonic oscillation, and (3) supplying a minimum ripple current to avoid false tripping of the current comparator.

Adequate Load Current

Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be provided to the load. In order to provide adequate load current, L should be at least:

$$L_{BOOST} > \frac{DC \bullet \left(V_{IN} - V_{CESAT}\right)}{2 \bullet f_{OSC} \bullet \left(I_{PK} - \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta}\right)}$$ Boost Topology

or

$$L_{DUAL} > \frac{DC \bullet \left(V_{IN} - V_{CESAT}\right)}{2 \bullet f_{OSC} \bullet \left(I_{PK} - \frac{|V_{OUT}| \bullet I_{OUT}}{V_{IN} \bullet \eta} - I_{OUT}\right)}$$ SEPIC or Inverting Topologies

where:

L_{BOOST} = L1 for Boost Topologies (see Figure 6)
L_{DUAL} = L1 = L2 for Coupled Dual Inductor Topologies (see Figure 7 and Figure 8)
L_{DUAL} = L1 || L2 for Uncoupled Dual Inductor Topologies (see Figure 7 and Figure 8)
DC = Switch Duty Cycle (see Power Switch Duty Cycle section in Appendix)
I_{PK} = Maximum Peak Switch Current; Should Not Exceed 6A for a Combined SW1 + SW2 Current or 3.4A of SW1 Current (see Electrical Characteristics section.)
η = Power Conversion Efficiency (typically 90% for Boost and 85% for Dual Inductor Topologies at high currents)
f_{OSC} = Switching Frequency
I_{OUT} = Maximum Output Current

Negative values of L_{BOOST} or L_{DUAL} indicate that the output load current, I_{OUT}, exceeds the switch current limit capability of the LT3579.

Avoiding Sub-Harmonic Oscillations

The LT3579's internal slope compensation circuit will prevent sub-harmonic oscillations that can occur when the duty cycle is greater than 50%, provided that the inductance exceeds a minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

$$L_{MIN} = \frac{\left(V_{IN} - V_{CESAT}\right) \bullet \left(2 \bullet DC - 1\right)}{4A \bullet f_{OSC} \bullet \left(1 - DC\right)}$$

where:

L_{MIN} = L1 for Boost Topologies (see Figure 6)
L_{MIN} = L1 = L2 for Coupled Dual Inductor Topologies (see Figure 7 and Figure 8)
L_{MIN} = L1 || L2 for Uncoupled Dual Inductor Topologies (see Figure 7 and Figure 8)

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Maximum Inductance

Excessive inductance can reduce ripple current to levels that are difficult for the current comparator (A4 in the Block Diagram) to cleanly discriminate, thus causing duty cycle jitter and/or poor regulation. The maximum inductance can be calculated by:

$$L_{MAX} = \frac{(V_{IN} - V_{CESAT}) \bullet DC}{f_{OSC} \bullet 0.5A}$$

where:

L_{MAX} = L1 for Boost Topologies (see Figure 6)
L_{MAX} = L1 = L2 for Coupled Dual Inductor Topologies (see Figure 7 and Figure 8)
L_{MAX} = L1 || L2 for Uncoupled Dual Inductor Topologies (see Figure 7 and Figure 8)

Inductor Current Rating

The inductor(s) must have a rating greater than its (their) peak operating current to prevent inductor saturation, which would result in catastrophic failure and efficiency losses. The maximum inductor current (considering start-up and steady-state conditions) is given by:

$$I_{L\_PEAK} = I_{LIM} + \frac{V_{IN} \bullet T_{MIN\_PROP}}{L}$$

where:

I_{L_PEAK} = Peak Inductor Current in L1 for a Boost Topology, or the sum of the Peak Inductor Currents in L1 and L2 for Dual Inductor Topologies.
I_{LIM} = For Hard-Saturation Inductors, 9.4A with SW1 and SW2 Tied Together, or 5.1A with just SW1 used. For Soft-Saturation Inductors, 6A with SW1 and SW2 Tied Together, or 3.4A with just SW1 used.
T_{MIN_PROP} = 100ns (Propagation Delay through the Current Feedback Loop).

Note that these equations offer conservative results for the required inductor current ratings. The current ratings could be lower for applications with light loads, provided the SS capacitor is sized appropriately to limit inductor currents at start-up.

DIODE SELECTION

Schottky diodes, with their low forward voltage drops and fast switching speeds, are recommended for use with the LT3579. Choose a Schottky with low parasitic capacitance to reduce reverse current spikes through the power switch of the LT3579. The Diodes Inc. MBRM360 is a very good choice with a 60V reverse voltage rating and an average forward current of 3A.

OUTPUT CAPACITOR SELECTION

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have an extremely low ESR and are available in very small packages. X5R or X7R type are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. A 22µF to 47µF output capacitor is sufficient for most applications, but systems with low output currents may need only 4.7µF to 22µF. Always use a capacitor with a sufficient voltage rating. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired output voltage. Tantalum polymer or OS-CON capacitors can be used, but it is likely that these capacitors will occupy more board area than a ceramic, and will have higher ESR with greater output ripple.

INPUT CAPACITOR SELECTION

Ceramic capacitors make a good choice for the input decoupling capacitor, C_{VIN}, which should be placed as close as possible to the V_{IN} pin of the LT3579. This ensures that the voltage seen at the V_{IN} pin of the LT3579 remains a nearly flat DC voltage. A 1µF to 4.7µF input capacitor is sufficient for most applications.

A ceramic bypass capacitor, C_{PWR}, should also be placed as close as possible to the input of the inductor. This ensures that the inductor ripple current is supplied from the bypass capacitor and provides a nearly flat DC voltage to the input of the voltage converter. A 4.7µF to 10µF input power capacitor is sufficient for most applications.

APPENDIX

Table 6 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers for detailed information on their entire selection of ceramic parts.

Table 6. Ceramic Capacitor Manufacturers

TDK	www.tdk.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com

PMOS SELECTION

An external PMOS, controlled by the LT3579's GATE pin, can be used to facilitate input or output disconnect. The GATE pin turns on the PMOS gradually during start-up (see Soft-Start of External PMOS in the Operation section), and turns the PMOS off when the LT3579 is in shutdown or in fault.

The use of the external PMOS, controlled by the GATE pin, is particularly beneficial when dealing with unintended output shorts in a boost regulator. In a conventional boost regulator, the inductor, Schottky diode, and power switches are susceptible to damage in the event of an output short to ground. Using an external PMOS in the boost regulator's power path (path from V_{IN} to V_{OUT}) controlled by the GATE pin, will serve to disconnect the input from the output when the output has a short to ground, thereby helping save the IC, and the other components in the power path from damage.

The PMOS chosen must be capable of handling the maximum input or output current depending on whether the PMOS is used at the input (see Figure 12) or the output (see Figure 13).

Ensure that the PMOS is biased with enough source to gate voltage (V_{SG}) to enhance the device into the triode mode of operation. The higher the V_{SG} voltage that biases the PMOS, the lower the R_{DSON} of the PMOS, thereby lowering power dissipation in the device during normal operation, as well as improving the efficiency of the application in which the PMOS is used. The following equations show the relationship between R_{GATE} (see Block Diagram) and the desired V_{SG} that the PMOS is biased with:

$$V_{SG} = \begin{cases} V_S \dfrac{R_{GATE}}{R_{GATE} + 2k\Omega} \text{ if } V_{GATE} < 2V \\ 933\mu A \bullet R_{GATE} \text{ if } V_{GATE} > 2V \end{cases}$$

When using a PMOS, it is advisable to configure the specific application for undervoltage lockout (see the Operation section). The goal is to have V_{IN} get to a certain minimum voltage where the PMOS has sufficient headroom to attain a high enough V_{SG}, which prevents it from entering the saturation mode of operation during start-up.

Figure 6 shows the PMOS connected in series with the output to act as an output disconnect during a fault condition. The Schottky diode from the V_{IN} pin to the GATE pin is optional and helps turn off the PMOS quicker in the event of hard shorts. The resistor from V_{IN} to the $\overline{SHDN}$ pin sets a UVLO of 4V for this application.

Connecting the PMOS in series with the output offers certain advantages over connecting it in series with the input:

- Since the load current is always less than the input current for a boost converter, the current rating of the PMOS goes down when connected in series with the output as opposed to the input.
- A PMOS in series with the output can be biased with a higher overdrive voltage than a PMOS used in series with the input, since $V_{OUT} > V_{IN}$. This higher overdrive results in a lower R_{DSON} for the PMOS, thereby improving the efficiency of the regulator.

In contrast, an input connected PMOS works as a simple hot-plug controller (covered in more detail in the Hot-Plug section). The input connected PMOS also functions as an inexpensive means of protecting against multiple output shorts in boost applications that synchronize the LT3579 with other compatible ICs (see Figure 12).

APPENDIX

Table 7 shows a list of several discrete PMOS manufacturers. Consult the manufacturers for detailed information on their entire selection of PMOS devices.

Table 7. Discrete PMOS Manufacturers

Vishay	www.vishay.com
Fairchild Semiconductor	www.fairchildsemi.com
Central Semiconductor	www.centralsemi.com

COMPENSATION – ADJUSTMENT

To compensate the feedback loop of the LT3579, a series resistor-capacitor network in parallel with an optional single capacitor must be connected from the V_C pin to GND. For most applications, choose a series capacitor in the range of 1nF to 10nF with 2.2nF being a good starting value. The optional parallel capacitor should range in value from 22pF to 180pF with 47pF being a good starting value. The compensation resistor, R_C, is usually in the range of 5k to 50k. A good technique to compensate a new application is to use a 100kΩ potentiometer in place of the series resistor R_C. With the series and parallel capacitors at 2.2nF and 47pF respectively, adjust the potentiometer while observing the transient response and the optimum value for R_C can be found. Figure 17a to Figure 17c illustrate this process for the circuit of Figure 20 with a load current stepped between 0.7A and 1.5A. Figure 17a shows the transient response with R_C equal to 1k. The phase margin is poor as evidenced by the excessive ringing in the output voltage and inductor current. In Figure 17b, the value of R_C is increased to 3.5k, which results in a more damped response. Figure 17c shows the results when R_C is increased further to 8k. The transient response is nicely damped and the compensation procedure is complete.

COMPENSATION – THEORY

Like all other current mode switching regulators, the LT3579 needs to be compensated for stable and efficient operation. Two feedback loops are used in the LT3579: a fast current loop which does not require compensation, and a slower voltage loop which does. Standard Bode plot analysis can be used to understand and adjust the voltage feedback loop.

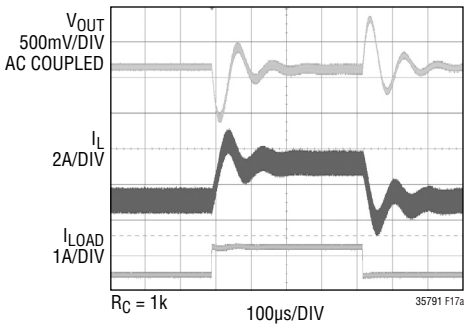


Figure 17a. Transient Response Shows Excessive Ringing

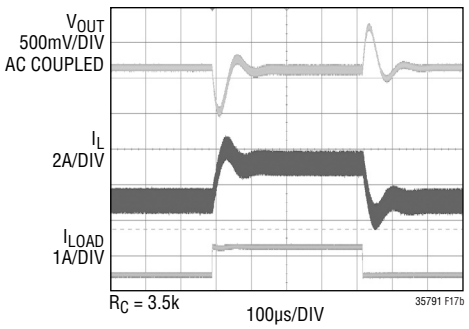


Figure 17b. Transient Response Is Better

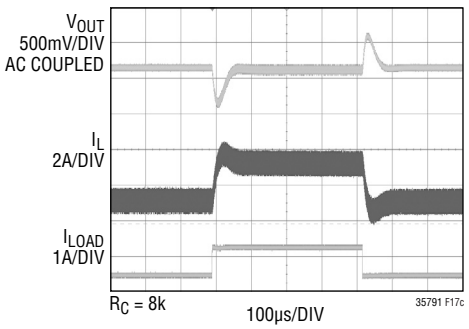
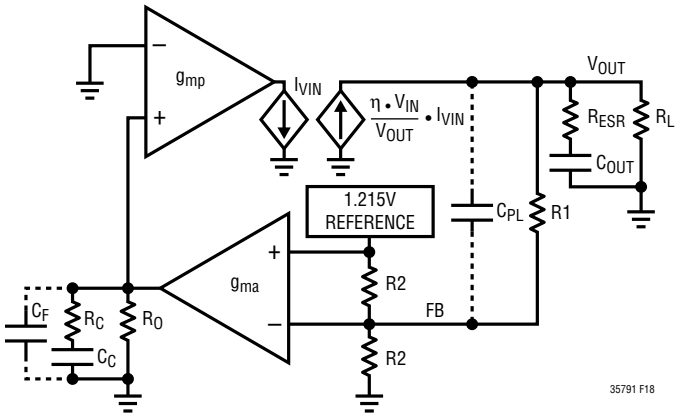


Figure 17c. Transient Response Is Well Damped

APPENDIX

As with any feedback loop, identifying the gain and phase contribution of the various elements in the loop is critical. Figure 18 shows the key equivalent elements of a boost converter. Because of the fast current control loop, the power stage of the IC, inductor and diode have been replaced by a combination of the equivalent transconductance amplifier g_{mp} and the current controlled current source (which converts I_{VIN} to $\frac{\eta V_{IN}}{V_{OUT}} I_{VIN}$). G_{mp} acts as a current source where the peak input current, I_{VIN}, is proportional to the V_C voltage.



C_C: COMPENSATION CAPACITOR
C_{OUT}: OUTPUT CAPACITOR
C_{PL}: PHASE LEAD CAPACITOR
C_F: HIGH FREQUENCY FILTER CAPACITOR
g_{ma}: TRANSCONDUCTOR AMPLIFIER INSIDE IC
g_{mp}: POWER STAGE TRANSCONDUCTANCE AMPLIFIER
R_C: COMPENSATION RESISTOR
R_L: OUTPUT RESISTANCE DEFINED AS $V_{OUT}/I_{LOADMAX}$
R_O: OUTPUT RESISTANCE OF gma
R1, R2; FEEDBACK RESISTOR DIVIDER NETWORK
R_{ESR}: OUTPUT CAPACITOR ESR
η: CONVERTER EFFICIENCY (~90% AT HIGHER CURRENTS)

Figure 18. Boost Converter Equivalent Model

Note that the maximum output currents of g_{mp} and g_{ma} are finite. The output of the g_{mp} stage is limited by the minimum switch current limit (see Electrical Specifications) and g_{ma} is nominally limited to about ±12µA.

From Figure 18, the DC gain, poles and zeros can be calculated as follows:

DC Gain:

$$A_{DC} = g_{ma} \bullet R_O \bullet g_{mp} \bullet \eta \bullet \frac{V_{IN}}{V_{OUT}} \bullet \frac{R_L}{2} \bullet \frac{0.5R_2}{R_1 + 0.5R_2}$$

$$\text{Output Pole: } P1 = \frac{2}{2 \bullet \pi \bullet R_L \bullet C_{OUT}}$$

$$\text{Error Amp Pole: } P2 = \frac{1}{2 \bullet \pi \bullet (R_O + R_C) \bullet C_C}$$

$$\text{Error Amp Zero: } Z1 = \frac{1}{2 \bullet \pi \bullet R_C \bullet C_C}$$

$$\text{ESR Zero: } Z2 = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}}$$

$$\text{RHP Zero: } Z3 = \frac{V_{IN}{}^2 \bullet R_L}{2 \bullet \pi \bullet V_{OUT}{}^2 \bullet L}$$

$$\text{High Frequency Pole: } P3 > \frac{f_S}{3}$$

$$\text{Phase Lead Zero: } Z4 = \frac{1}{2 \bullet \pi \bullet R_1 \bullet C_{PL}}$$

$$\text{Phase Lead Pole: } P4 = \frac{1}{2 \bullet \pi \bullet \frac{R_1 \bullet 0.5R_2}{R_1 + 0.5R_2} \bullet C_{PL}}$$

Error Amp Filter Pole:

$$P5 = \frac{1}{2 \bullet \pi \bullet \frac{R_C \bullet R_O}{R_C + R_O} C_F}, C_F < \frac{C_C}{10}$$

APPENDIX

The current mode zero (Z3) is a right half plane zero which can be an issue in feedback control design, but is manageable with proper external component selection.

Using the circuit in Figure 20 as an example, Table 8 shows the parameters used to generate the Bode plot shown in Figure 19.

Table 8. Bode Plot Parameters

PARAMETER	VALUE	UNITS	COMMENT
R_L	7	Ω	Application Specific
C_{OUT}	30	µF	Application Specific
R_{ESR}	2	mΩ	Application Specific
R0	305	kΩ	Not Adjustable
C_C	2200	pF	Adjustable
C_F	47	pF	Optional/Adjustable
C_{PL}	0	pF	Optional/Adjustable
R_C	8	kΩ	Adjustable
R1	130	kΩ	Adjustable
R2	14.6	kΩ	Not Adjustable
V_{OUT}	12	V	Application Specific
V_{IN}	5	V	Application Specific
g_{ma}	250	µmho	Not Adjustable
g_{mp}	28	mho	Not Adjustable
L	2.2	µH	Application Specific
f_{OSC}	1.0	MHz	Adjustable

From Figure 19, the phase is –134° when the gain reaches 0dB giving a phase margin of 46°. The crossover frequency is 8kHz, which is more than three times lower than the frequency of the RHP zero Z3 to achieve adequate phase margin.

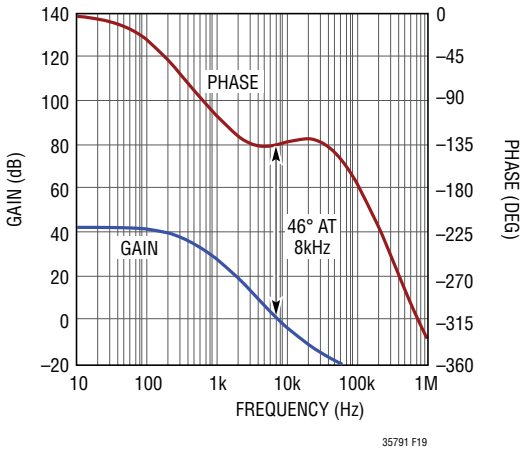


Figure 19. Bode Plot for Example Boost Converter

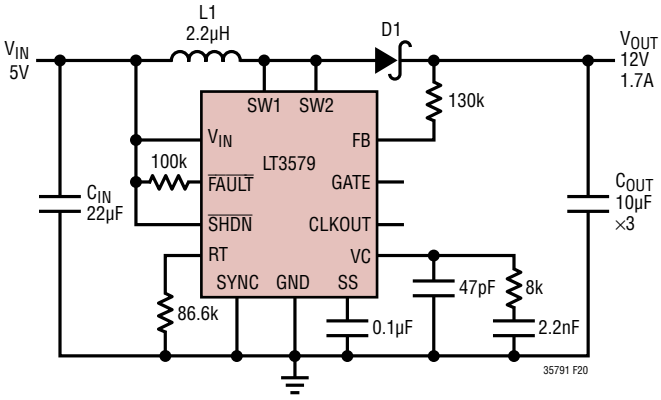
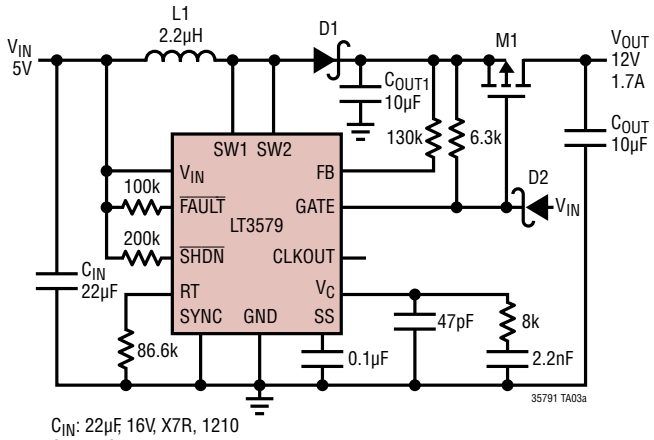


Figure 20. 5V to 12V Boost Converter

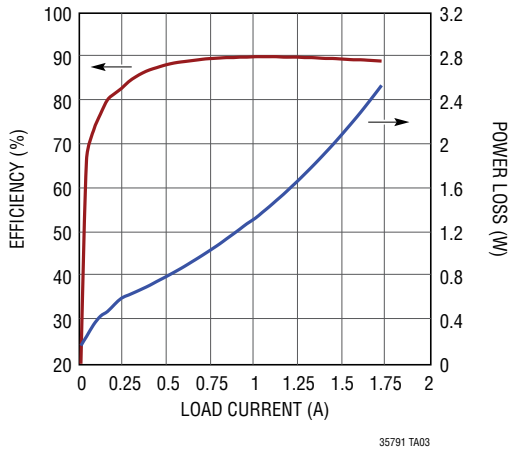
TYPICAL APPLICATION

1MHz, 5V to 12V Boost Converter can Survive Output Shorts

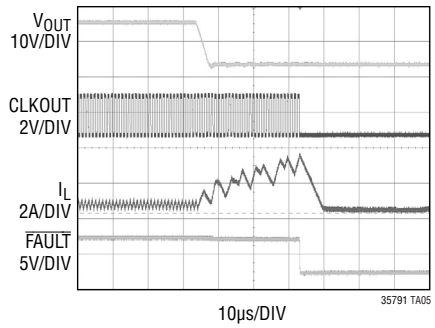


C_{IN}: 22µF, 16V, X7R, 1210
C_{OUT1}, C_{OUT}: 10µF, 25V, X7R, 1210
D1: VISHAY SSB43L
D2: CENTRAL SEMI CMDSH-3TR
L1: WÜRTH WE-PD 744771002
M1: SILICONIX SI7123DN

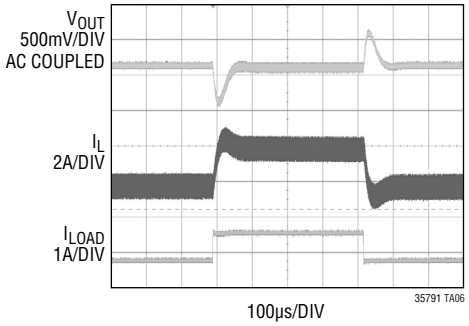
Efficiency and Power Loss



Output Short

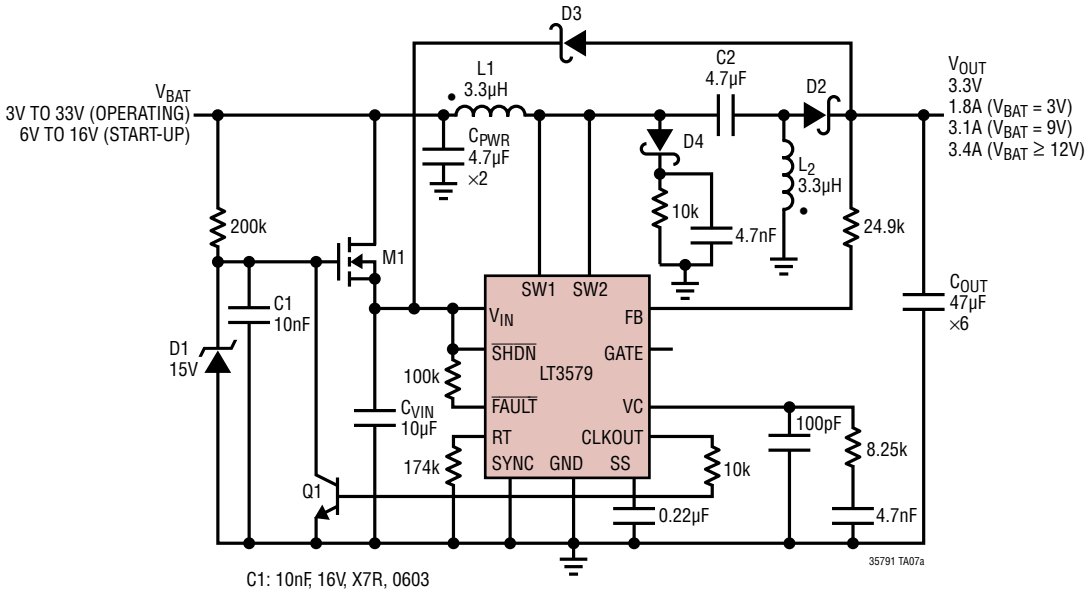


Transient Response with 0.7A to 1.5A to 0.7A Output Load Step



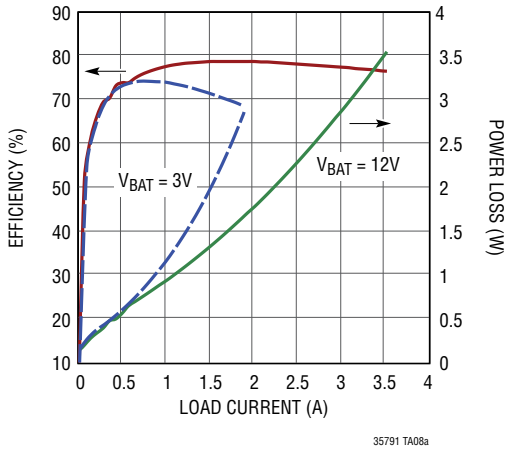
TYPICAL APPLICATION

500kHz SEPIC Converter Generates 3.3V from a 3V to 33V Input

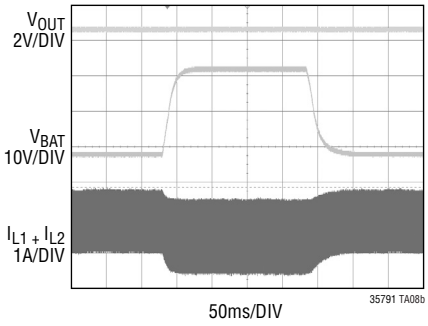


C1: 10nF, 16V, X7R, 0603
C_{VIN}: 10µF, 16V, X7R, 1206
C_{PWR}, C2: 4.7µF, 50V, X7R, 1210
C_{OUT}: 47µF, 6.3V, X7R, 1210
D1: CENTRAL SEMI CMHZ5245B-LTZ
D2: VISHAY SS5P6
D3: CENTRAL SEMI CMMSH2-40
D4: CENTRAL SEMI CMMSH2-40
L1, L2: WÜRTH WE-DD 744870003
M1: 2N7002
Q1: MMBT3904

Efficiency and Power Loss

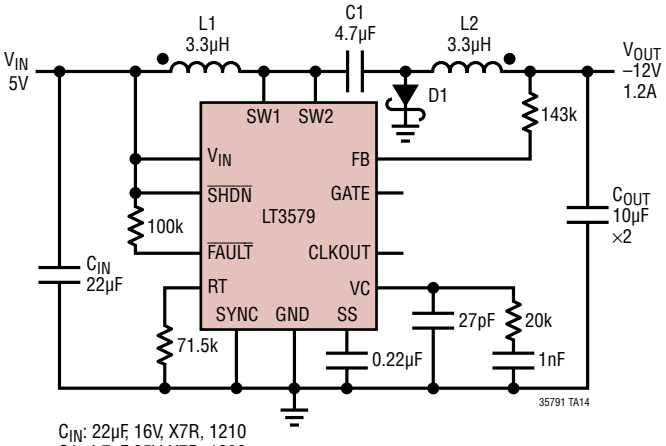


Transient Response with 9V to 33V to 9V V_{BAT} Glitch (R_{LOAD} = 1.5Ω)



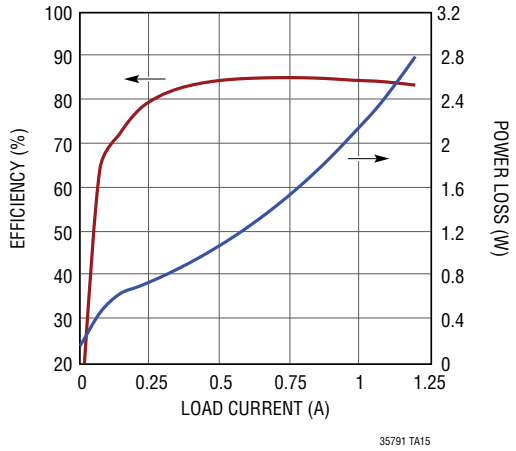
TYPICAL APPLICATION

1.2MHz, 5V to -12V Inverting Converter

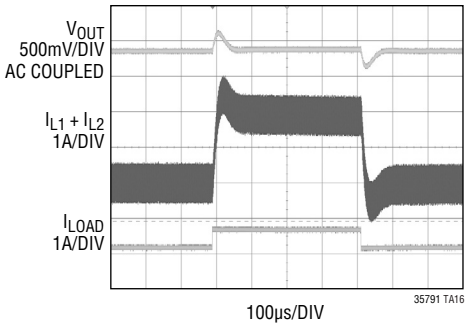


C_{IN}: 22µF, 16V, X7R, 1210
C1: 4.7µF, 25V, X7R, 1206
C_{OUT}: 10µF, 25V, X7R, 1210
D1: DIODES INC B230A
L1, L2: COOPER BUSSMANN DRQ125-3R3-R

Efficiency and Power Loss



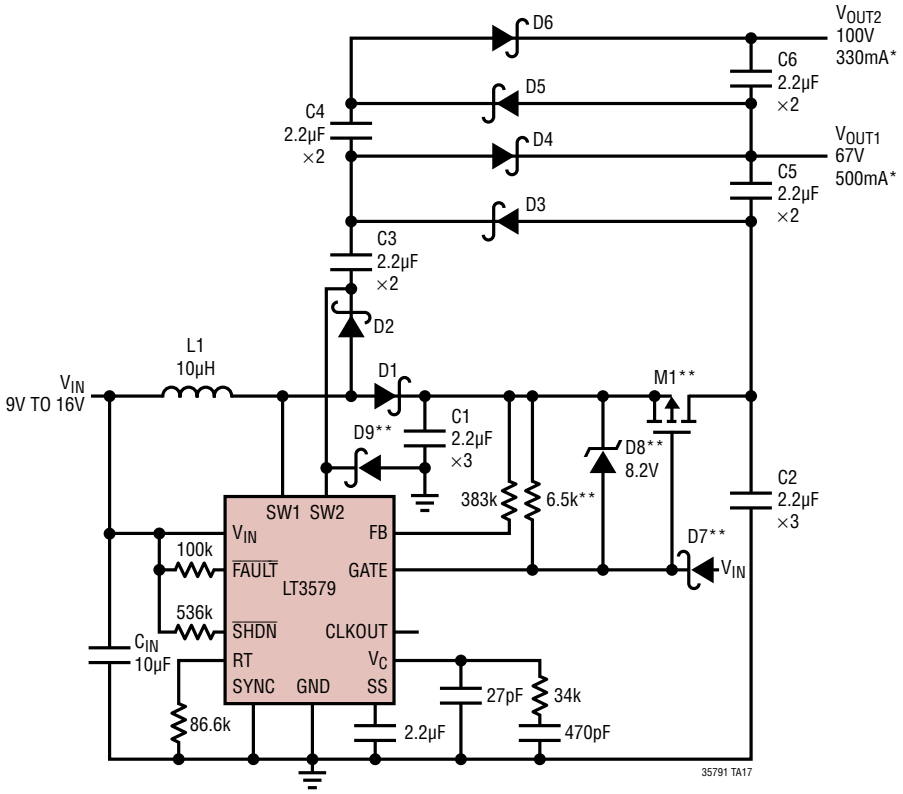
Transient Response with 0.5A to 1A to 0.5A Output Load Step



TYPICAL APPLICATION

VFD (Vacuum Fluorescent Display) Power Supply Switches at 1MHz

Danger High Voltage! Operation by High Voltage Trained Personnel Only



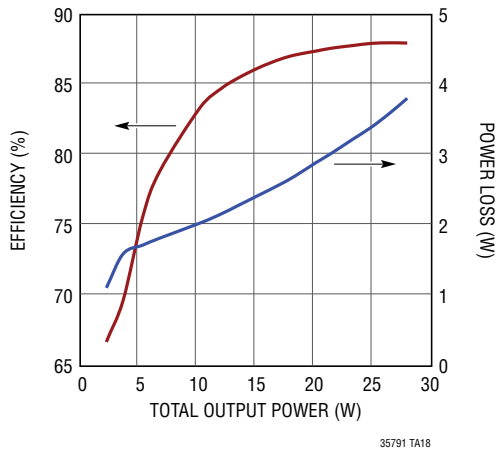
C_{IN}: 10µF, 25V, X7R, 1210
C1-C6: 2.2µF, 50V, X7R, 1210
D1-D6: DIODES INC SBR2A40P1
D7: CENTRAL SEMI CMDSH-3TR
D8: CENTRAL SEMI CMDZ5237B-LTZ
D9: DIODES INC MBRM360
L1: WÜRTH WE-PD 7447710
M1: SILICONIX SI7461DP

*MAX TOTAL OUTPUT POWER

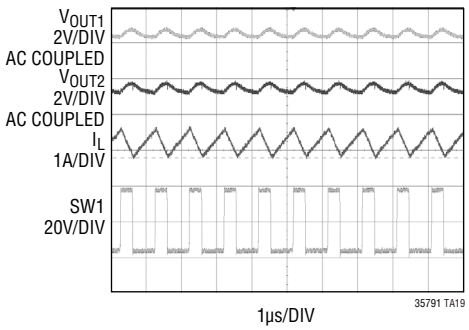
22W (V_{IN} = 9V)
27W (V_{IN} = 12V)
33W (V_{IN} = 16V)

**OPTIONAL FOR OUTPUT SHORT CIRCUIT PROTECTION

Efficiency and Power Loss (V_{IN} = 12V)

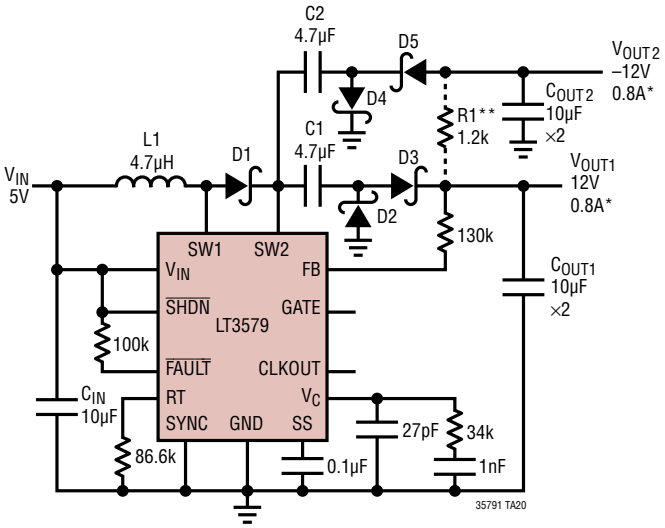


Cycle-to-Cycle



TYPICAL APPLICATION

1MHz, 5V to ±12V Converter

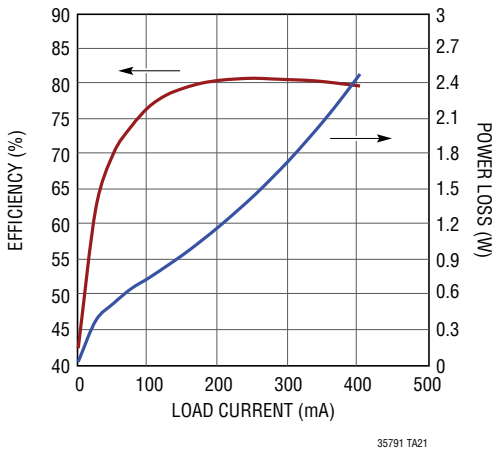


C_{IN}: 10µF, 16V, X7R, 1206
C1, C2: 4.7µF, 25V, X7R, 1206
C_{OUT1}, C_{OUT2}: 10µF, 25V, X7R, 1210
D1-D5: DIODES INC SBR2A40P1
L1: VISHAY IHLP-2525CZ-01-4R7
R1: 1.2k, 2W

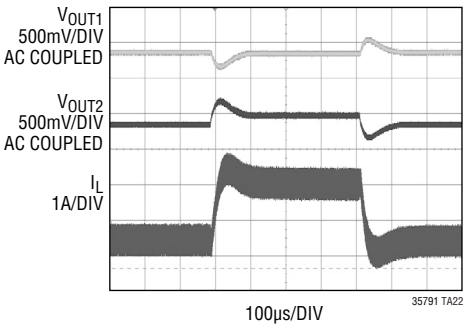
*MAX TOTAL OUTPUT POWER = 9.6W

**IF DRIVING ASYMMETRICAL LOADS, PLACE A 1.2k, 2W RESISTOR FROM THE +12V OUTPUT TO THE –12V OUTPUT FOR IMPROVED LOAD REGULATION OF THE –12V OUTPUT.

Efficiency and Power Loss

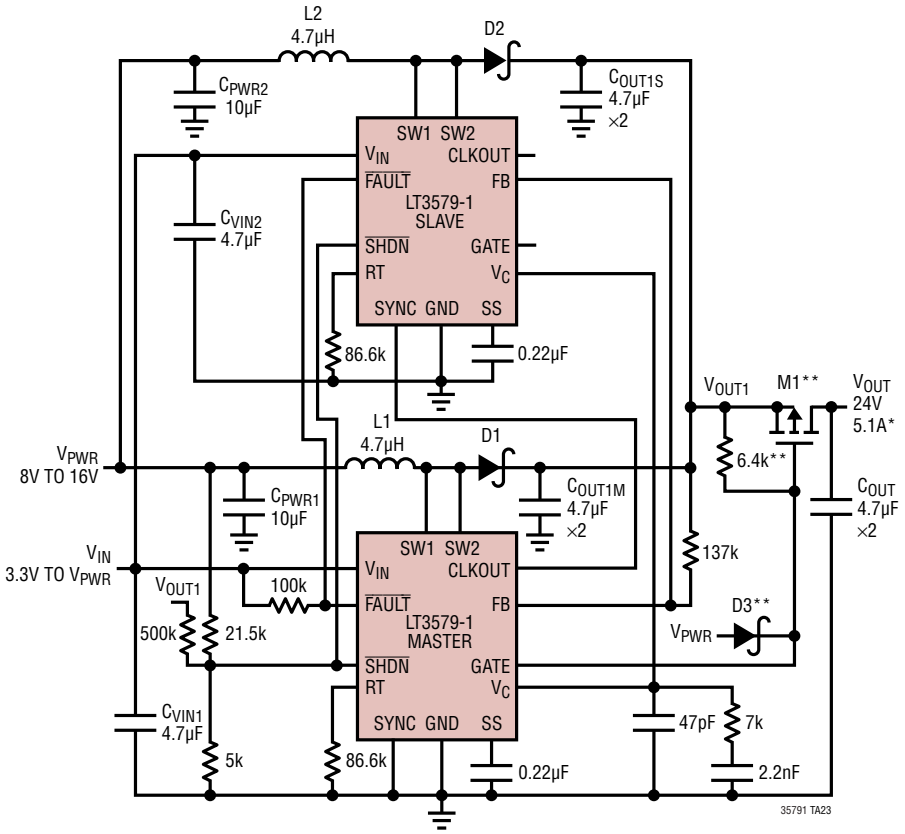


Transient Response with 0.15A to 0.35A to 0.15A Symmetrical Output Load Step



TYPICAL APPLICATION

1MHz, 2-Phase Converter Generates a 24V Output from a 8V to 16V Input and Uses Small Components



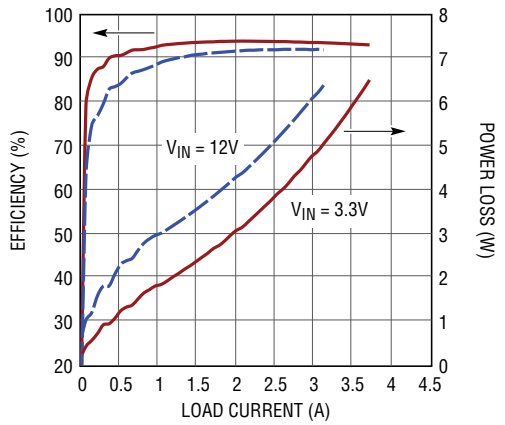
C_{PWR1}, C_{PWR2}: 10µF, 25V, X7R, 1210
C_{VIN1}, C_{VIN2}: 4.7µF, 25V, X7R, 1206
C_{OUT1M}, C_{OUT1S}, C_{OUT}: 4.7µF, 50V, X5R, 1210
D1, D2: CENTRAL SEMI CTLSH5-40M833
D3: CENTRAL SEMI CTLSH1-40M563
L1, L2: VISHAY IHLP-2525CZ-01-4R7
M1: SILICONIX SI7461DP

***MAX OUTPUT CURRENT**

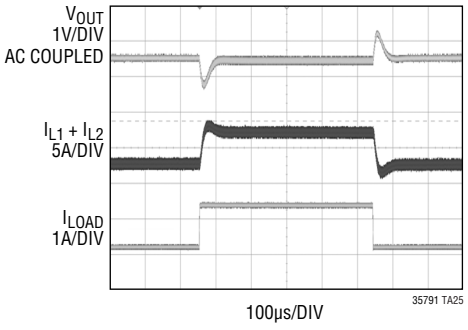
	V_{PWR} = 8V	V_{PWR} = 12V	V_{PWR} = 16V
V_{IN} = 3.3V TO 5V	2.4A	3.7A	5.1A
V_{IN} = V_{PWR}	2.2A	3.1A	3.9A

**OPTIONAL FOR OUTPUT SHORT CIRCUIT PROTECTION

Efficiency and Power Loss (V_{PWR} = 12V)

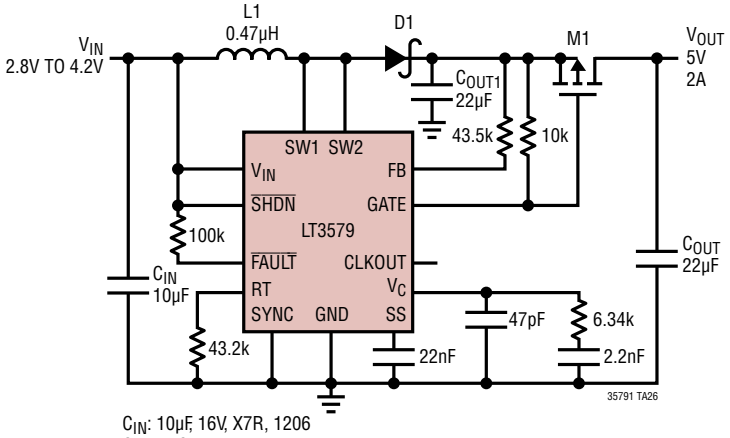


Transient Response with 1.5A to 3.25A to 1.5A Output Load Step (V_{PWR} = 12V and V_{IN} = 3.3V)



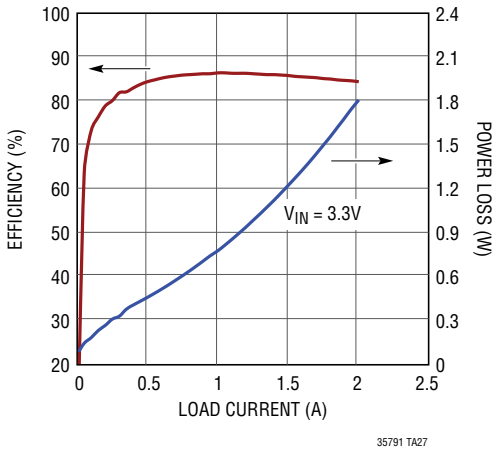
TYPICAL APPLICATION

2MHz, Boost Converter with Output Disconnect Generates a 5V Output from 2.8V to 4.2V Input

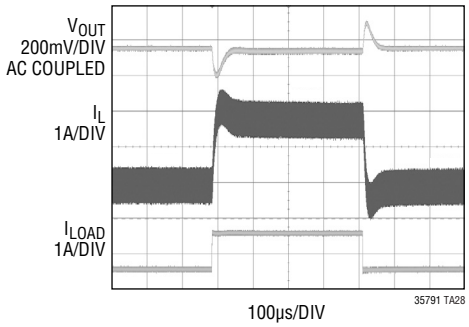


C_{IN}: 10µF, 16V, X7R, 1206
C_{OUT1}, C_{OUT}: 22µF, 16V, X7R, 1210
D1: CENTRAL SEMI CTLSH3-30M833
L1: VISHAY IHLP-2020BZ-01-R47
M1: SILICONIX SI7123DN

Efficiency and Power Loss

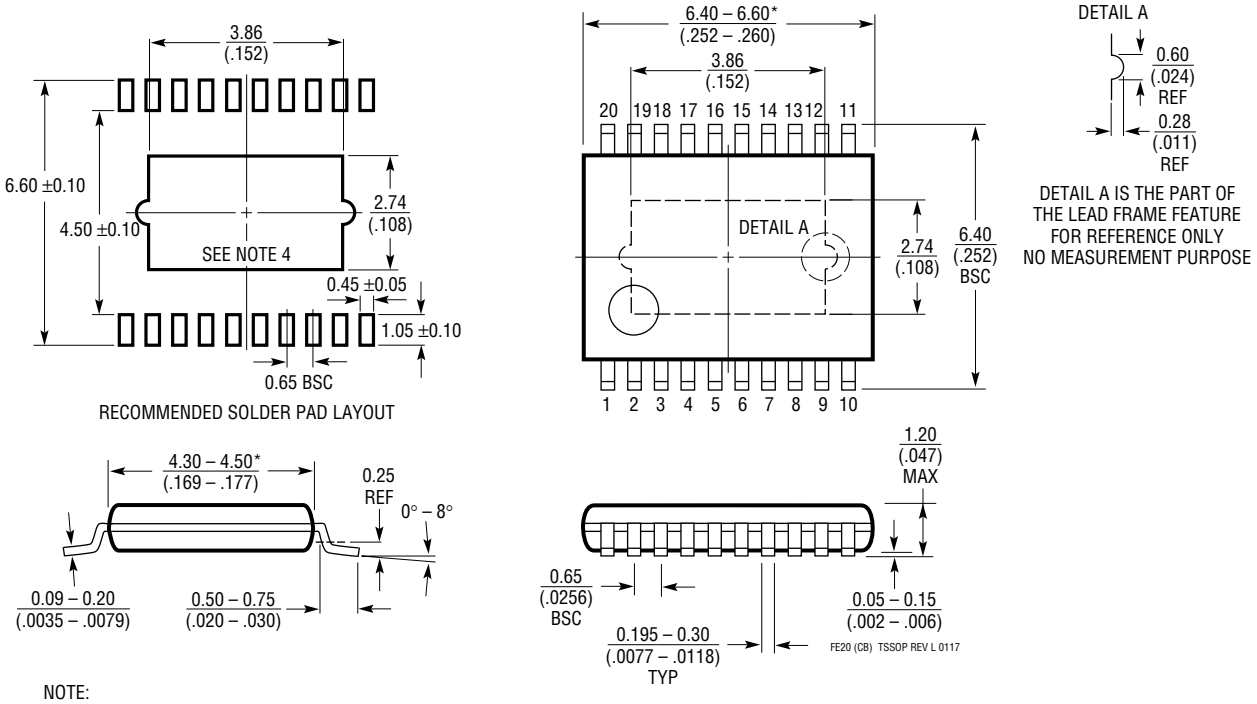


Transient Response with 0.8A to 1.8A to 0.8A Output Load Step (V_{IN} = 3.3V)



PACKAGE DESCRIPTION

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation CB

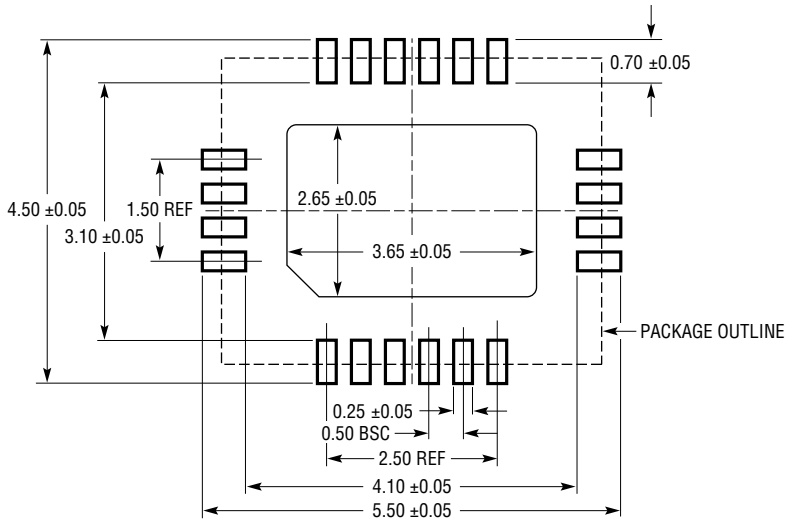


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

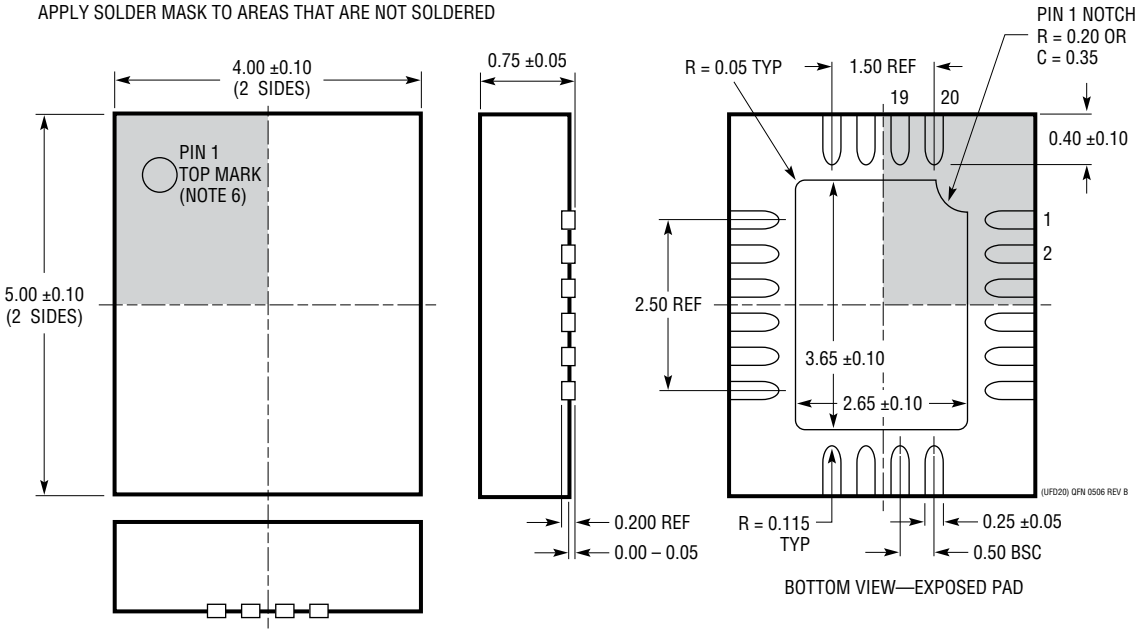
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

UFD Package
20-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1711 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

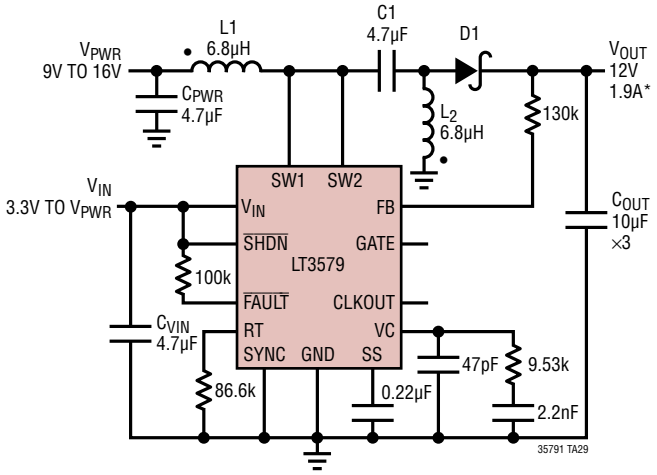
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

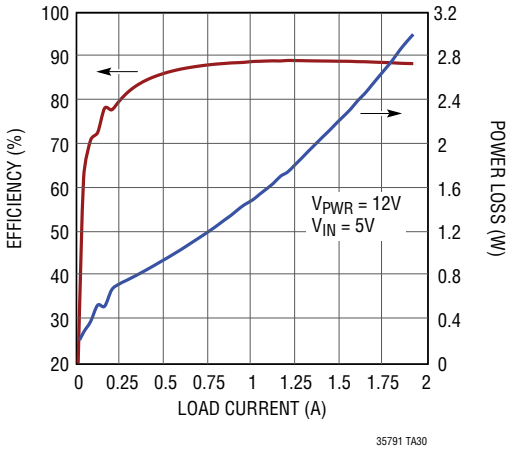
REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/14	Clarified Electrical Specifications	4
		Clarified Table 1	13
		Clarified Table 2	14
		Clarified Table 3	15
		Clarified Table 8	30
B	10/18	Added Note 5 to Switch V_{CESAT} parameter and notes section	3, 4

TYPICAL APPLICATION

1MHz SEPIC Converter Generates a 12V Output from a 9V to 16V Input



Efficiency and Power Loss



C_{PWR}: 4.7µF, 25V, X7R, 1206
C_{VIN}: 4.7µF, 25V, X7R, 1206
C1: 4.7µF, 25V, X7R, 1206
C_{OUT}: 10µF, 25V, X7R, 1210
D1: DIODES INC MBRM360
L1, L2: COOPER BUSSMANN DRQ125-6R8-R

***MAX OUTPUT CURRENT**

	V_{PWR} = 9V	V_{PWR} = 12V
V_{IN} = 3.3V TO 5V	1.6A	1.9A
V_{IN} = V_{PWR}	1.4A	1.4A

LINE REGULATION (V_{IN} = 5V, I_{OUT} = 1A) = 0.017%/V
LOAD REGULATION (V_{PWR} = 12V, V_{IN} = 5V) = –0.23%/A

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3581	3.3A (I_{SW}), 42V, 2.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 22V, $V_{OUT(MAX)}$ = 42V, I_Q = 1.9mA, I_{SD} = < 1µA, 4mm × 3mm DFN-14, MSOP-16E
LT3580	2A (I_{SW}), 42V, 2.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 32V, $V_{OUT(MAX)}$ = 42V, I_Q = 1mA, I_{SD} = < 1µA, 3mm × 3mm DFN-8, MSOP-8E
LT3479	3A (I_{SW}), 40V, 3.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 24V, $V_{OUT(MAX)}$ = 40V, I_Q = 5mA, I_{SD} = < 1µA, 4mm × 3mm DFN-14, TSSOP-16E