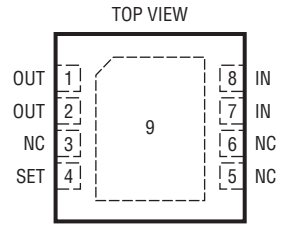
ABSOLUTE MAXIMUM RATINGS (Note 1) All Voltages Relative to V_{OUT}

IN Pin Voltage Relative to SET, OUT .....±40V
SET Pin Current (Note 6) .....±15mA
SET Pin Voltage (Relative to OUT, Note 6).....±10V
Output Short-Circuit Duration ..... Indefinite

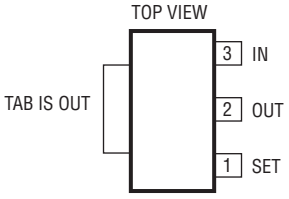
Operating Junction Temperature Range (Notes 2, 8)
E, I Grades ..... –40°C to 125°C
MP Grade..... –55°C to 125°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (ST, TS8 Packages Only)
Soldering, 10 sec..... 300°C

PIN CONFIGURATION



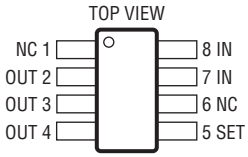
DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 28°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 9) IS OUT, MUST BE SOLDERED TO OUT ON THE PCB; SEE THE APPLICATIONS INFORMATION SECTION



ST PACKAGE
3-LEAD PLASTIC SOT-223

T_{JMAX} = 125°C, θ_{JA} = 24°C/W, θ_{JC} = 15°C/W
TAB IS OUT, MUST BE SOLDERED TO OUT ON THE PCB; SEE THE APPLICATIONS INFORMATION SECTION



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23

T_{JMAX} = 125°C, θ_{JA} = 57°C/W, θ_{JC} = 15°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3082EDD#PBF	LT3082EDD#TRPBF	LDYT	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3082IDD#PBF	LT3082IDD#TRPBF	LDYT	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3082EST#PBF	LT3082EST#TRPBF	3082	3-Lead Plastic SOT-223	–40°C to 125°C
LT3082IST#PBF	LT3082IST#TRPBF	3082	3-Lead Plastic SOT-223	–40°C to 125°C
LT3082MPST#PBF	LT3082MPST#TRPBF	3082MP	3-Lead Plastic SOT-223	–55°C to 125°C
LT3082ETS8#PBF	LT3082ETS8#TRPBF	LTDYV	8-Lead Plastic SOT-23	–40°C to 125°C
LT3082ITS8#PBF	LT3082ITS8#TRPBF	LTDYV	8-Lead Plastic SOT-23	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3082EDD	LT3082EDD#TR	LDYT	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3082IDD	LT3082IDD#TR	LDYT	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3082EST	LT3082EST#TR	3082	3-Lead Plastic SOT-223	–40°C to 125°C
LT3082IST	LT3082IST#TR	3082	3-Lead Plastic SOT-223	–40°C to 125°C
LT3082MPST	LT3082MPST#TR	3082MP	3-Lead Plastic SOT-223	–55°C to 125°C
LT3082ETS8	LT3082ETS8#TR	LTDYV	8-Lead Plastic SOT-23	–40°C to 125°C
LT3082ITS8	LT3082ITS8#TR	LTDYV	8-Lead Plastic SOT-23	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
SET Pin Current	I_{SET}	V_{IN} = 2V, I_{LOAD} = 1mA		9.90	10	10.10	µA
		2V ≤ V_{IN} ≤ 40V, 1mA ≤ I_{LOAD} ≤ 200mA	●	9.80	10	10.20	µA
Offset Voltage (V_{OUT} – V_{SET})	V_{OS}	V_{IN} = 2V, I_{LOAD} = 1mA		–2		2	mV
		V_{IN} = 2V, I_{LOAD} = 1mA	●	–4		4	mV
Load Regulation (Note 7)	ΔI_{SET}	ΔI_{LOAD} = 1mA to 200mA			–0.1		nA
	ΔV_{OS}	ΔI_{LOAD} = 1mA to 200mA	●		–0.5	–2	mV
Line Regulation	ΔI_{SET}	ΔV_{IN} = 2V to 40V, I_{LOAD} = 1mA			0.03	0.2	nA/V
	ΔV_{OS}	ΔV_{IN} = 2V to 40V, I_{LOAD} = 1mA			0.003	0.010	mV/V
Minimum Load Current (Note 3)		2V ≤ V_{IN} ≤ 40V	●		300	500	µA
Dropout Voltage (Note 4)		I_{LOAD} = 10mA	●		1.22	1.45	V
		I_{LOAD} = 200mA	●		1.3	1.65	V
Current Limit		V_{IN} = 5V, V_{SET} = 0V, V_{OUT} = –0.1V	●	200	300		mA
Error Amplifier RMS Output Noise (Note 5)		I_{LOAD} = 200mA, 10Hz ≤ f ≤ 100kHz, C_{OUT} = 10µF, C_{SET} = 0.1µF			33		μV_{RMS}
Reference Current RMS Output Noise (Note 5)		10Hz ≤ f ≤ 100kHz			0.7		nA_{RMS}
Ripple Rejection		f = 120Hz, V_{RIPPLE} = 0.5V_{P-P}, I_{LOAD} = 0.1A, C_{OUT} = 2.2µF, C_{SET} = 0.1µF			90		dB
		f = 10kHz			75		dB
		f = 1MHz			20		dB
Thermal Regulation	I_{SET}	10ms Pulse			0.003		%/W

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise specified, all voltages are with respect to V_{OUT}. The LT3082E is tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT3082E is 100% tested at T_A = 25°C. Performance at –40°C and 125°C is assured by design, characterization, and correlation with statistical process controls. The LT3082I is guaranteed to meet all data sheet specifications over the full –40°C to 125°C operating junction temperature range. The LT3082MP is 100% tested and guaranteed over the –55°C to 125°C operating junction temperature range.

Note 3: Minimum load current is equivalent to the quiescent current of the part. Since all quiescent and drive current is delivered to the output of the part, the minimum load current is the minimum current required to maintain regulation.

Note 4: For the LT3082, dropout is specified as the minimum input-to-output voltage differential required supplying a given output current.

Note 5: Adding a small capacitor across the reference current resistor lowers output noise. Adding this capacitor bypasses the resistor shot noise and reference current noise; output noise is then equal to error amplifier noise (see the Applications Information section).

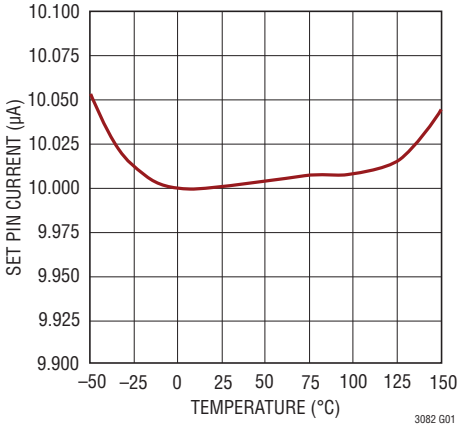
Note 6: Diodes with series 1k resistors clamp the SET pin to the OUT pin. These diodes and resistors only carry current under transient overloads.

Note 7: Load regulation is Kelvin-sensed at the package.

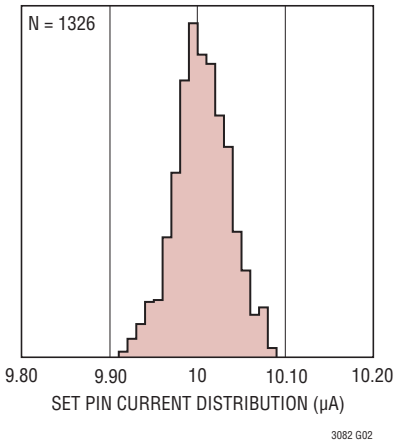
Note 8: This IC includes overtemperature protection that protects the device during momentary overload conditions. Junction temperature exceeds the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

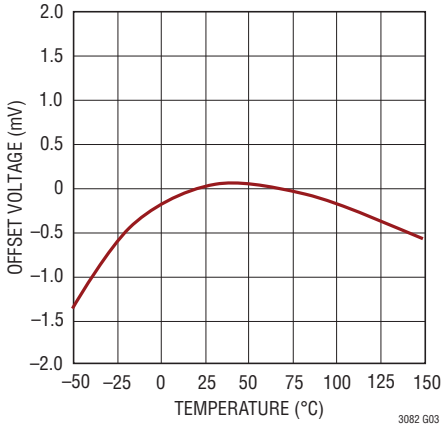
SET Pin Current



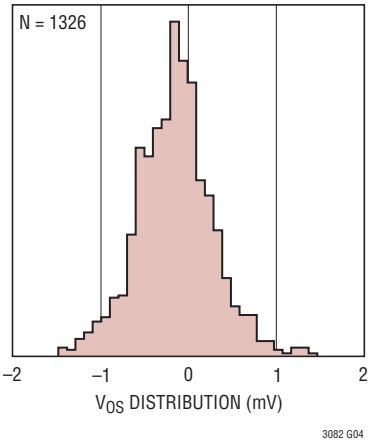
SET Pin Current Distribution



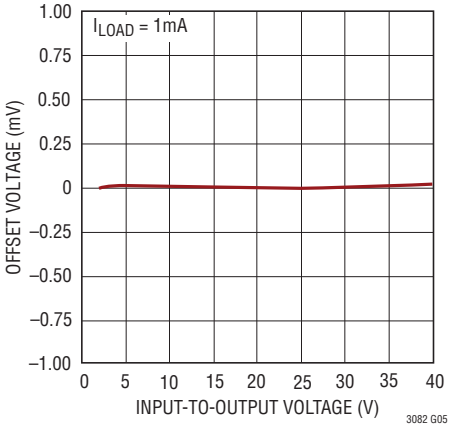
Offset Voltage ($V_{OUT} – V_{SET}$)



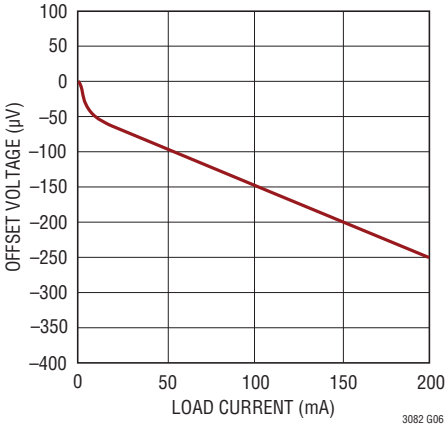
Offset Voltage Distribution



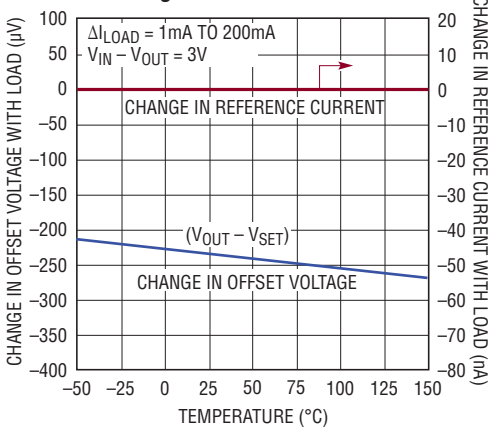
Offset Voltage



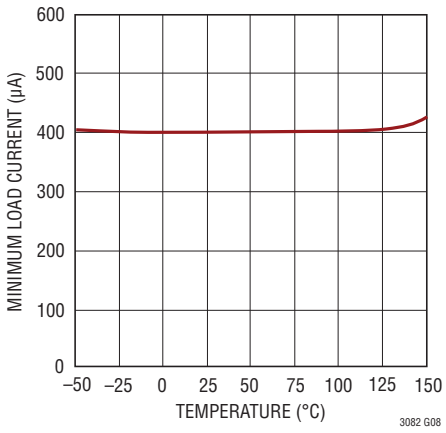
Offset Voltage



Load Regulation

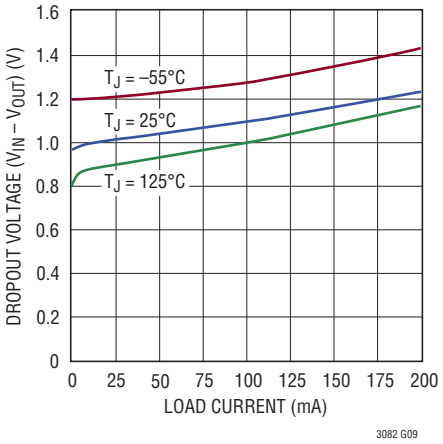


Minimum Load Current

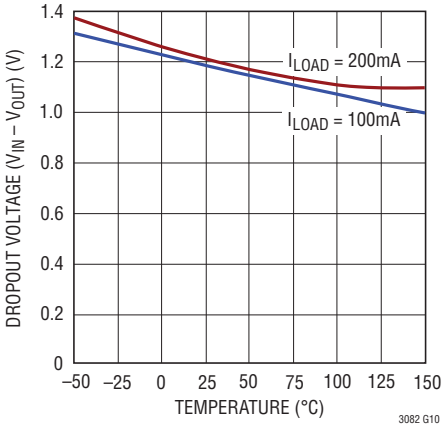


TYPICAL PERFORMANCE CHARACTERISTICS

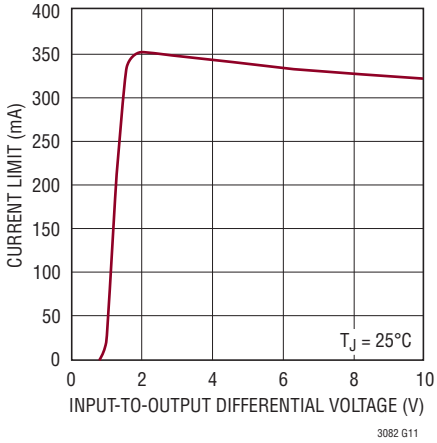
Dropout Voltage



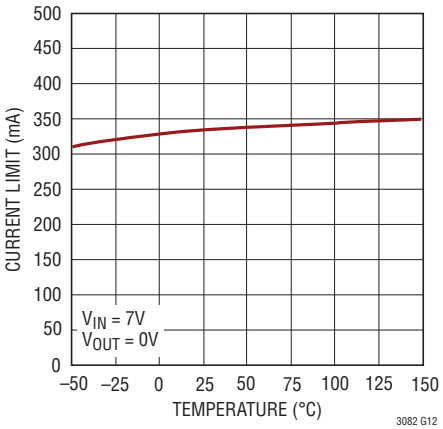
Dropout Voltage



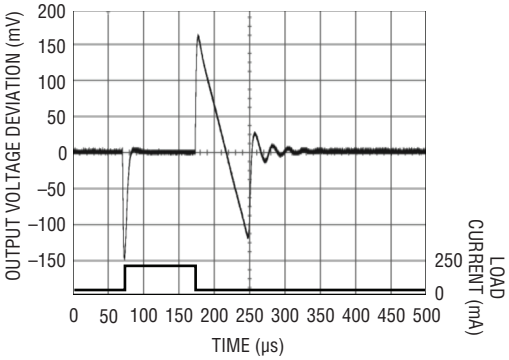
Current Limit



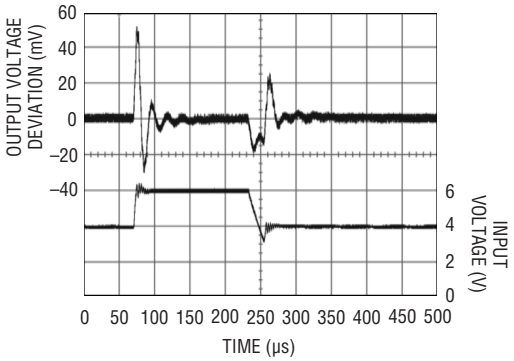
Current Limit



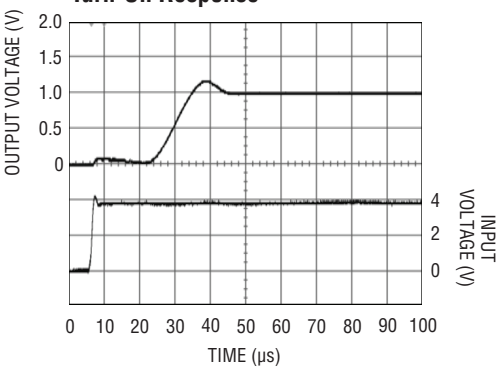
Load Transient Response



Line Transient Response

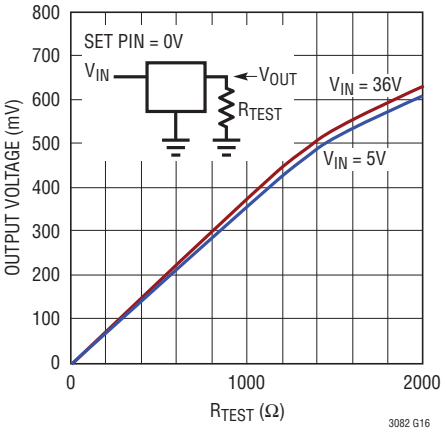


Turn-On Response

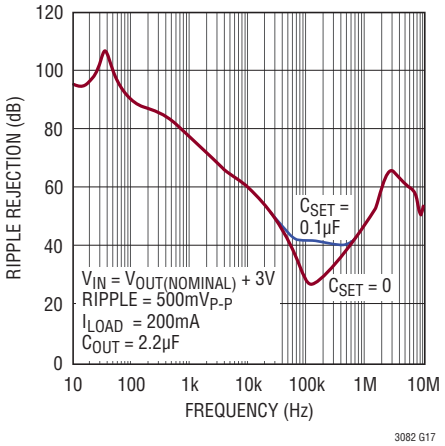


TYPICAL PERFORMANCE CHARACTERISTICS

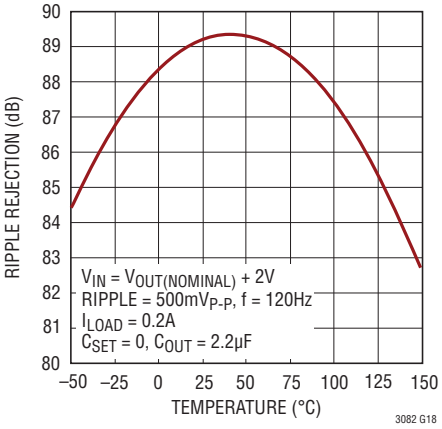
Residual Output for Less Than Minimum Load Current



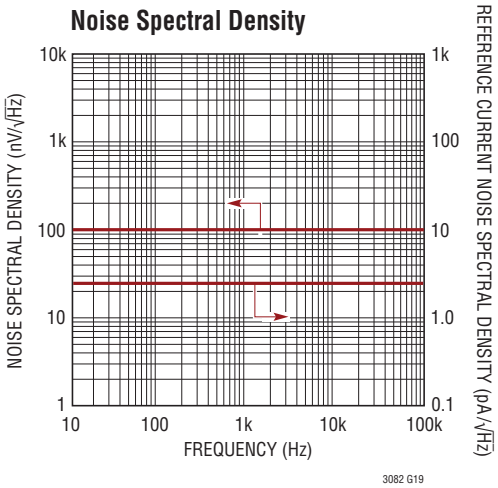
Ripple Rejection



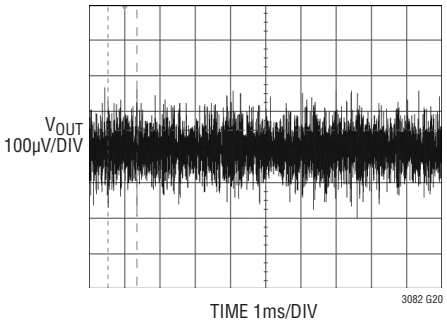
Ripple Rejection (120Hz)



Noise Spectral Density



Output Voltage Noise



VOUT = 1V
RSET = 100k
CSET = 0.1µF
COUT = 2.2µF
ILOAD = 200mA

PIN FUNCTIONS (DD/ST/TS8)

IN (Pins 7, 8/Pin 3/Pins 7, 8): Input. This pin supplies power to regulate internal circuitry and supply output load current. For the device to operate properly and regulate, the voltage on this pin must be 1.2V to 1.4V above the OUT pin (depending on output load current—see the dropout voltage specifications in the Electrical Characteristics table).

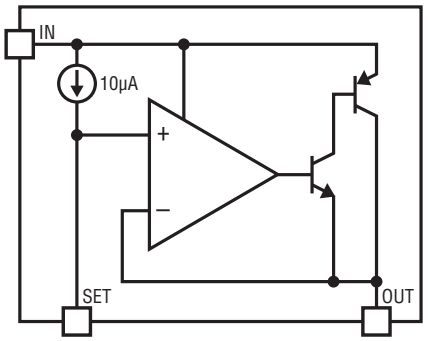
NC (Pins 3, 5, 6/NA/Pins 1, 6): No Connection. These pins have no connection to internal circuitry and may be tied to IN, OUT, GND or floated.

OUT (Pins 1, 2/Pin 2/Pins 2, 3, 4): Output. This is the power output of the device. The LT3082 requires a 0.5mA minimum load current or the output will not regulate.

SET (Pin 4/Pin 1/Pin 5): Set. This pin is the error amplifier's noninverting input and also sets the operating bias point of the circuit. A fixed 10µA current source flows out of this pin. A single external resistor programs V_{OUT}. Output voltage range is 0V to 38.5V.

Exposed Pad/Tab (Pin 9/Tab/NA): Output. The Exposed Pad of the DFN package and the Tab of the SOT-223 package are tied internally to OUT. Tie them directly to OUT pins (Pins 1, 2/Pin 2) at the PCB. The amount of copper area and planes connected to the Exposed Pad/Tab determine the effective thermal resistance of the packages (see the Applications Information section).

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Introduction

The LT3082 regulator is easy to use and has all the protection features expected in high performance regulators. Included are reverse-input, reverse-output and reverse input-to-output protection for sensitive circuitry and loads. Additional protection includes short-circuit protection and thermal shutdown with hysteresis.

The LT3082 fits well in applications needing multiple rails. This new architecture adjusts down to zero with a single resistor, handling modern low voltage digital IC's as well as allowing easy parallel operation and thermal management without heat sinks. Adjusting to zero output allows shutting off the powered circuitry. When the input is preregulated—such as a 5V or 3.3V input supply—external resistors can help spread the heat.

A precision "0" TC 10µA reference current source connects to the noninverting input of a power operational amplifier. The power operational amplifier provides a low impedance buffered output to the voltage on the noninverting input. A single resistor from the noninverting input to ground sets the output voltage. If this resistor is set to 0Ω, zero output voltage results. Therefore, any output voltage between zero and the maximum defined by the input power supply voltage is obtainable.

The benefit of using a true internal current source as the reference, as opposed to a bootstrapped reference in older regulators, is not so obvious in this architecture. A true reference current source allows the regulator to have gain and frequency response independent of the impedance on the positive input. On older adjustable regulators, such as the LT1086, loop gain changes with output voltage and bandwidth changes if the adjustment pin is bypassed to ground. For the LT3082, loop gain is unchanged with output voltage changes or bypassing. Output regulation is not a fixed percentage of output voltage, but is a fixed fraction of millivolts. Use of a true current source allows all of the gain in the buffer amplifier to provide regulation, and none of that gain is needed to amplify up the reference to a higher output voltage.

Programming Output Voltage

The LT3082 generates a 10µA reference current that flows out of the SET pin. Connecting a resistor from SET to GND generates a voltage that becomes the reference point for the error amplifier (see Figure 1). The reference voltage equals 10µA multiplied by the value of the SET pin resistor. Any voltage may be generated and there is no minimum output voltage for the regulator. Table 1 lists many common output voltages and the closest standard 1% resistor values used to generate that output voltage.

Regulation of the output voltage requires a minimum load current of 0.5mA. For a true 0V output operation, return this minimum 0.5mA load current to a negative supply voltage.

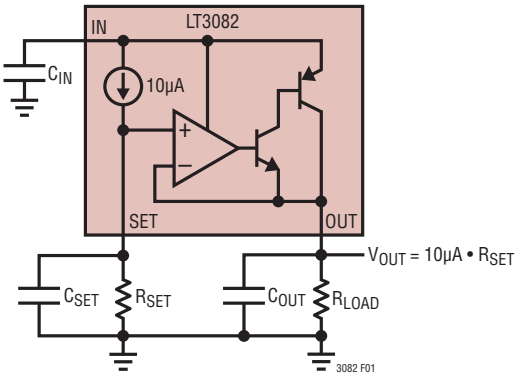


Figure 1. Basic Adjustable Regulator

APPLICATIONS INFORMATION

Table 1. 1% Resistors for Common Output Voltages

V_{OUT} (V)	R_{SET} (k)
1	100
1.2	121
1.5	150
1.8	182
2.5	249
3.3	332
5	499

With a 10µA current source generating the reference voltage, leakage paths to or from the SET pin can create errors in the reference and output voltages. High quality insulation should be used (e.g., Teflon, Kel-F). The cleaning of all insulating surfaces to remove fluxes and other residues may be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Minimize board leakage by encircling the SET pin and circuitry with a guard ring that is operated at a potential close to itself. Tie the guard ring to the OUT pin. Guarding both sides of the circuit board is required. Bulk leakage reduction depends on the guard ring width. 10nA of leakage into or out of the SET pin and its associated circuitry creates a 0.1% reference voltage error. Leakages of this magnitude, coupled with other sources of leakage, can cause significant offset voltage and reference drift, especially over the possible operating temperature range. Figure 2 depicts an example guard ring layout.

If guard ring techniques are used, this bootstraps any stray capacitance at the SET pin. Since the SET pin is a high impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This will be most noticeable when operating with minimum output capacitors at full load current. The easiest way to remedy this is to bypass the SET pin with a small amount of capacitance from SET to ground; 10pF to 20pF is sufficient.

Stability and Output Capacitance

The LT3082 requires an output capacitor for stability. It is designed to be stable with most low ESR capacitors (typically ceramic, tantalum or low ESR electrolytic). A minimum output capacitor of 2.2µF with an ESR of 0.5Ω or less is recommended to prevent oscillations. Larger values of output capacitance decrease peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3082, increase the effective output capacitor value. For improvement in transient response performance, place a capacitor across the voltage setting resistor. Capacitors up to 1µF can be used. This bypass capacitor reduces system noise as well, but start-up time is proportional to the time constant of the voltage setting resistor (R_{SET} in Figure 1) and SET pin bypass capacitor.

Give extra consideration to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of di-

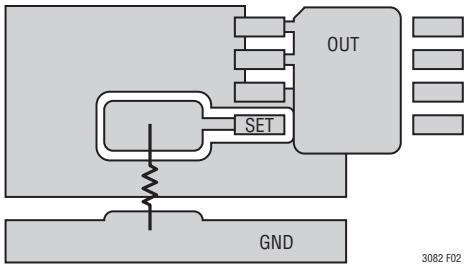


Figure 2. Example Guard Ring Layout for DFN Package

APPLICATIONS INFORMATION

electrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients, as shown in Figures 3 and 4. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than with Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress. In a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

Stability and Input Capacitance

Low ESR, ceramic input bypass capacitors are acceptable for applications without long input leads. However, applications connecting a power supply to an LT3082 circuit's IN and GND pins with long input wires combined with a low ESR, ceramic input capacitors are prone to voltage spikes, reliability concerns and application-specific board oscillations. The input wire inductance found in many battery powered applications, combined with the low ESR ceramic input capacitor, forms a high-Q LC resonant tank circuit. In some instances this resonant frequency beats against the output current dependent LDO bandwidth and interferes with proper operation. Simple circuit modifications/solutions are then required. This behavior is not indicative of LT3082 instability, but is a common ceramic input bypass capacitor application issue.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. Wire diameter is not a major factor on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire (diameter = 0.26") is about half the self-inductance of a 30-AWG wire (diameter = 0.01"). One foot of 30-AWG wire has about 465nH of self-inductance.

One of two ways reduces a wire's self-inductance. One method divides the current flowing towards the LT3082 between two parallel conductors. In this case, the farther apart the wires are from each other, the more the self-inductance is reduced; up to a 50% reduction when placed a few inches apart. Splitting the wires basically connects

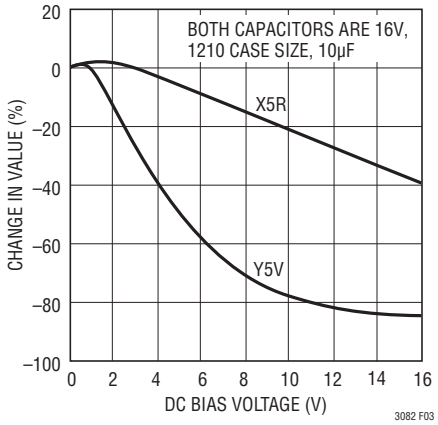


Figure 3. Ceramic Capacitor DC Bias Characteristics

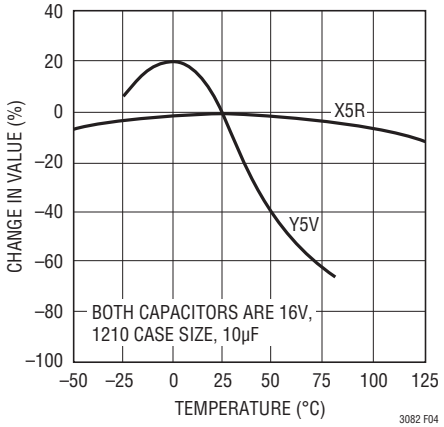


Figure 4. Ceramic Capacitor Temperature Characteristics

APPLICATIONS INFORMATION

two equal inductors in parallel, but placing them in close proximity gives the wires mutual inductance adding to the self-inductance. The second and most effective way to reduce overall inductance is to place both forward and return current conductors (the input and GND wires) in very close proximity. Two 30-AWG wires separated by only 0.02", used as forward- and return-current conductors, reduce the overall self-inductance to approximately one-fifth that of a single isolated wire.

If wiring modifications are not permissible for the applications, including series resistance between the power supply and the input of the LT3082 also stabilizes the application. As little as 0.1Ω to 0.5Ω, often less, is effective in damping the LC resonance. If the added impedance between the power supply and the input is unacceptable, adding ESR to the input capacitor also provides the necessary damping of the LC resonance. However, the required ESR is generally higher than the series impedance required.

Paralleling Devices

Higher output current is obtained by paralleling multiple LT3082s together. Tie the individual SET pins together and tie the individual IN pins together. Connect the outputs in common using small pieces of PC trace as ballast resistors to promote equal current sharing. PC trace resistance in mΩ/inch is shown in Table 2. Ballasting requires only a tiny area on the PCB.

Table 2. PC Board Trace Resistance

WEIGHT (oz)	10mil WIDTH	20mil WIDTH
1	54.3	27.1
2	27.1	13.6

Trace resistance is measured in mΩ/in

The worst-case room temperature offset, only ±2mV between the SET pin and the OUT pin, allows the use of very small ballast resistors.

As shown in Figure 5, each LT3082 has a small 50mΩ ballast resistor, which at full output current gives better than 80% equalized sharing of the current. The external resistance of 50mΩ (25mΩ for the two devices in parallel) adds only about 10mV of output regulation drop at an output of 0.4A. Even with an output voltage as low as 1V, this adds only 1% to the regulation. Of course, paralleling more than two LT3082s yields even higher output current.

Spreading the devices on the PC board also spreads the heat. Series input resistors can further spread the heat if the input-to-output difference is high.

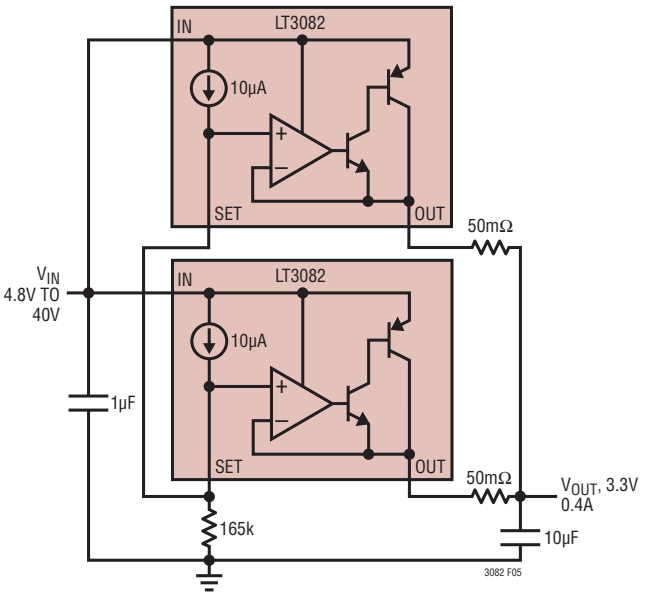


Figure 5. Parallel Devices

Quieting the Noise

The LT3082 offers numerous noise performance advantages. Every linear regulator has its sources of noise. In general, a linear regulator's critical noise source is the reference. In addition, consider the error amplifier's noise contribution along with the resistor divider's noise gain.

Many traditional low noise regulators bond out the voltage reference to an external pin (usually through a large value resistor) to allow for bypassing and noise reduction. The LT3082 does not use a traditional voltage reference like other linear regulators. Instead, it uses a 10µA reference current. The 10µA current source generates noise current levels of 2.7pA/$\sqrt{Hz}$ (0.7nA$_{RMS}$ over the 10Hz to 100kHz bandwidth). The equivalent voltage noise equals the RMS noise current multiplied by the resistor value.

The SET pin resistor generates spot noise equal to $\sqrt{4kTR}$ (k = Boltzmann's constant, $1.38 \cdot 10^{-23}$J/°K, and T is absolute temperature) which is RMS summed with the voltage noise If the application requires lower noise performance, bypass the voltage/current setting resistor with a capacitor to GND. Note that this noise-reduction capacitor increases start-up time as a factor of the RC time constant.

APPLICATIONS INFORMATION

The LT3082 uses a unity-gain follower from the SET pin to the OUT pin. Therefore, multiple possibilities exist (besides a SET pin resistor) to set output voltage. For example, using a high accuracy voltage reference from SET to GND removes the errors in output voltage due to reference current tolerance and resistor tolerance. Active driving of the SET pin is acceptable.

The typical noise scenario for a linear regulator is that the output voltage setting resistor divider gains up the noise reference, especially if V_{OUT} is much greater than V_{REF}. The LT3082's noise advantage is that the unity-gain follower presents no noise gain whatsoever from the SET pin to the output. Thus, noise figures do not increase accordingly. Error amplifier noise is typical 100nV/$\sqrt{Hz}$ (33μV_{RMS} over the 10Hz to 100kHz bandwidth). The error amplifier's noise is RMS summed with the other noise terms to give a final noise figure for the regulator.

Curves in the Typical Performance Characteristics section show noise spectral density and peak-to-peak noise characteristics for both the reference current and error amplifier over the 10Hz to 100kHz bandwidth.

Load Regulation

The LT3082 is a floating device. No ground pin exists on the packages. Thus, the IC delivers all quiescent current and drive current to the load. Therefore, it is not possible to provide true remote load sensing. The connection resistance between the regulator and the load determines load regulation performance. The data sheet's load regulation specification is Kelvin sensed at the package's pins. Negative-side sensing is a true Kelvin connection by returning the bottom of the voltage setting resistor to the negative side of the load (see Figure 6).

Connected as shown, system load regulation is the sum of the LT3082's load regulation and the parasitic line resistance multiplied by the output current. To minimize load regulation, keep the positive connection between the regulator and load as short as possible. If possible, use large diameter wire or wide PC board traces.

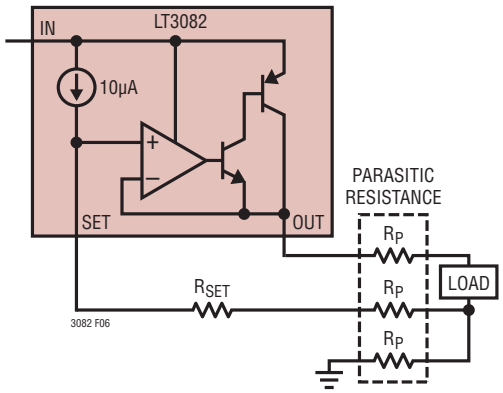


Figure 6. Connections for Best Load Regulation

Thermal Considerations

The LT3082's internal power and thermal limiting circuitry protects itself under overload conditions. For continuous normal load conditions, do not exceed the 125°C maximum junction temperature. Carefully consider all sources of thermal resistance from junction-to-ambient. This includes (but is not limited to) junction-to-case, case-to-heat sink interface, heat sink resistance or circuit board-to-ambient as the application dictates. Consider all additional, adjacent heat generating sources in proximity on the PCB.

Surface mount packages provide the necessary heatsinking by using the heat spreading capabilities of the PC board, copper traces and planes. Surface mount heat sinks, plated through-holes and solder-filled vias can also spread the heat generated by power devices.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly, or the bottom of the pin most directly, in the heat path. This is the lowest thermal resistance path for heat flow. Only proper device mounting ensures the best possible thermal flow from this area of the package to the heat sinking material.

Note that the Exposed Pad of the DFN package and the tab of the SOT-223 package is electrically connected to the output (V_{OUT}).

APPLICATIONS INFORMATION

Tables 3 through 5 list thermal resistance as a function of copper areas in a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes and 2oz external trace planes with a total finished board thickness of 1.6mm.

Table 3. DD Package, 8-Lead DFN

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	25°C/W
1000mm^2	2500mm^2	2500mm^2	25°C/W
225mm^2	2500mm^2	2500mm^2	28°C/W
100mm^2	2500mm^2	2500mm^2	32°C/W

*Device is mounted on topside

Table 4. TS8 Package, 8-Lead SOT-23

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	54°C/W
1000mm^2	2500mm^2	2500mm^2	54°C/W
225mm^2	2500mm^2	2500mm^2	57°C/W
100mm^2	2500mm^2	2500mm^2	63°C/W

*Device is mounted on topside

Table 5. ST Package, 3-Lead SOT-223

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	20°C/W
1000mm^2	2500mm^2	2500mm^2	20°C/W
225mm^2	2500mm^2	2500mm^2	24°C/W
100mm^2	2500mm^2	2500mm^2	29°C/W

*Device is mounted on topside

For further information on thermal resistance and using thermal information, refer to JEDEC standard JESD51, notably JESD51-12.

PCB layers, copper weight, board layout and thermal vias affect the resultant thermal resistance. Please reference JEDEC standard JESD51-7 for further information on high thermal conductivity test boards. Achieving low thermal resistance necessitates attention to detail and careful layout. Demo circuit 1447A's board layout using multiple inner V_{OUT} planes and multiple thermal vias achieves 28°C/W performance for the DFN package.

Calculating Junction Temperature

Example: Given an industrial factory application with an input voltage of 15V ±10%, an output voltage of 12V ±5%, an output current of 200mA and a maximum ambient temperature of 50°C, what would be the maximum junction temperature for a DFN package?

The total circuit power equals:

$$P_{TOTAL} = (V_{IN} – V_{OUT})(I_{OUT})$$

The SET pin current is negligible and can be ignored.

$V_{IN(MAX\ CONTINUOUS)}$ = 16.5 (15V + 10%)

$V_{OUT(MIN\ CONTINUOUS)}$ = 11.4V (12V – 5%)

I_{OUT} = 200mA

Power dissipation under these conditions equals:

$$P_{TOTAL} = (16.5 – 11.4V)(200mA) = 1.02W$$

Junction temperature equals:

$$T_J = T_A + P_{TOTAL} \bullet \theta_{JA}$$

$$T_J = 50°C + (1.02W \bullet 30°C/W) = 80.6°C$$

In this example, junction temperature is below the maximum rating, ensuring reliable operation.

APPLICATIONS INFORMATION

Protection Features

The LT3082 incorporates several protection features ideal for battery-powered circuits, among other applications. In addition to normal monolithic regulator protection features such as current limiting and thermal limiting, the LT3082 protects itself against reverse-input voltages, reverse-output voltages, and reverse OUT-to-SET pin voltages.

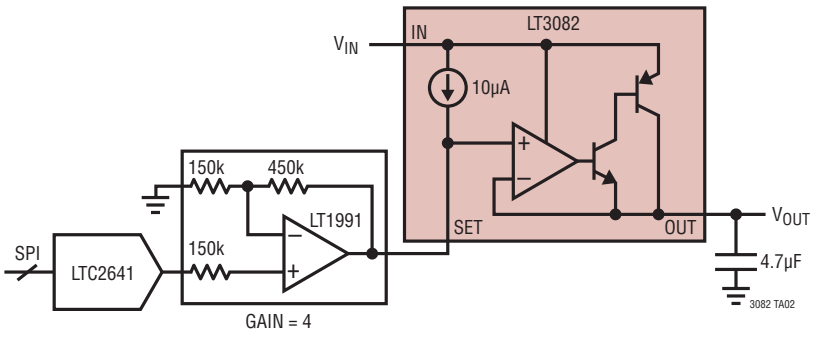
Current limit protection and thermal overload protection protect the IC against output current overload conditions. For normal operation, do not exceed a junction temperature of 125°C. The thermal shutdown circuit's temperature threshold is typically 165°C and incorporates about 5°C of hysteresis.

The LT3082's IN pin withstands ±40V voltages with respect to the OUT and SET pins. Reverse current flow, if OUT is greater than IN, is less than 1mA (typically under 100µA), protecting the LT3082 and sensitive loads.

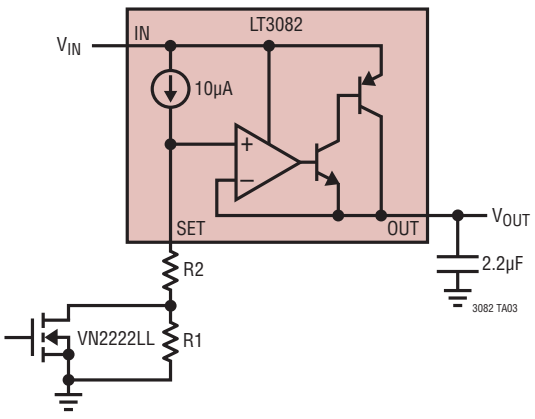
Clamping diodes and 1k limiting resistors protect the LT3082's SET pin relative to the OUT pin voltage. These protection components typically only carry current under transient overload conditions. These devices are sized to handle ±10V differential voltages and ±15mA crosspin current flow without concern. Relative to these application concerns, note the following two scenarios. The first scenario employs a noise-reducing SET pin bypass capacitor while OUT is instantaneously shorted to GND. The second scenario follows improper shutdown techniques in which the SET pin is reset to GND quickly while OUT is held up by a large output capacitance with light load. The Typical Applications section shows simple, robust techniques for shutting down SET and OUT together.

TYPICAL APPLICATIONS

DAC-Controlled Regulator

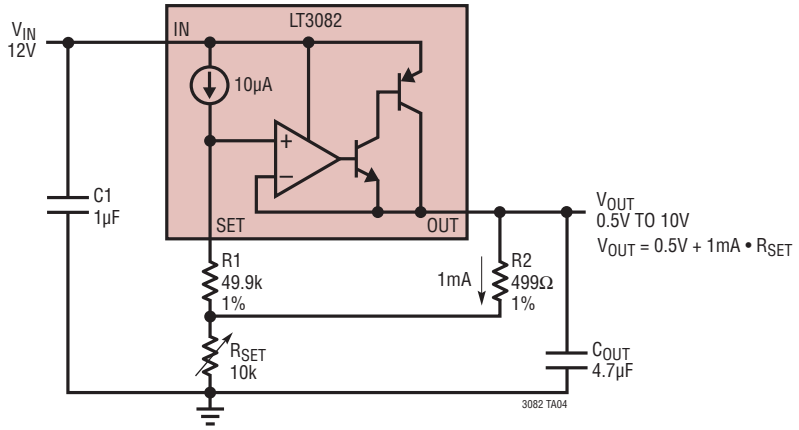


Two-Level Regulator

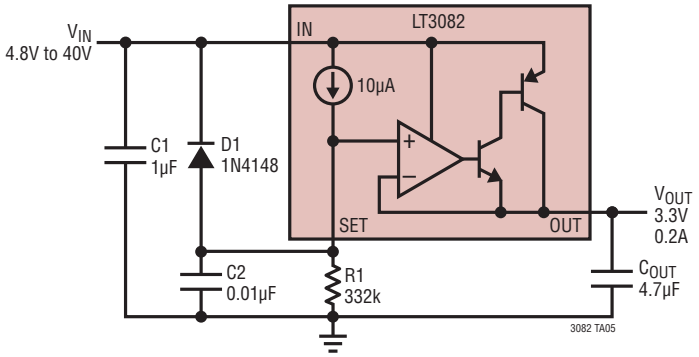


TYPICAL APPLICATIONS

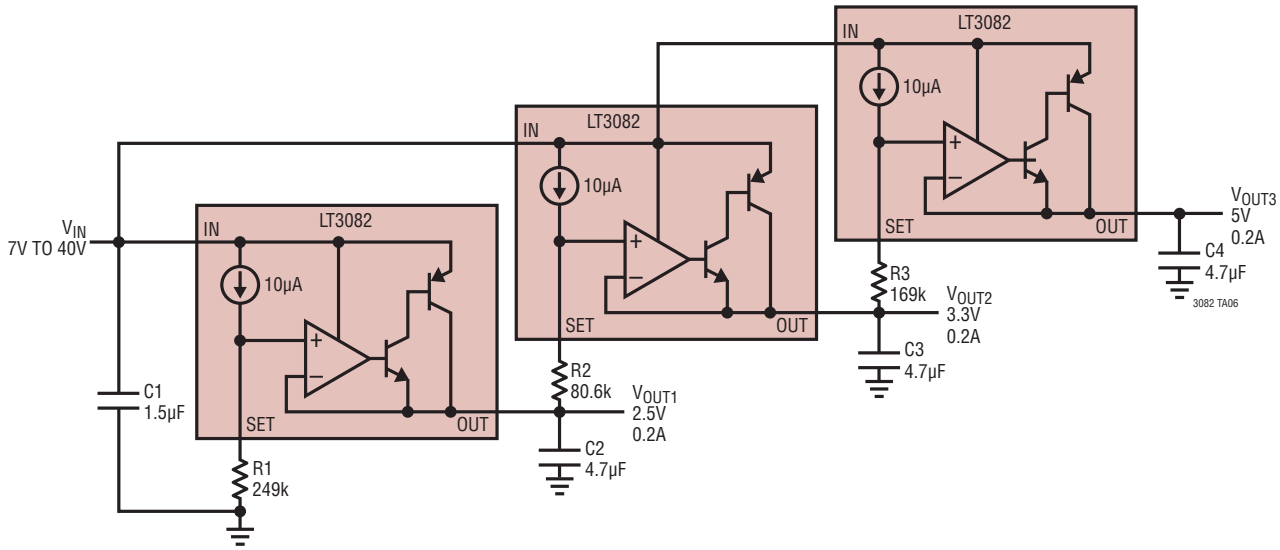
Using a Lower Value SET Resistor



Adding Soft-Start

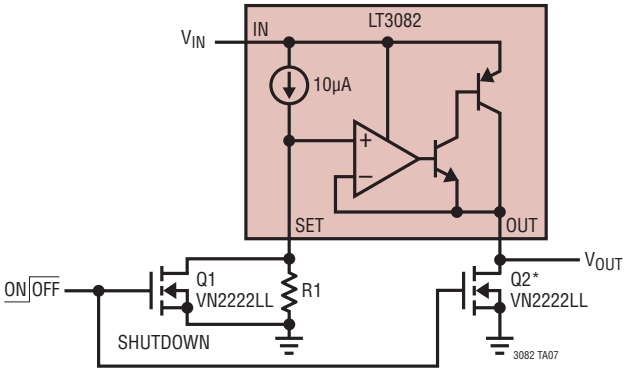


Coincident Tracking



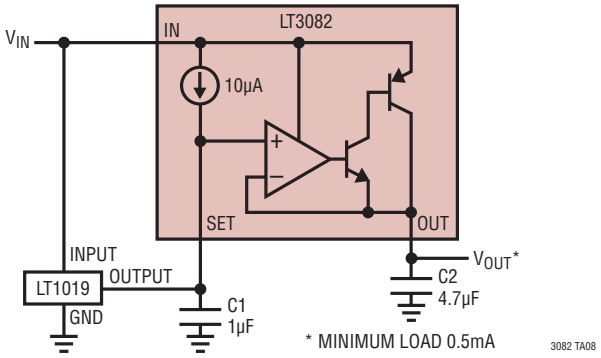
TYPICAL APPLICATIONS

Adding Shutdown

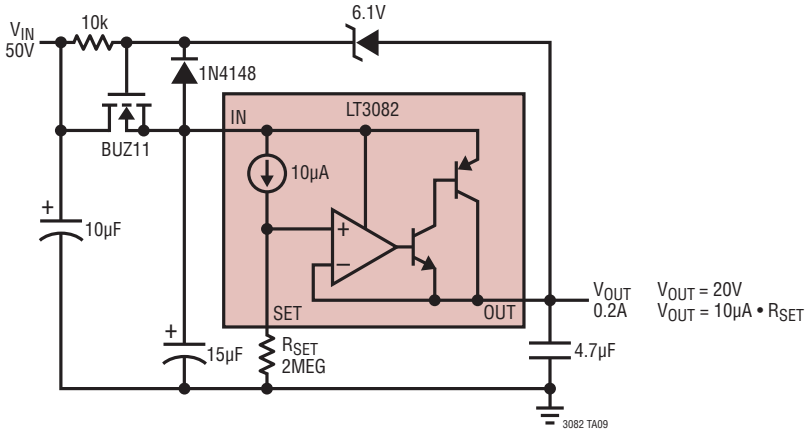


*Q2 INSURES ZERO OUTPUT IN THE ABSENCE OF ANY OUTPUT LOAD.

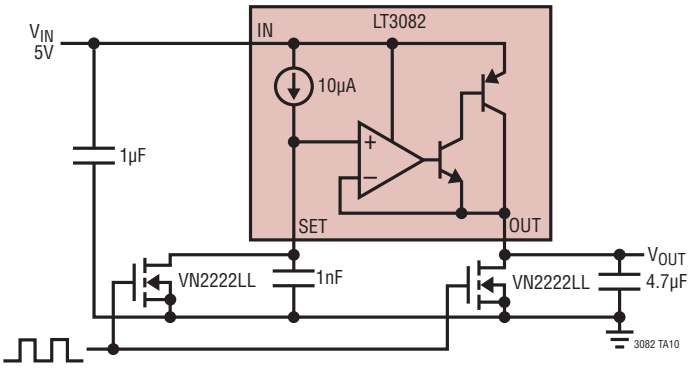
Reference Buffer



High Voltage Regulator

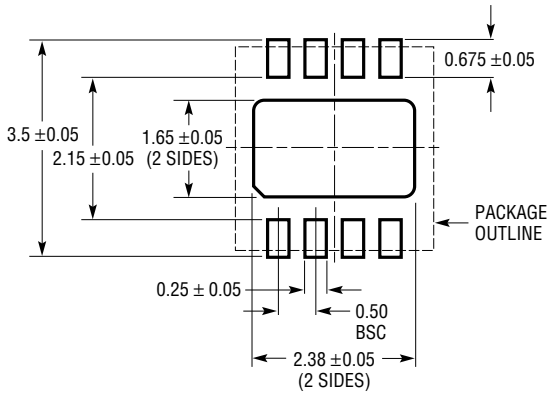


Ramp Generator

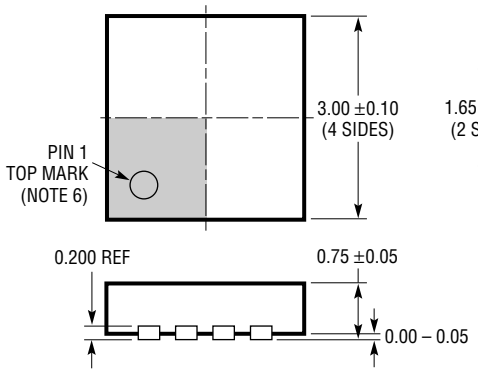


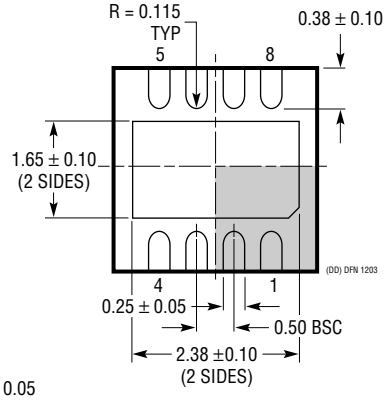
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



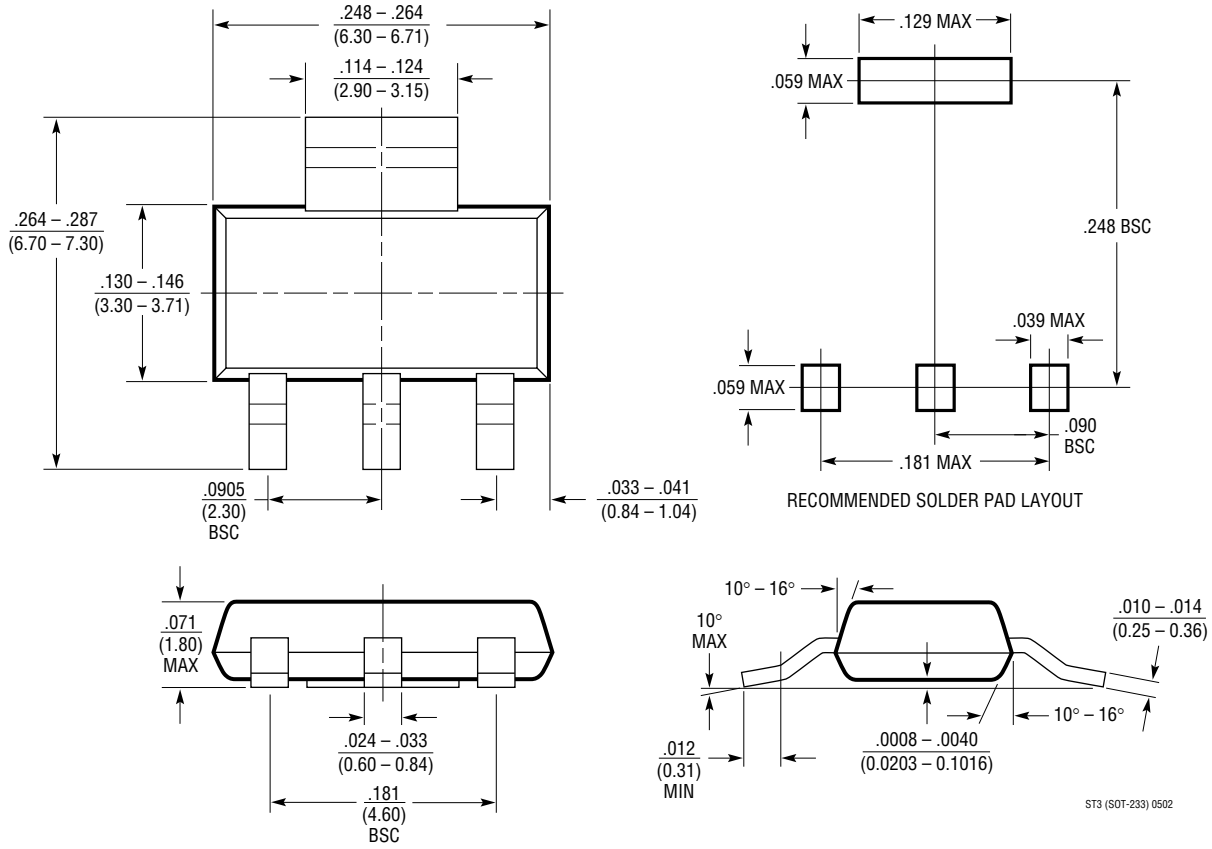


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

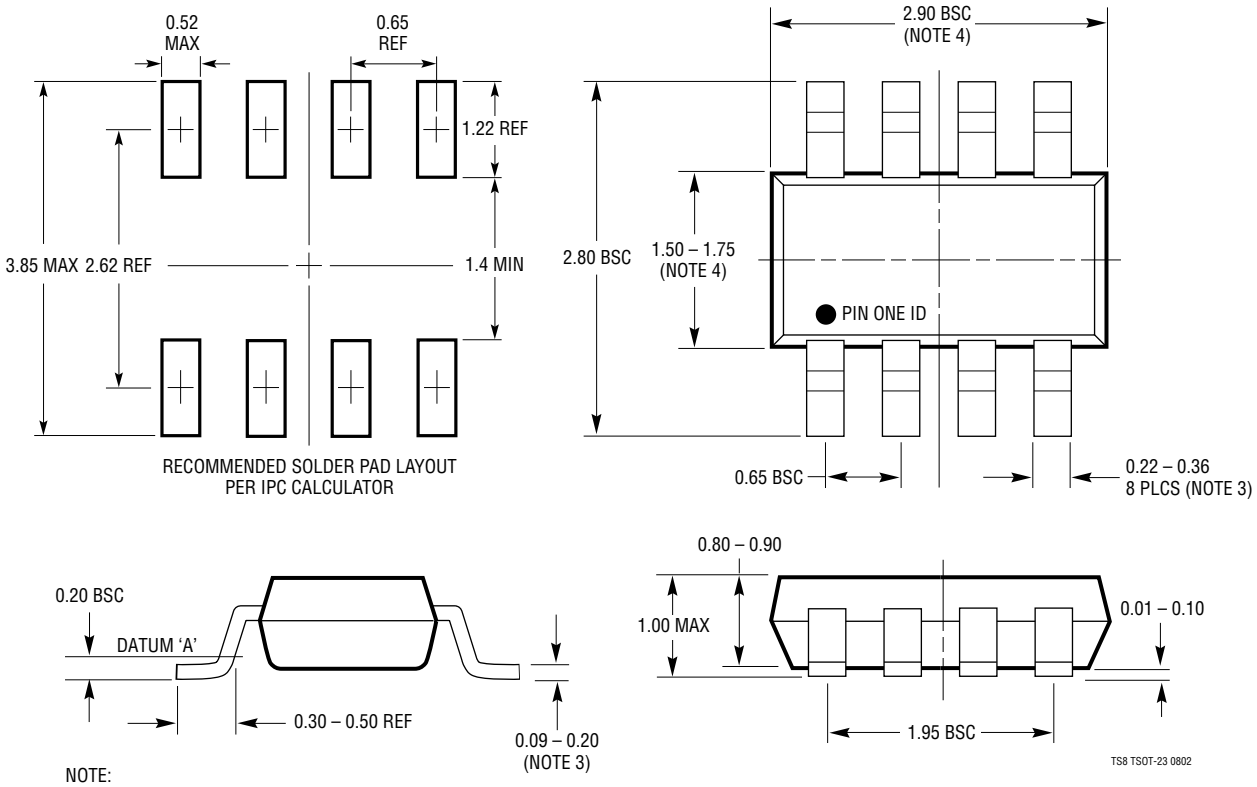
PACKAGE DESCRIPTION

ST Package
3-Lead Plastic SOT-223
(Reference LTC DWG # 05-08-1630)



PACKAGE DESCRIPTION

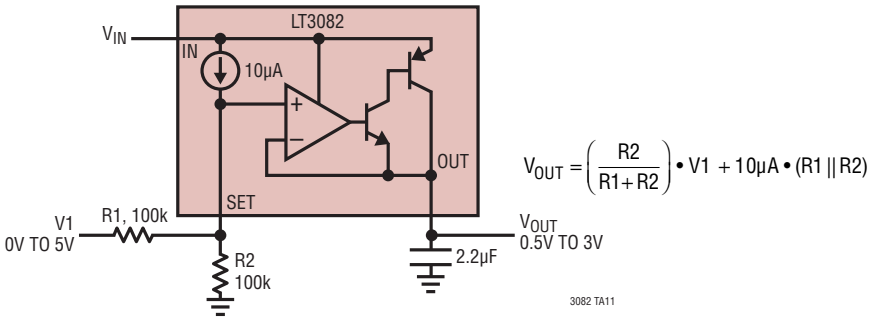
TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

TYPICAL APPLICATIONS

Active-Driven Regulator



$$V_{OUT} = \left(\frac{R2}{R1+R2}\right) \bullet V1 + 10\mu A \bullet (R1 \,||\, R2)$$

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1761	100mA, Low Noise LDO	300mV Dropout Voltage, Low Noise = 20µV_{RMS}, V_{IN}: 1.8V to 20V, ThinSOT™ Package
LT1762	150mA, Low Noise LDO	300mV Dropout Voltage, Low Noise = 20µV_{RMS}, V_{IN}: 1.8V to 20V, MS-8 Package
LT1763	500mA, Low Noise LDO	300mV Dropout Voltage, Low Noise = 20µV_{RMS}, V_{IN}: 1.8V to 20V, SO-8 Package
LT1962	300mA, Low Noise LDO	270mV Dropout Voltage, Low Noise = 20µV_{RMS}, V_{IN}: 1.8V to 20V, MS-8 Package
LT1964	200mA, Low Noise, Negative LDO	340mV Dropout Voltage, Low Noise = 30µV_{RMS}, V_{IN}: –1.8V to –20V, ThinSOT Package
LT3008	20mA, 45V, 3µA I_Q Micropower LDO	280mV Dropout Voltage, Low I_Q = 3µA, V_{IN}: 2V to 45V, V_{OUT}: 0.6V to 39.5V; ThinSOT and 2mm × 2mm DFN-6 Packages
LT3009	20mA, 3µA I_Q Micropower LDO	280mV Dropout Voltage, Low I_Q = 3µA, V_{IN}: 1.6V to 20V, V_{OUT}: 0.6V to 19.5V; ThinSOT and SC-70 Packages
LT3010	50mA, High Voltage, Micropower LDO	V_{IN}: 3V to 80V, V_{OUT}: 1.275V to 60V, V_{DO} = 0.3V, I_Q = 30µA, I_{SD} <1µA, Low Noise <100µV_{RMS}, Stable with 1µF Output Capacitor, Exposed MS8 Package
LT3011	50mA, High Voltage, Micropower LDO with Power Good	V_{IN}: 3V to 80V, V_{OUT}: 1.275V to 60V, V_{DO} = 0.3V, I_Q = 46µA, I_{SD} <1µA, Low Noise <100µV_{RMS}, Power Good, Stable with 1µF Output Capacitor, 3mm × 3mm DFN-10 and Exposed MS-12E Packages
LT3012	250mA, 4V to 80V, Low Dropout Micropower Linear Regulator	V_{IN}: 4V to 80V, V_{OUT}: 1.24V to 60V, V_{DO} = 0.4V, I_Q = 40µA, I_{SD} <1µA, TSSOP-16E and 4mm × 3mm DFN-12 Packages
LT3013	250mA, 4V to 80V, Low Dropout Micro-power Linear Regulator with PWRGD	V_{IN}: 4V to 80V, V_{OUT}: 1.24V to 60V, V_{DO} = 0.4V, I_Q = 65µA, I_{SD} <1µA, Power Good; TSSOP-16E and 4mm × 3mm DFN-12 Packages
LT3014/LT3014HV	20mA, 3V to 80V, Low Dropout Micropower Linear Regulator	V_{IN}: 3V to 80V (100V for 2ms, HV Version), V_{OUT}: 1.22V to 60V, V_{DO} = 0.35V, I_Q = 7µA, I_{SD} <1µA, ThinSOT and 3mm × 3mm DFN-8 Packages
LT3020	100mA, Low Voltage VLDO Linear Regulator	V_{IN}: 0.9V to 10V, V_{OUT}: 0.2V to 5V (Min), V_{DO} = 0.15V, I_Q = 120µA, Noise <250µV_{RMS}, Stable with 2.2µF Ceramic Capacitors, DFN-8 and MS-8 Packages
LT3021	500mA, Low Voltage, Very Low Dropout VLDO Linear Regulator	V_{IN}: 0.9V to 10V, Dropout Voltage = 160mV (Typical), Adjustable Output (V_{REF} = $V_{OUT(MIN)}$ = 200mV), Fixed Output Voltages: 1.2V, 1.5V, 1.8V, Stable with Low ESR, Ceramic Output Capacitors 16-Pin 5mm × 5mm DFN and 8-Lead SO Packages
LT3080/LT3080-1	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2-Supply Operation), Low Noise = 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors; TO-220, SOT-223, MSOP-8 and 3mm × 3mm DFN-8 Packages; LT3080-1 Version Has Integrated Internal Ballast Resistor
LT3085	500mA, Parallelable, Low Noise, Low Dropout Linear Regulator	275mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors; MSOP-8 and 2mm × 3mm DFN-6 Packages

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