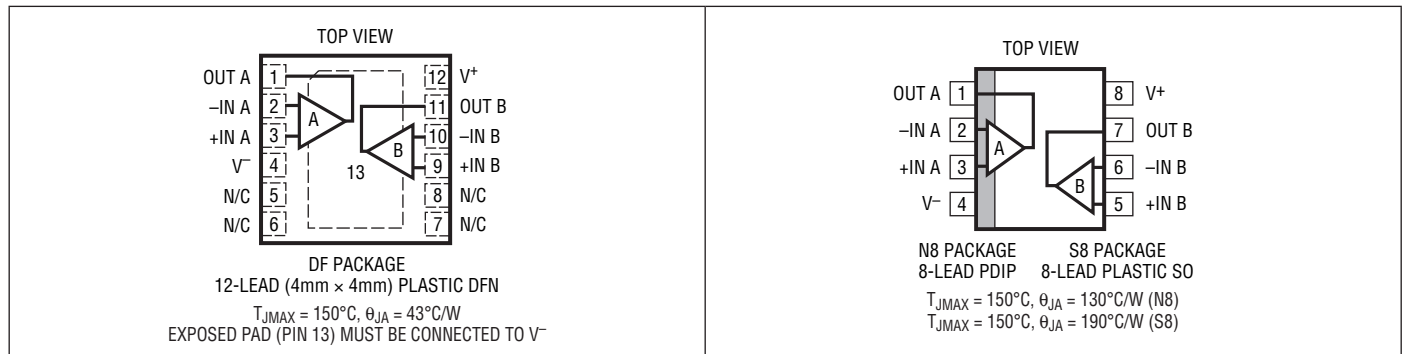


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-).....	36V	Specified Temperature Range (Note 5)	-40°C to 85°C
Input Current (Note 2).....	$\pm 10\text{mA}$	Maximum Junction Temperature.....	150°C
Output Short-Circuit Duration (Note 3)	Indefinite	Storage Temperature Range.....	-65°C to 150°C
Operating Temperature Range (Note 4)....	-40°C to 85°C	Lead Temperature (Soldering, 10 sec)	
		S8 and N8 Package.....	300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1469CN8#PBF	NA	LT1469CN8	8-Lead PDIP	0°C to 70°C
LT1469IN8#PBF	NA	LT1469IN8	8-Lead PDIP	-40°C to 85°C
LT1469CS8#PBF	LT1469CS8#TRPBF	1469	8-Lead Plastic Small Outline	0°C to 70°C
LT1469IS8#PBF	LT1469IS8#TRPBF	1469I	8-Lead Plastic Small Outline	-40°C to 85°C
LT1469ACDF#PBF	LT1469ACDF#TRPBF	1469	12-Lead (4mm × 4mm) Plastic DFN	0°C to 70°C
LT1469AIDF#PBF	LT1469AIDF#TRPBF	1469	12-Lead (4mm × 4mm) Plastic DFN	-40°C to 85°C
LT1469CDF#PBF	LT1469CDF#TRPBF	1469	12-Lead (4mm × 4mm) Plastic DFN	0°C to 70°C
LT1469IDF#PBF	LT1469IDF#TRPBF	1469	12-Lead (4mm × 4mm) Plastic DFN	-40°C to 85°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1469CN8	NA	LT1469CN8	8-Lead PDIP	0°C to 70°C
LT1469IN8	NA	LT1469IN8	8-Lead PDIP	-40°C to 85°C
LT1469CS8	LT1469CS8#TR	1469	8-Lead Plastic Small Outline	0°C to 70°C
LT1469IS8	LT1469IS8#TR	1469I	8-Lead Plastic Small Outline	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V _{SUPPLY}	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	N8, S8 Packages	±15V ±5V	50 50	125 200		μV μV
		LT1469A, DF Package	±15V ±5V	50 50	125 200		μV μV
		LT1469, DF Package	±15V ±5V	100 150	225 300		μV μV
I _{OS}	Input Offset Current		±5V to ±15V	13	±50		nA
I _{B−}	Inverting Input Bias Current		±5V to ±15V	3	±10		nA
I _{B+}	Noninverting Input Bias Current		±5V to ±15V	−10	±40		nA
	Input Noise Voltage	0.1Hz to 10Hz	±5V to ±15V	0.3			μV _{P-P}
e _n	Input Noise Voltage Density	f = 10kHz	±5V to ±15V	5			nV/√Hz
i _n	Input Noise Current Density	f = 10kHz	±5V to ±15V	0.6			pA/√Hz
R _{IN}	Input Resistance	Common Mode, V _{CM} = ±12.5V Differential	±15V ±15V	100 50	240 150		MΩ kΩ
C _{IN}	Input Capacitance		±15V	4			pF
V _{CM}	Input Voltage Range (Positive)	Guaranteed by CMRR	±15V ±5V	12.5 2.5	13.5 3.6		V V
	Input Voltage Range (Negative)	Guaranteed by CMRR	±15V ±5V		−14.3 −4.4	−12.5 −2.5	V V
CMRR	Common Mode Rejection Ratio	V _{CM} = ±12.5V	±15V	96	110		dB
		V _{CM} = ±2.5V	±5V	96	112		dB
	Minimum Supply Voltage	Guaranteed by PSRR		±2.5	±4.5		V
PSRR	Power Supply Rejection Ratio	V _S = ±4.5V to ±15V		100	112		dB
A _{VOL}	Large-Signal Voltage Gain	V _{OUT} = ±12.5V, R _L = 10k	±15V	300	2000		V/mV
		V _{OUT} = ±12.5V, R _L = 2k	±15V	300	2000		V/mV
		V _{OUT} = ±2.5V, R _L = 10k	±5V	200	8000		V/mV
		V _{OUT} = ±2.5V, R _L = 2k	±5V	200	8000		V/mV
V _{OUT}	Maximum Output Swing	R _L = 10k	±15V	±13.0	±13.6		V
		R _L = 2k	±15V	±12.8	±13.5		V
		R _L = 10k	±5V	±3.0	±3.7		V
		R _L = 2k	±5V	±2.8	±3.6		V
I _{OUT}	Maximum Output Current	V _{OUT} = ±12.5V	±15V	±15	±22		mA
		V _{OUT} = ±2.5V	±5V	±15	±22		mA
I _{SC}	Output Short-Circuit Current	V _{OUT} = 0V, 0.2V Overdrive (Note 3)	±15V	±25	±40		mA
SR	Slew Rate	A _V = −10, R _L = 2k (Note 6)	±15V	15	22		V/μs
			±5V	11	17		V/μs
FPBW	Full-Power Bandwidth	10V Peak, (Note 7)	±15V		350		kHz
		3V Peak, (Note 7)	±5V		900		kHz
GBW	Gain Bandwidth Product	f = 100kHz, R _L = 2k	±15V	60	90		MHz
			±5V	55	88		MHz
t _r , t _f	Rise Time, Fall Time	A _V = 1, 10% to 90%, 0.1V Step	±15V		11		ns
			±5V		12		ns
OS	Overshoot	A _V = 1, 0.1V Step	±15V		30		%
			±5V		35		%
t _{PD}	Propagation Delay	A _V = 1, 50% V _{IN} to 50% V _{OUT} , 0.1V Step	±15V		9		ns
			±5V		10		ns

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$. $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
t_S	Settling Time	10V Step, 0.01%, $A_V = -1$	$\pm 15\text{V}$		760		ns
		10V Step, $150\mu\text{V}$, $A_V = -1$	$\pm 15\text{V}$		900		ns
		5V Step, 0.01%, $A_V = -1$	$\pm 5\text{V}$		770		ns
THD	Total Harmonic Distortion	$A_V = -1$, $V_{OUT} = 10\text{V}_{P-P}$, $f = 100\text{kHz}$	$\pm 15\text{V}$		-96.5		dB
		$A_V = 1$, $V_{OUT} = 20\text{V}_{P-P}$, $f = 1\text{kHz}$	$\pm 15\text{V}$		-125		dB
R_{OUT}	Output Resistance	$A_V = 1$, $f = 100\text{kHz}$	$\pm 15\text{V}$		0.02		Ω
	Channel Separation	$V_{OUT} = \pm 12.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	100	130		dB
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	100	130		dB
I_S	Supply Current	Per Amplifier	$\pm 15\text{V}$		4.1	5.2	mA
			$\pm 5\text{V}$		3.8	5	mA
ΔV_{OS}	Input Offset Voltage Match	S8, DF A-Grade	$\pm 15\text{V}$		30	225	μV
			$\pm 5\text{V}$		50	350	μV
ΔI_{B-}	Inverting Input Bias Current Match		$\pm 5\text{V}$ to $\pm 15\text{V}$		2	18	nA
ΔI_{B+}	Noninverting Input Bias Current Match		$\pm 5\text{V}$ to $\pm 15\text{V}$		5	78	nA
ΔCMRR	Common Mode Rejection Match	$V_{CM} = \pm 12.5\text{V}$ (Note 9)	$\pm 15\text{V}$	93	113		dB
		$V_{CM} = \pm 2.5\text{V}$ (Note 9)	$\pm 5\text{V}$	93	115		dB
ΔPSRR	Power Supply Rejection Match	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$ (Note 9)		97	115		dB

The ● denotes the specifications which apply over the full operating temperature range, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$. $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	N8, S8 Packages	$\pm 15\text{V}$	●		350	μV
			$\pm 5\text{V}$	●		350	μV
		LT1469A, DF Package	$\pm 15\text{V}$	●		225	μV
			$\pm 5\text{V}$	●		275	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 8)	$\pm 15\text{V}$	●		450	$\mu\text{V}/^\circ\text{C}$
			$\pm 5\text{V}$	●		450	$\mu\text{V}/^\circ\text{C}$
			$\pm 15\text{V}$	●	1	5	$\mu\text{V}/^\circ\text{C}$
			$\pm 5\text{V}$	●	1	3	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●		± 80	nA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 8)	$\pm 5\text{V}$ to $\pm 15\text{V}$	●	60		$\text{pA}/^\circ\text{C}$
I_{B-}	Inverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●		± 20	nA
$\Delta I_{B-}/\Delta T$	Inverting Input Bias Current Drift	(Note 8)	$\pm 5\text{V}$ to $\pm 15\text{V}$	●	40		$\text{pA}/^\circ\text{C}$
I_{B+}	Noninverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●		± 60	nA
V_{CM}	Input Voltage Range (Positive)	Guaranteed by CMRR	$\pm 15\text{V}$	●	12.5		V
			$\pm 5\text{V}$	●	2.5		V
	Input Voltage Range (Negative)	Guaranteed by CMRR	$\pm 15\text{V}$	●		-12.5	V
			$\pm 5\text{V}$	●		-2.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12.5\text{V}$	$\pm 15\text{V}$	●	94		dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	94		dB
	Minimum Supply Voltage	Guaranteed by PSRR		●		± 4.5	V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$		●	95		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12.5\text{V}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	●	100		V/mV
		$V_{OUT} = \pm 12.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	100		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 10\text{k}$	$\pm 5\text{V}$	●	100		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	●	100		V/mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$. $V_{\text{CM}} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OUT}	Maximum Output Swing	$R_L = 10\text{k}$	$\pm 15\text{V}$	●	± 12.9			V
		$R_L = 2\text{k}$	$\pm 15\text{V}$	●	± 12.7			V
		$R_L = 10\text{k}$	$\pm 5\text{V}$	●	± 2.9			V
		$R_L = 2\text{k}$	$\pm 5\text{V}$	●	± 2.7			V
I_{OUT}	Maximum Output Current	$V_{\text{OUT}} = \pm 12.5\text{V}$	$\pm 15\text{V}$	●	± 12.5			mA
		$V_{\text{OUT}} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	± 12.5			mA
I_{SC}	Output Short-Circuit Current	$V_{\text{OUT}} = 0\text{V}$, 0.2V Overdrive (Note 3)	$\pm 15\text{V}$	●	± 17			mA
SR	Slew Rate	$A_V = -10$, $R_L = 2\text{k}$ (Note 6)	$\pm 15\text{V}$	●	13			V/ μs
			$\pm 5\text{V}$	●	9			V/ μs
GBW	Gain Bandwidth Product	$f = 100\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	55			MHz
			$\pm 5\text{V}$	●	50			MHz
	Channel Separation	$V_{\text{OUT}} = \pm 12.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	98			dB
		$V_{\text{OUT}} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	●	98			dB
I_S	Supply Current	Per Amplifier	$\pm 15\text{V}$	●			6.5	mA
			$\pm 5\text{V}$	●			6.3	mA
ΔV_{OS}	Input Offset Voltage Match	S8, DF A-Grade	$\pm 15\text{V}$	●			600	μV
			$\pm 5\text{V}$	●			600	μV
$\Delta I_{\text{B-}}$	Inverting Input Bias Current Match		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			38	nA
$\Delta I_{\text{B+}}$	Noninverting Input Bias Current Match		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			118	nA
ΔCMRR	Common Mode Rejection Match	$V_{\text{CM}} = \pm 12.5\text{V}$ (Note 9)	$\pm 15\text{V}$	●	91			dB
		$V_{\text{CM}} = \pm 2.5\text{V}$ (Note 9)	$\pm 5\text{V}$	●	91			dB
ΔPSRR	Power Supply Rejection Match	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$ (Note 9)		●	92			dB

The ● denotes the specifications which apply over the full operating temperature range, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{\text{CM}} = 0\text{V}$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	N8, S8 Packages	$\pm 15\text{V}$	●			500	μV
			$\pm 5\text{V}$	●			500	μV
		LT1469A, DF Package	$\pm 15\text{V}$	●			300	μV
			$\pm 5\text{V}$	●			350	μV
		LT1469, DF Package	$\pm 15\text{V}$	●			600	μV
			$\pm 5\text{V}$	●			600	μV
$\Delta V_{\text{OS}}/\Delta T$	Input Offset Voltage Drift	(Note 8)	$\pm 15\text{V}$	●		1	6	$\mu\text{V}/^{\circ}\text{C}$
			$\pm 5\text{V}$	●		1	5	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 120	nA
$\Delta I_{\text{OS}}/\Delta T$	Input Offset Current Drift	(Note 8)	$\pm 5\text{V}$ to $\pm 15\text{V}$	●		120		$\text{pA}/^{\circ}\text{C}$
$I_{\text{B-}}$	Inverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 40	nA
$\Delta I_{\text{B-}}/\Delta T$	Inverting Input Bias Current Drift	(Note 8)	$\pm 5\text{V}$ to $\pm 15\text{V}$	●		80		$\text{pA}/^{\circ}\text{C}$
$I_{\text{B+}}$	Noninverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 80	nA
V_{CM}	Input Voltage Range (Positive)	Guaranteed by CMRR	$\pm 15\text{V}$	●	12.5			V
			$\pm 5\text{V}$	●	2.5			V
	Input Voltage Range (Negative)	Guaranteed by CMRR	$\pm 15\text{V}$	●			-12.5	V
			$\pm 5\text{V}$	●			-2.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{\text{CM}} = 0\text{V}$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = \pm 12.5\text{V}$	$\pm 15\text{V}$	●	92			dB
		$V_{\text{CM}} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	92			dB
	Minimum Supply Voltage	Guaranteed by PSRR		●			± 4.5	V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$		●	93			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{\text{OUT}} = \pm 12.5\text{V}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	●	75			V/mV
		$V_{\text{OUT}} = \pm 12.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	75			V/mV
		$V_{\text{OUT}} = \pm 2.5\text{V}$, $R_L = 10\text{k}$	$\pm 5\text{V}$	●	75			V/mV
		$V_{\text{OUT}} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	●	75			V/mV
V_{OUT}	Maximum Output Swing	$R_L = 10\text{k}$	$\pm 15\text{V}$	●	± 12.8			V
		$R_L = 2\text{k}$	$\pm 15\text{V}$	●	± 12.6			V
		$R_L = 10\text{k}$	$\pm 5\text{V}$	●	± 2.8			V
		$R_L = 2\text{k}$	$\pm 5\text{V}$	●	± 2.6			V
I_{OUT}	Maximum Output Current	$V_{\text{OUT}} = \pm 12.5\text{V}$	$\pm 15\text{V}$	●	± 7			mA
		$V_{\text{OUT}} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	± 7			mA
I_{SC}	Output Short-Circuit Current	$V_{\text{OUT}} = 0\text{V}$, 0.2V Overdrive (Note 3)	$\pm 15\text{V}$	●	± 12			mA
SR	Slew Rate	$A_V = -10$, $R_L = 2\text{k}$ (Note 6)	$\pm 15\text{V}$	●	9			V/ μs
			$\pm 5\text{V}$	●	6			V/ μs
GBW	Gain Bandwidth Product	$f = 100\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	45			MHz
			$\pm 5\text{V}$	●	40			MHz
	Channel Separation	$V_{\text{OUT}} = \pm 12.5\text{V}$, $R_L = 2\text{k}$ $V_{\text{OUT}} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	96			dB
			$\pm 5\text{V}$	●	96			dB
I_S	Supply Current	Per Amplifier	$\pm 15\text{V}$	●			7	mA
			$\pm 5\text{V}$	●			6.8	mA
ΔV_{OS}	Input Offset Voltage Match	S8, DF A-Grade	$\pm 15\text{V}$	●			800	μV
			$\pm 5\text{V}$	●			800	μV
ΔI_{B-}	Inverting Input Bias Current Match		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			78	nA
ΔI_{B+}	Noninverting Input Bias Current Match		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			158	nA
ΔCMRR	Common Mode Rejection Match	$V_{\text{CM}} = \pm 12.5\text{V}$ (Note 9)	$\pm 15\text{V}$	●	89			dB
		$V_{\text{CM}} = \pm 2.5\text{V}$ (Note 9)	$\pm 5\text{V}$	●	89			dB
ΔPSRR	Power Supply Rejection Match	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$ (Note 9)		●	90			dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes and two 100Ω series resistors. If the differential input voltage exceeds 0.7V, the input current should be limited to less than 10mA. Input voltages outside the supplies will be clamped by ESD protection devices and input currents should also be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: The LT1469C and LT1469I are guaranteed functional over the operating temperature range of -40°C to 85°C .

Note 5: The LT1469C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet specified performance from -40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1469I is guaranteed to meet specified performance from -40°C to 85°C .

Note 6: Slew rate is measured between $\pm 8\text{V}$ on the output with $\pm 12\text{V}$ swing for $\pm 15\text{V}$ supplies and $\pm 2\text{V}$ on the output with $\pm 3\text{V}$ swing for $\pm 5\text{V}$ supplies.

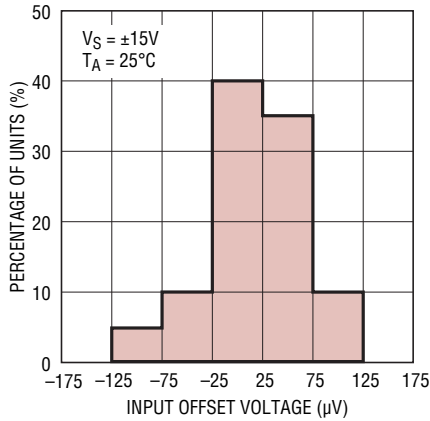
Note 7: Full-power bandwidth is calculated from the slew rate. $\text{FPBW} = \text{SR}/2\pi V_p$.

Note 8: This parameter is not 100% tested.

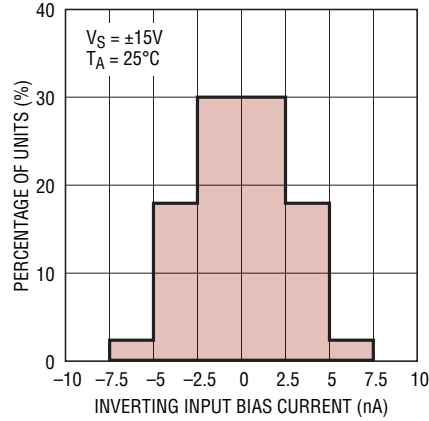
Note 9: ΔCMRR and ΔPSRR are defined as follows: 1) CMRR and PSRR are measured in $\mu\text{V/V}$ on each amplifier; 2) the difference between the two sides is calculated in $\mu\text{V/V}$; 3) the result is converted to dB.

TYPICAL PERFORMANCE CHARACTERISTICS

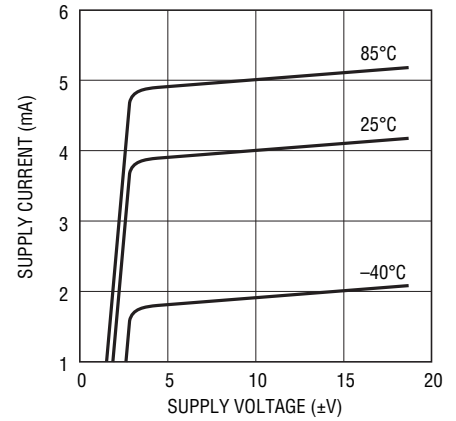
Distribution of Input Offset Voltage



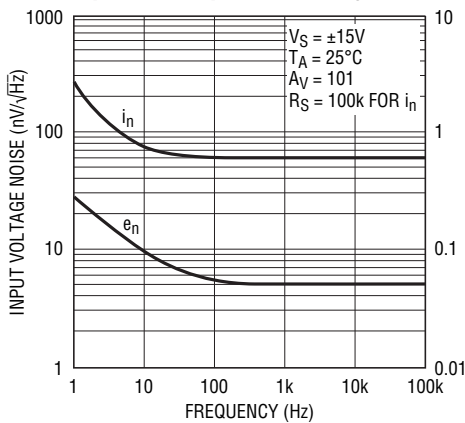
Distribution of Inverting Input Bias Current



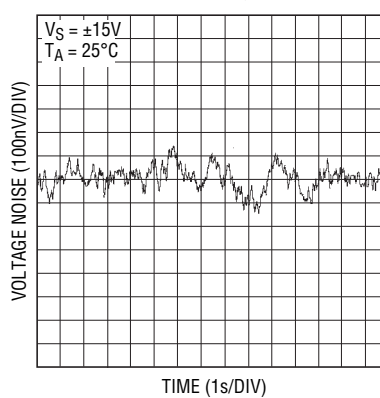
Supply Current vs Supply Voltage and Temperature



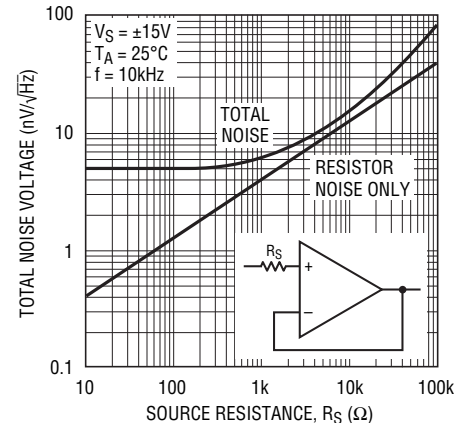
Input Noise Spectral Density



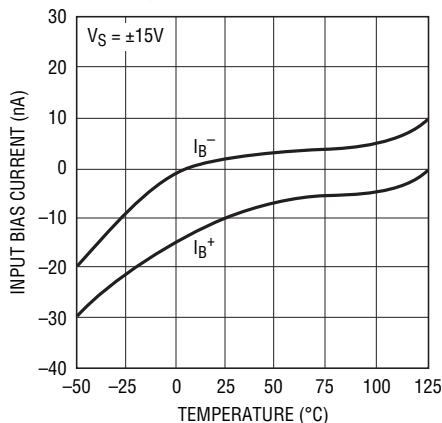
0.1Hz to 10Hz Voltage Noise



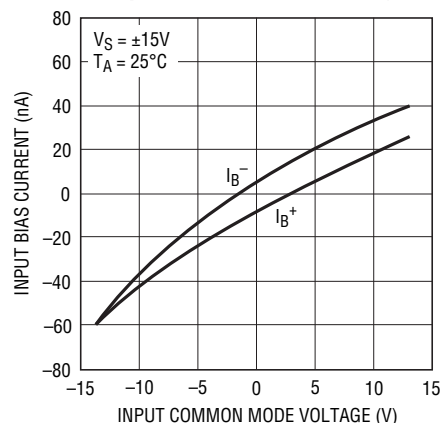
Total Noise vs Unmatched Source Resistance



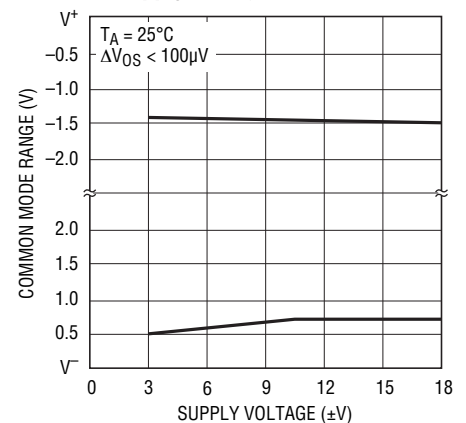
Input Bias Current vs Temperature



Input Bias Current vs Input Common Mode Voltage

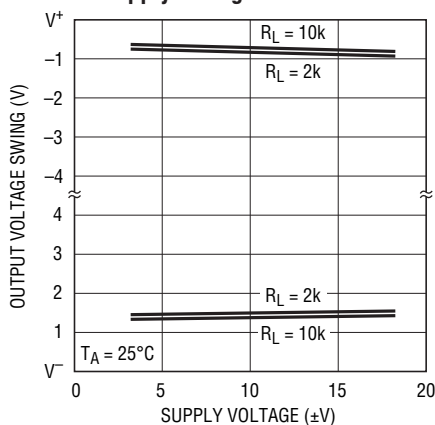


Input Common Mode Range vs Supply Voltage



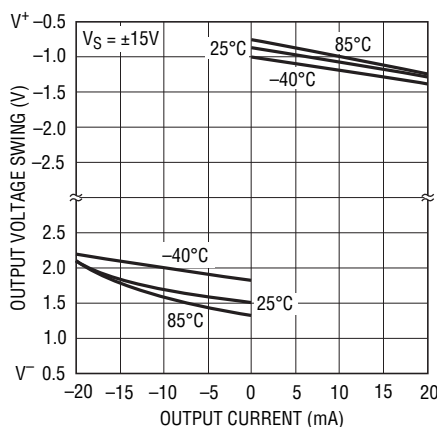
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Swing vs Supply Voltage



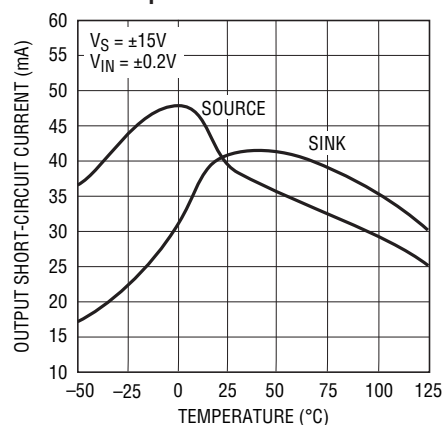
1469 G10

Output Voltage Swing vs Load Current



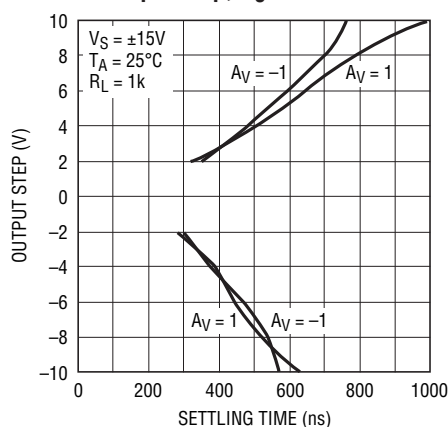
1469 G11

Output Short-Circuit Current vs Temperature



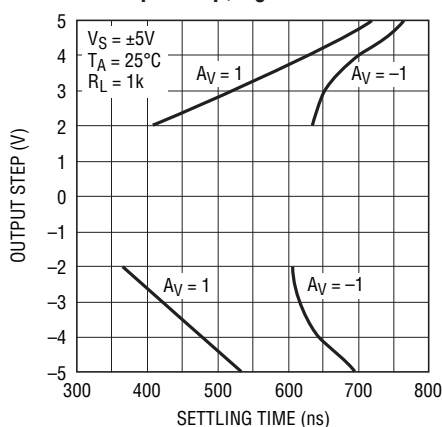
1469 G12

Settling Time to 0.01% vs Output Step, $V_S = \pm 15\text{V}$



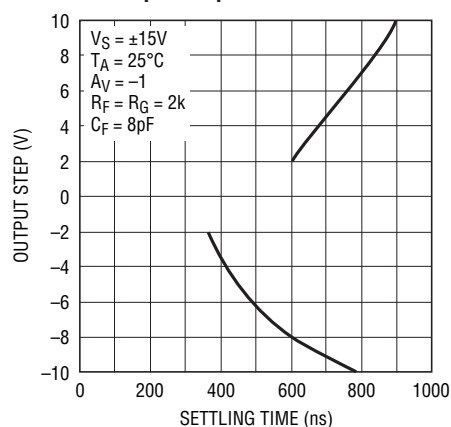
1469 G13

Settling Time to 0.01% vs Output Step, $V_S = \pm 5\text{V}$



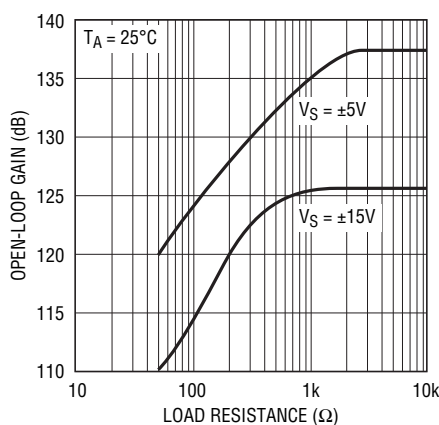
1469 G14

Settling Time to 150 μV vs Output Step



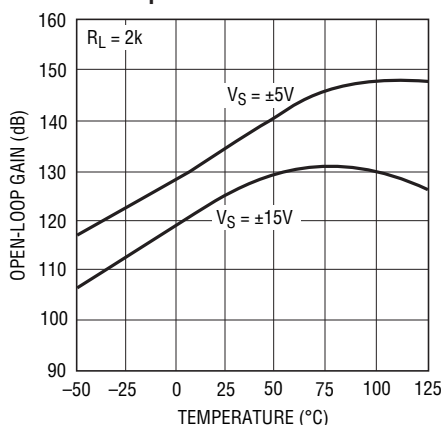
1469 G15

Open-Loop Gain vs Resistive Load



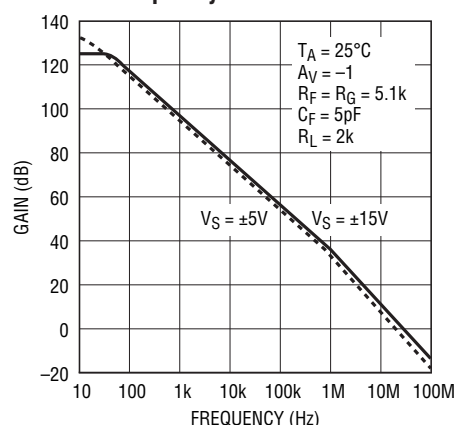
1469 G16

Open-Loop Gain vs Temperature



1469 G17

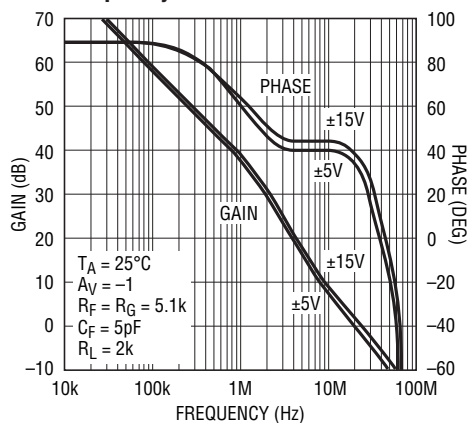
Open-Loop Gain vs Frequency



1469 G18

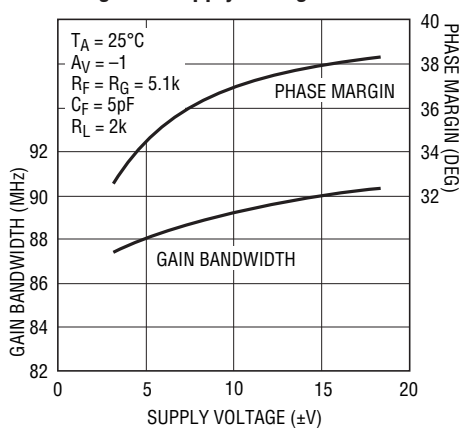
TYPICAL PERFORMANCE CHARACTERISTICS

Open-Loop Gain and Phase vs Frequency



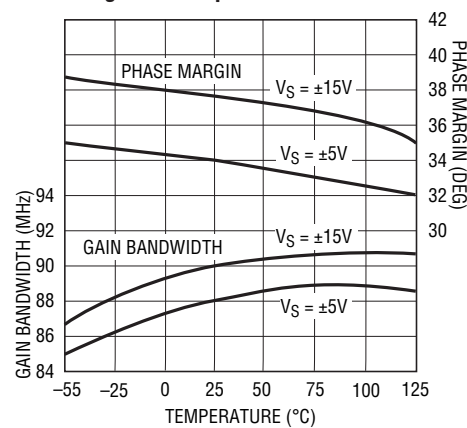
1469 G19

Gain Bandwidth and Phase Margin vs Supply Voltage



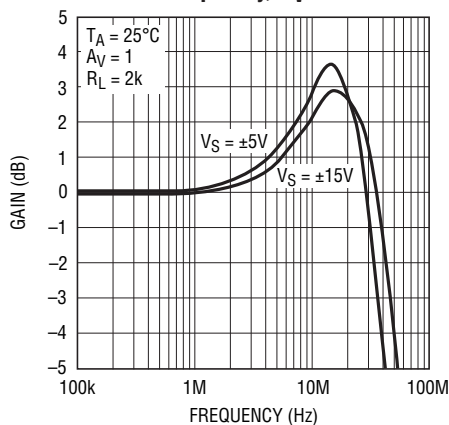
1469 G20

Gain Bandwidth and Phase Margin vs Temperature



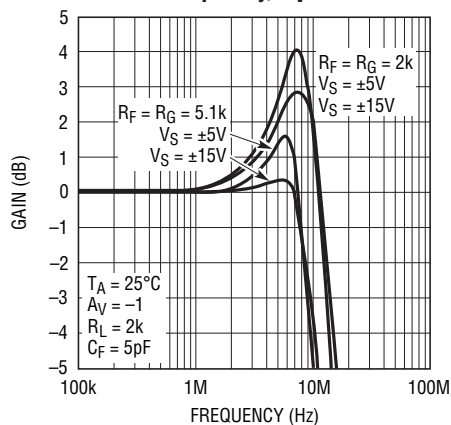
1469 G21

Gain vs Frequency, $A_V = 1$



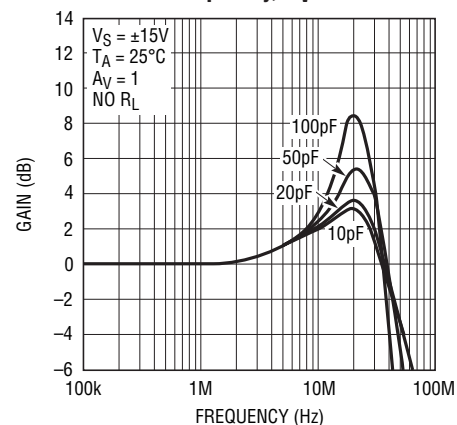
1469 G22

Gain vs Frequency, $A_V = -1$



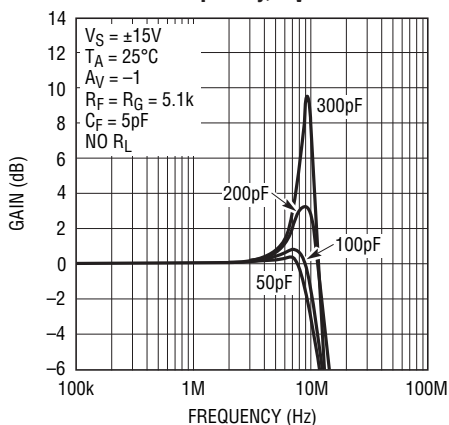
1469 G23

Gain vs Frequency, $A_V = 1$



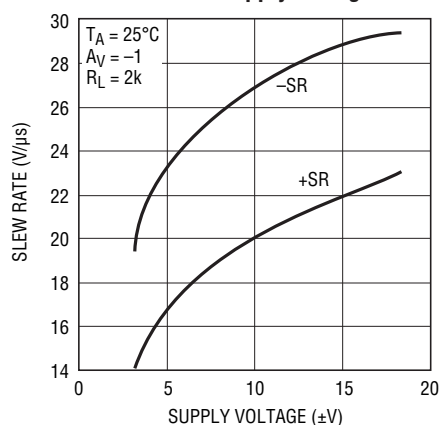
1469 G24

Gain vs Frequency, $A_V = -1$



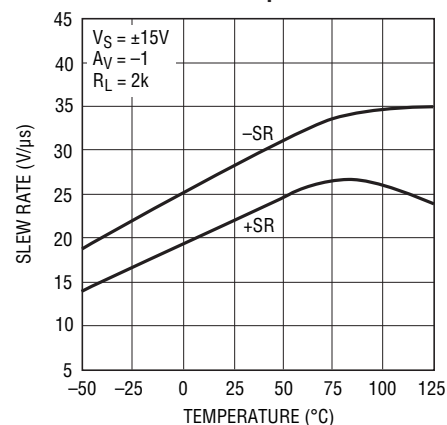
1469 G25

Slew Rate vs Supply Voltage



1469 G26

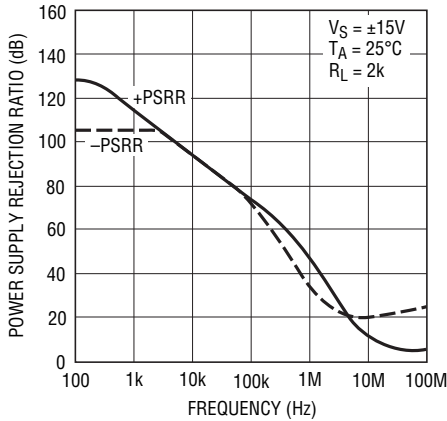
Slew Rate vs Temperature



1469 G27

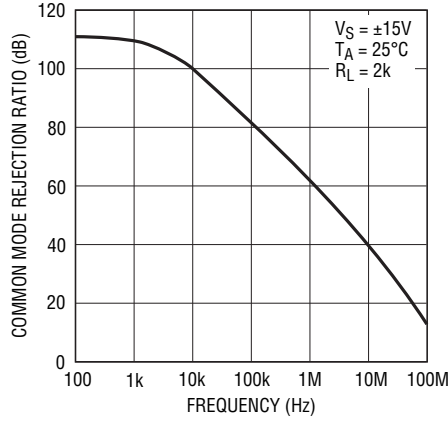
TYPICAL PERFORMANCE CHARACTERISTICS

Power Supply Rejection Ratio vs Frequency



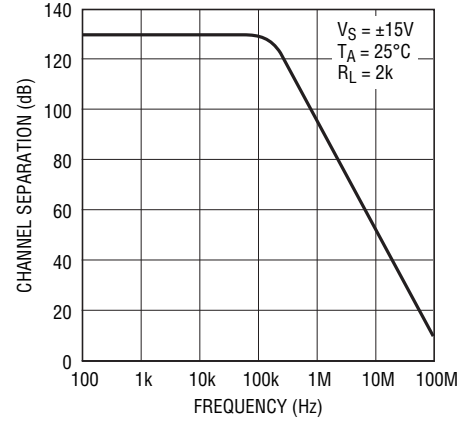
1469 G28

Common Mode Rejection Ratio vs Frequency



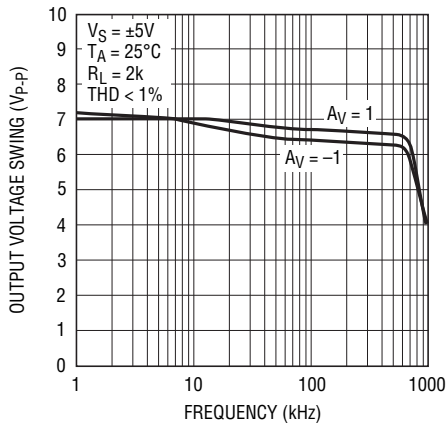
1469 G29

Channel Separation vs Frequency



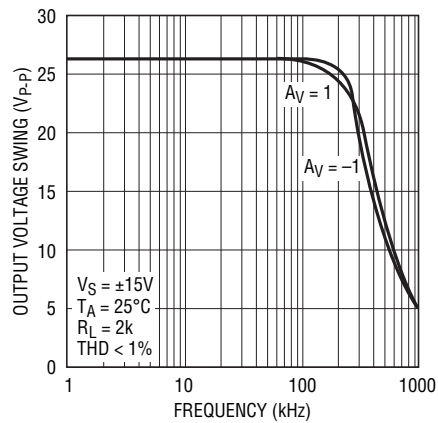
1469 G30

Undistorted Output Swing vs Frequency, $V_S = \pm 5V$



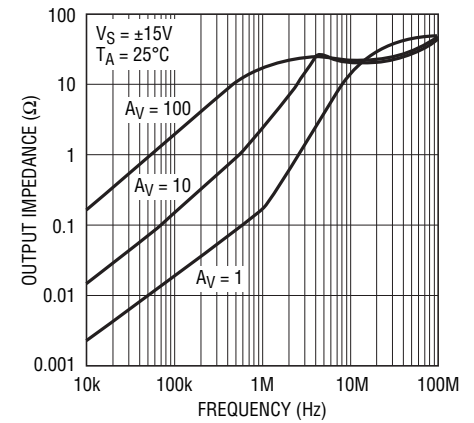
1469 G31

Undistorted Output Swing vs Frequency, $V_S = \pm 15V$



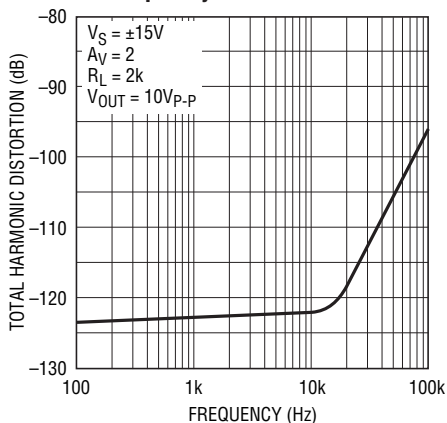
1469 G32

Output Impedance vs Frequency



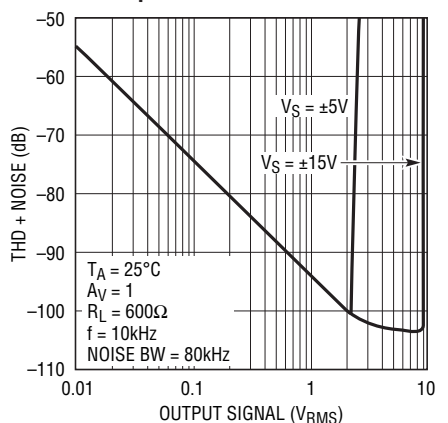
1469 G33

Total Harmonic Distortion vs Frequency



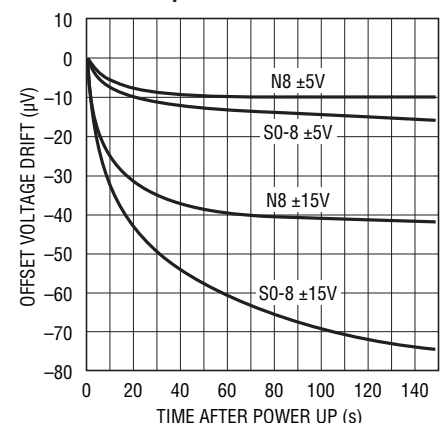
1469 G34

Total Harmonic Distortion + Noise vs Amplitude



1469 G35

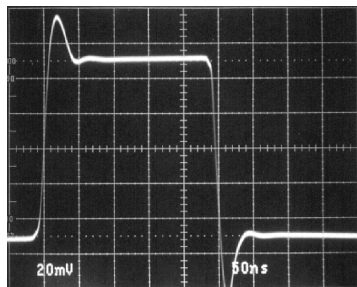
Warm-Up Drift vs Time



1469 G36

TYPICAL PERFORMANCE CHARACTERISTICS

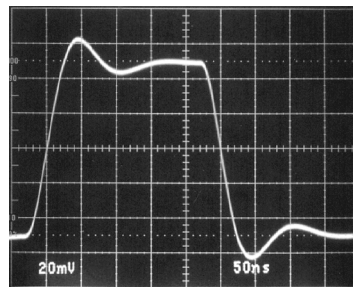
Small-Signal Transient, $A_V = 1$



$V_S = \pm 15V$

1469 G37

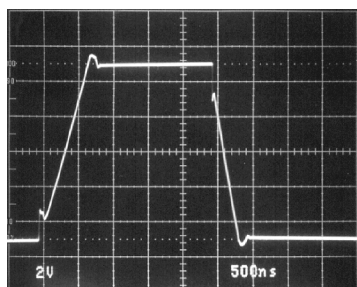
Small-Signal Transient, $A_V = -1$



$V_S = \pm 15V$

1469 G38

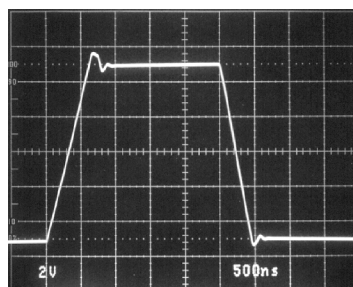
Large-Signal Transient, $A_V = 1$



$V_S = \pm 15V$

1469 G39

Large-Signal Transient, $A_V = -1$



$V_S = \pm 15V$

1469 G40

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1469 requires attention to detail in board layout in order to maximize DC and AC performance. For best AC results (for example, fast settling time) use a ground plane, short lead lengths and RF quality bypass capacitors (0.01 μ F to 0.1 μ F) in parallel with low ESR bypass capacitors (1 μ F to 10 μ F tantalum). For best DC performance, use “star” grounding techniques, equalize input trace lengths and minimize leakage (e.g., 1.5G Ω of leakage between an input and a 15V supply will generate 10nA—equal to the maximum I_B —specification).

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: for inverting configurations tie the ring to ground, in noninverting connections tie the ring to the inverting input (note the input capacitance will increase which may require a compensating capacitor as discussed below).

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the inputs can exceed the inherent drift of

APPLICATIONS INFORMATION

the amplifier. Air currents over device leads should be minimized, package leads should be short and the two input leads should be as close together as possible and maintained at the same temperature.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or even oscillations. For feedback resistors greater than 2k, a feedback capacitor of value $C_F > R_G \cdot C_{IN}/R_F$ should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one, and a large feedback resistor is used, C_F should be greater than or equal to C_{IN} . An example would be a DAC I-to-V converter as shown on the front page of the data sheet where the DAC can have many tens of picofarads of output capacitance. Another example would be a gain of -1 with 5k resistors; a 5pF to 10pF capacitor should be added across the feedback resistor.

Input Considerations

Each input of the LT1469 is protected with a 100Ω series resistor and back-to-back diodes across the bases of the input devices. If large differential input voltages are anticipated, limit the input current to less than 10mA with an external series resistor. Each input also has two ESD clamp diodes—one to each supply. If an input is driven beyond the supply, limit the current with an external resistor to less than 10mA.

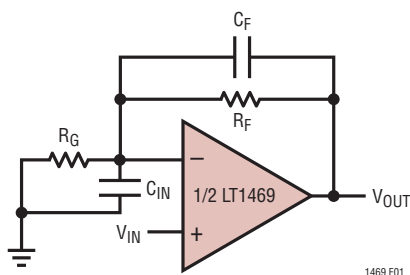


Figure 1. Nulling Input Capacitance

The LT1469 employs bias current cancellation at the inputs. The inverting input current is trimmed at zero common mode voltage to minimize errors in inverting applications such as I-to-V converters. The noninverting input current is not trimmed and has a wider variation and therefore a larger maximum value. As the input offset current can be greater than either input current, the use of balanced source resistance is NOT recommended as it actually degrades DC accuracy and also increases noise.

The input bias currents vary with common mode voltage. The cancellation circuitry was not designed to track this common mode voltage because the settling time would have been adversely affected.

The LT1469 inputs can be driven to the negative supply and to within 0.5V of the positive supply without phase reversal. As the input moves closer than 0.5V to the positive supply, the output reverses phase.

Total Input Noise

The total input noise of the LT1469 is optimized for a source resistance between 1k and 20k. Within this range, the total input noise is dominated by the noise of the source resistance itself. When the source resistance is below 1k, voltage noise of the amplifier dominates. When the source resistance is above 20k, the input noise current is the dominant contributor.

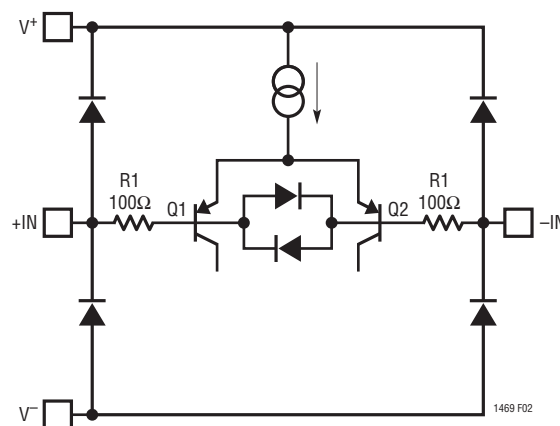


Figure 2. Input Stage Protection

APPLICATIONS INFORMATION

Capacitive Loading

The LT1469 drives capacitive loads of up to 100pF in unity-gain and 300pF in a gain of -1 . When there is a need to drive a larger capacitive load, a small series resistor should be inserted between the output and the load. In addition, a capacitor should be added between the output and the inverting input as shown in Figure 3.

Settling Time

The LT1469 is a single stage amplifier with an optimal thermal layout that leads to outstanding settling performance. Measuring settling even at the 12-bit level is very challenging, and at the 16-bit level requires a great deal of subtlety and expertise. Fortunately, there are two excellent Linear Technology reference sources for settling

measurements—Application Notes 47 and 74. Appendix B of AN47 is a vital primer on 12-bit settling measurements and AN74 extends the state-of-the-art while concentrating on settling time with a 16-bit current output DAC input.

The settling of the DAC I-to-V converter on the front page was measured using the exact methods of AN74. The optimum nulling of the DAC output capacitance requires 15pF across the 12k feedback resistor. The theoretical limit for 16-bit settling is 11.1 times this RC time constant or $2\mu\text{s}$. The actual settling time is $2.4\mu\text{s}$ at the output of the LT1469.

The RC output noise filter adds a slight settling time delay but reduces the noise bandwidth to 1.6MHz which increases the output resolution for 16-bit accuracy.

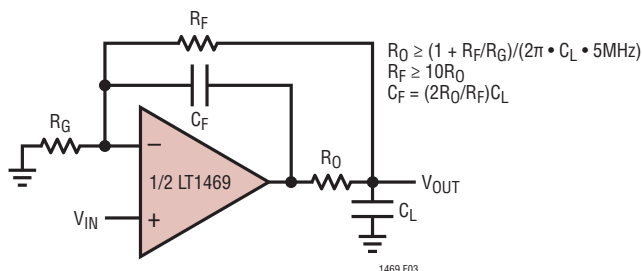
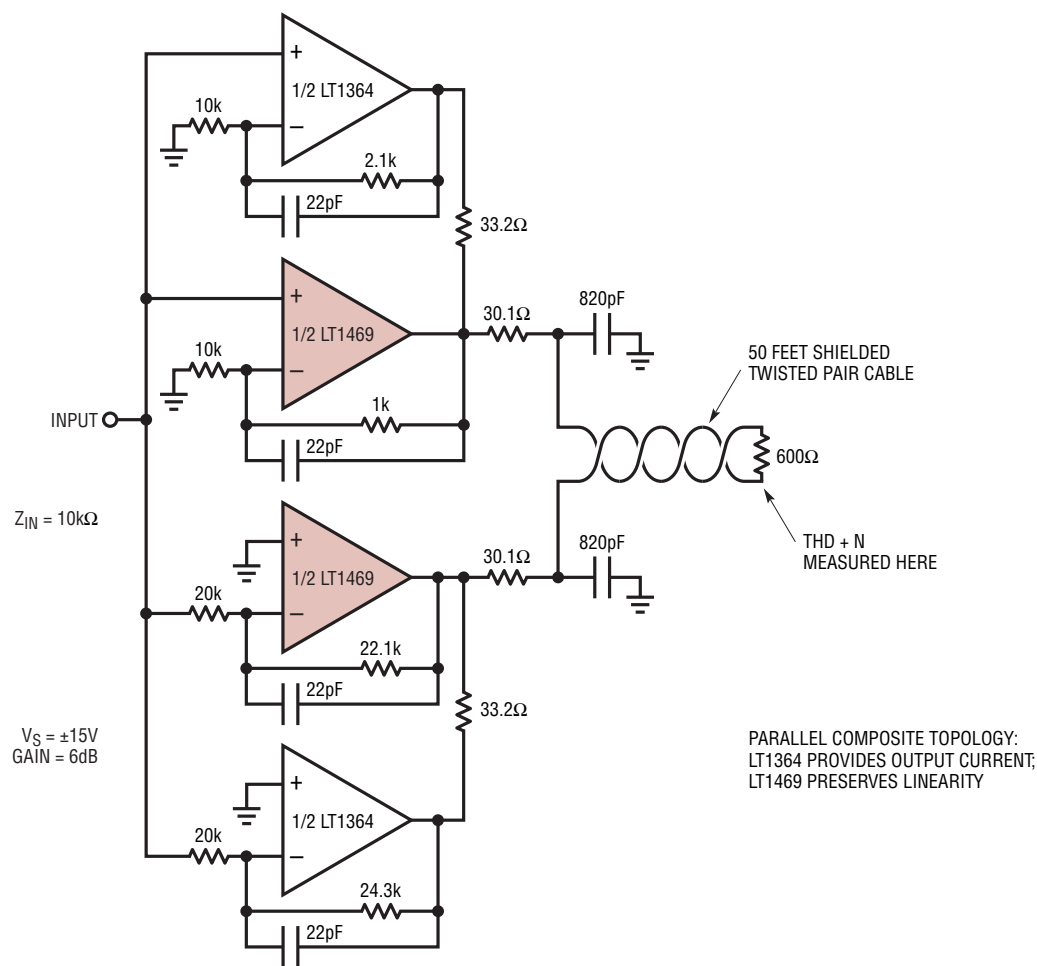


Figure 3. Driving Capacitive Loads

TYPICAL APPLICATIONS

Ultralow Distortion Balanced Audio Line Driver



TOTAL HARMONIC DISTORTION + NOISE	V _{OUT}	FREQUENCY	MEASUREMENT BANDWIDTH
0.00025%	10V _{RMS}	1kHz	22kHz
0.0008%	10V _{RMS}	20Hz TO 20kHz	80kHz
0.0006%	26dBu	1kHz	22kHz

*1dBu = 1 milliwatt into 600Ω

1469 TA02

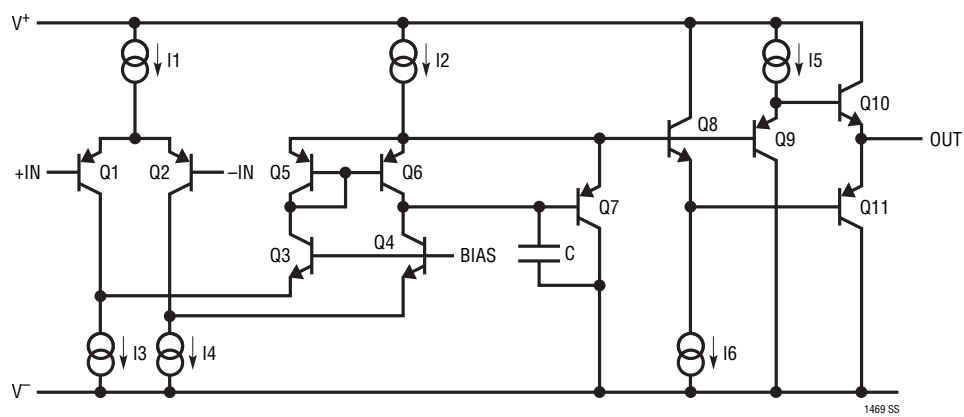
Extending 16-Bit DAC Performance to 200V Output Swing



*HEAT SINK
**VISHAY S102 RESISTOR 0.01%
***1% METAL FILM RESISTOR

NOTE: FOR FURTHER EXPLANATION,
REFER TO APPLICATION NOTE 74, APPENDIX H

SIMPLIFIED SCHEMATIC

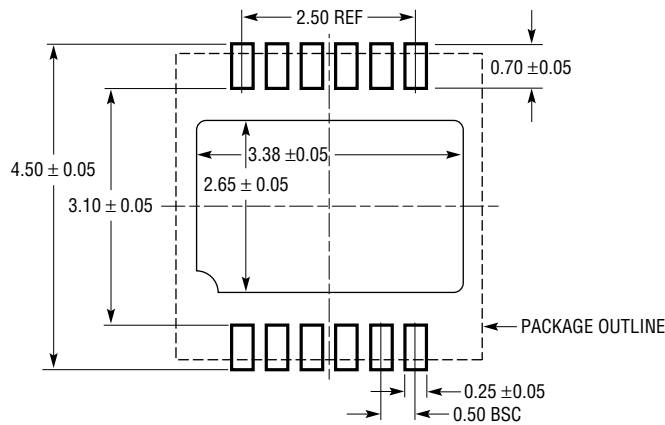


PACKAGE DESCRIPTION

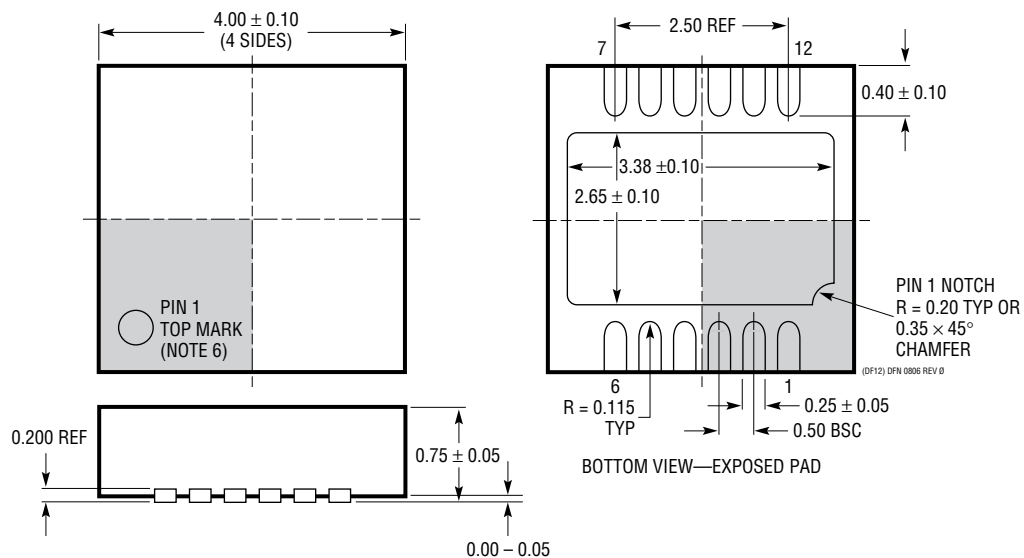
DF Package

12-Lead Plastic DFN (4mm × 4mm)

(Reference LTC DWG # 05-08-1733 Rev 0)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

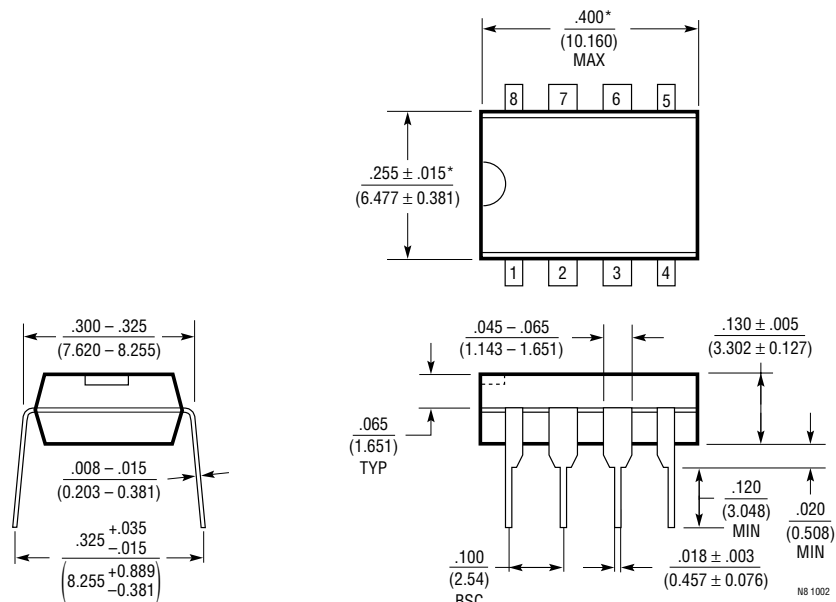


NOTE:

1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

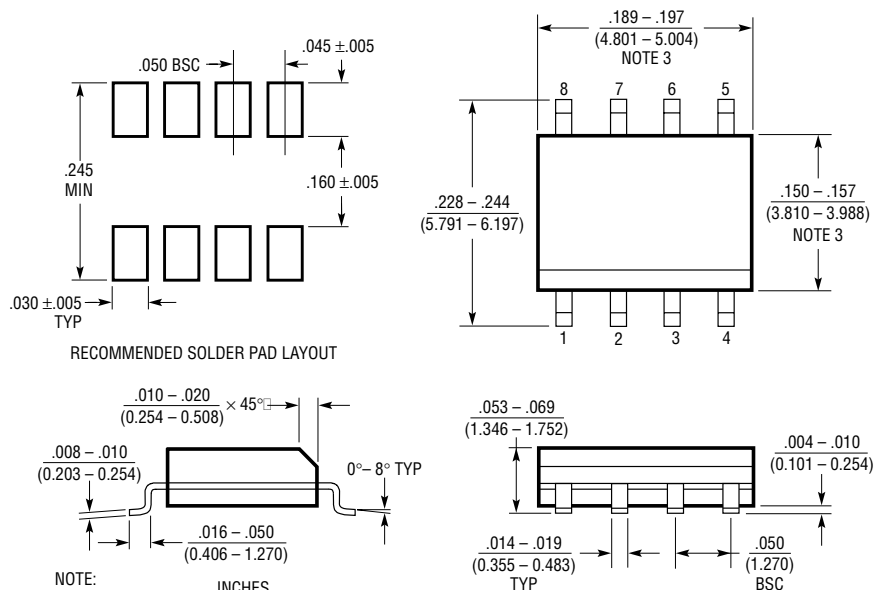
PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow 0.300)
 (Reference LTC DWG # 05-08-1510)



NOTE:
 1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 *THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
 (Reference LTC DWG # 05-08-1610)



NOTE:
 1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

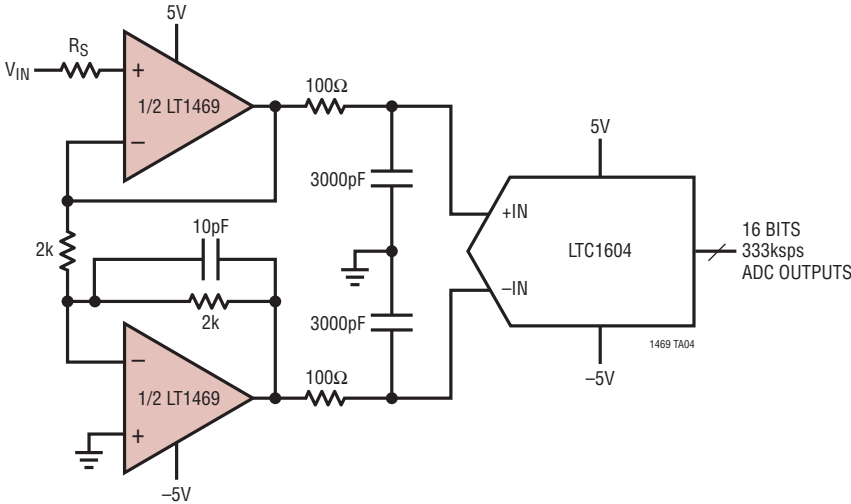
S08 0303

REVISION HISTORY (Revision history begins at Rev B)

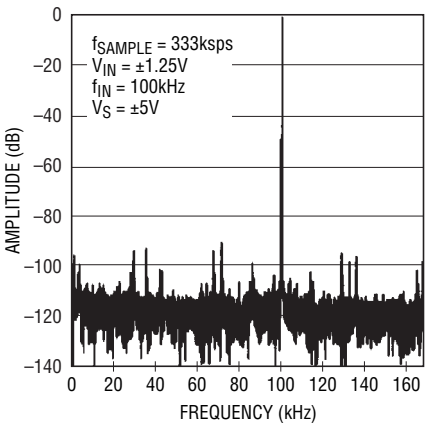
REV	DATE	DESCRIPTION	PAGE NUMBER
B	1/11	Change to Electrical Characteristics	3, 5, 6

TYPICAL APPLICATION

16-Bit Accurate Single Ended to Differential ADC Buffer



4096 Point FFT of ADC Output



1469 TA04a

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1167	Precision Instrumentation Amplifier	Single Resistor Gain Set, 0.04% Max Gain Error, 10ppm Max Gain Nonlinearity
LT1468	Single 90MHz, 22V/μs, 16-Bit Accurate Op Amp	75μV VOS(MAX), Single Version of LT1469
LT1468-2	Single 200MHz, 30V/μs, 16-Bit Accurate AV ≥ 2 Op Amp	75μV VOS(MAX)
LT1469-2	Dual 200MHz, 30V/μs, 16-Bit Accurate AV ≥ 2 Op Amp	75μV VOS(MAX)
LTC1595/LTC1596	16-Bit Serial Multiplying IOU DAC	±1LSB Max INL/DNL, Low Glitch, DAC8043 16-Bit Upgrade
LTC1597	16-Bit Parallel Multiplying IOU DAC	±1LSB Max INL/DNL, Low Glitch, On-Chip Bipolar Resistors
LTC1604	16-Bit, 333ksps Sampling ADC	±2.5V Input, SINAD = 90dB, THD = -100dB
LTC1605	Single 5V, 16-Bit, 100ksps Sampling ADC	Low Power, ±10V Inputs, Parallel/Byte Interface
LT1723	Dual 200MHz, 70V/μs Low Noise Precision Op Amp	VS ≤ ±5V, en = 3.8nV/√Hz, -85dBc at 1MHz
LT1801	Dual 80MHz, 25V/μs Low Power Rail-to-Rail Precision Op Amp	VS ≤ ±5V, ICC = 1.6mA, VOS ≤ 350μV
LT6221	Dual 60MHz, 20V/μs Low Power Rail-to-Rail Precision Op Amp	VS ≤ ±5V, ICC = 0.9mA, VOS ≤ 350μV
LTC6244HV	Dual 50MHz, Low Noise, Precision CMOS Op Amp	VS ≤ ±5V, VOS ≤ 100μV, IB ≤ 75pA