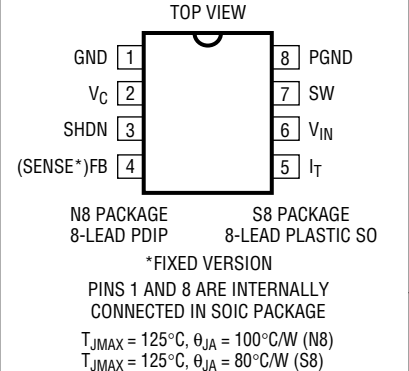


ABSOLUTE MAXIMUM RATINGS

V_{IN} Voltage	10V
SW Voltage	25V
FB Voltage	10V
SHDN Voltage	10V
V_C Voltage	4V
I_T Voltage	4V
Maximum Power Dissipation	700mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER	
	LT1302CN8 LT1302CS8 LT1302CN8-5 LT1302CS8-5	
	S8 PART MARKING	
	1302 13025	

Consult factory for Industrial and Military grade parts.

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{IN} = 2.5\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I _Q	Quiescent Current	V _{SHDN} = 0.5V, V _{FB} = 1.3V V _{SHDN} = 1.8V	● ●		200 15	300 25	μA μA
V _{IN}	Input Voltage Range		●	2.0 2.2		8	V V
V _{FB}	Feedback Voltage (LT1302)	V _C = 0.4V	●	1.22	1.24	1.26	V
	Feedback Pin Bias Current (LT1302)	V _{FB} = 1V			100		nA
	Output Sense Voltage (LT1302-5)	V _C = 0.4V	●	4.85	5.05	5.25	V
	Output Ripple Voltage (LT1302-5)	V _C = 0.4V			50		mV
	Sense Pin Resistance to Ground (LT1302-5)				420		kΩ
V _{OS}	Offset Voltage	See Block Diagram			15		mV
	Comparator Hysteresis	(Note 1)			5		mV
	Oscillator Frequency	Current Limit Not Asserted (Note 2)	●	175 160	220 310	265 310	kHz kHz
DC	Maximum Duty Cycle			75	86	95	%
t _{ON}	Switch On Time	Current Limit Not Asserted			3.9		μs
t _{OFF}	Switch Off Time				0.7		μs
	Output Line Regulation	2 < V _{IN} < 8V	●		0.06	0.15	%/V
V _{CESAT}	Switch Saturation Voltage	I _{SW} = 2A	● ●		310	400 475	mV mV
	Switch Leakage Current	V _{SW} = 5V, Switch Off	●		0.1	10	μA
	Switch Current Limit	V _C = 0.4V (Burst Mode Operation) V _C = 1.25V (Full Power) (Note 3)	● ●	2.0	1 2.8	3.9	A A
	Error Amplifier Voltage Gain	0.9V ≤ V _C ≤ 1.2V, ΔV _C /ΔV _{FB}		50	75		V/V
V _{SHDNH}	Shutdown Pin High		●	1.8			V
V _{SHDNL}	Shutdown Pin Low		●			0.5	V
I _{SHDN}	Shutdown Pin Bias Current	V _{SHDN} = 5V V _{SHDN} = 2V V _{SHDN} = 0V	● ● ●		8 3 0.1	20 1	μA μA μA
	I _T Pin Resistance to Ground				3.9		kΩ

The ● denotes specifications which apply over the 0°C to 70°C temperature range.

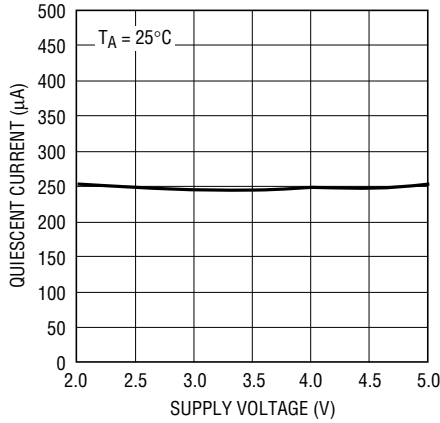
Note 1: Hysteresis is specified at DC. Output ripple depends on capacitor size and ESR.

Note 2: The LT1302 operates in a variable frequency mode. Switching frequency depends on load inductance and operating conditions and may be above specified limits.

Note 3: Minimum switch current 100% tested. Maximum switch current guaranteed by design.

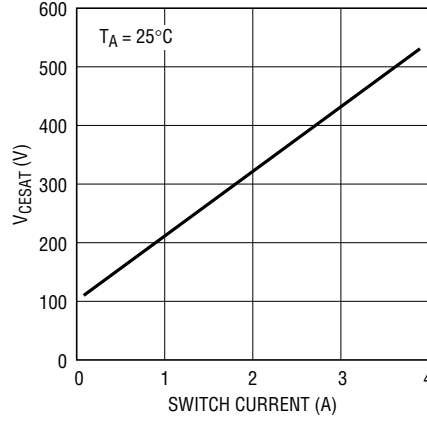
TYPICAL PERFORMANCE CHARACTERISTICS

**No-Load Quiescent Current
Circuit of Figure 1**



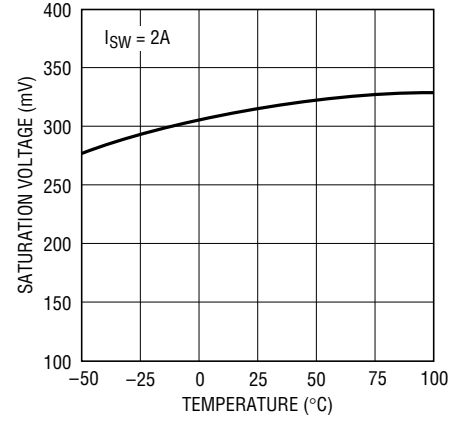
1302 G01

Switch Saturation Voltage



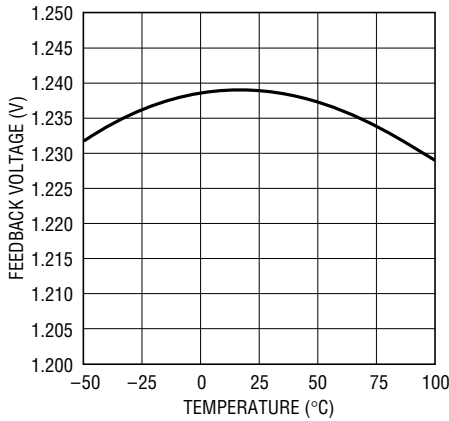
1302 G02

Switch Saturation Voltage



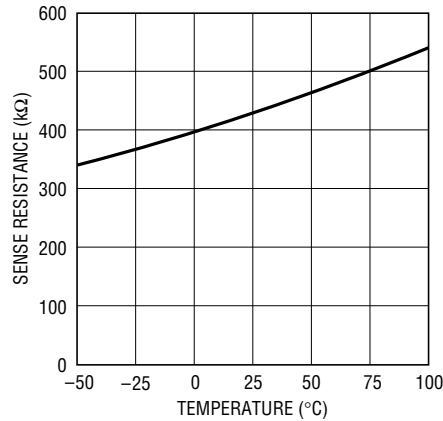
1302 G03

LT1302 Feedback Voltage



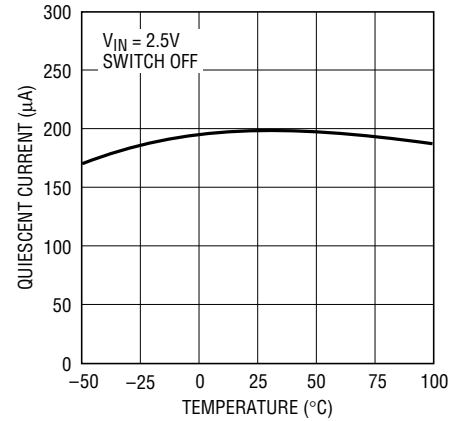
1302 G04

LT1302-5 Sense Pin Resistance



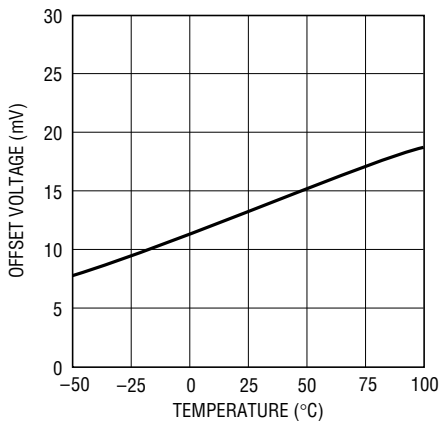
1302 G05

Quiescent Current



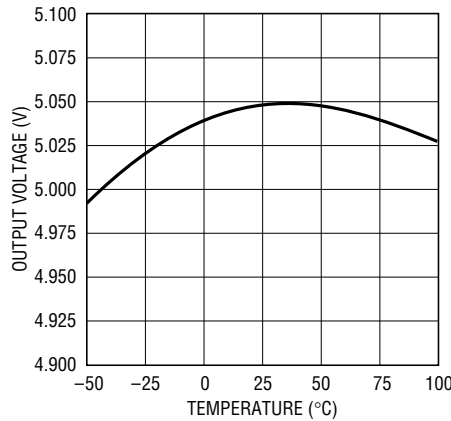
1302 G06

Error Amplifier Offset Voltage



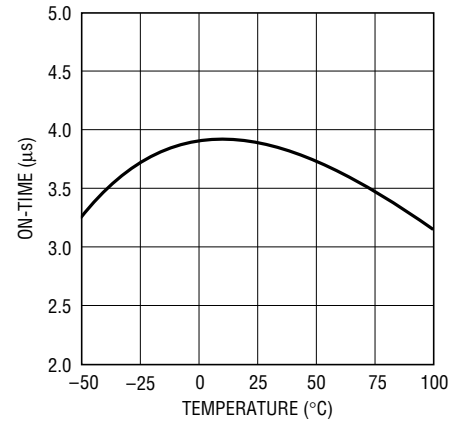
1302 G07

LT1302-5 Output Voltage



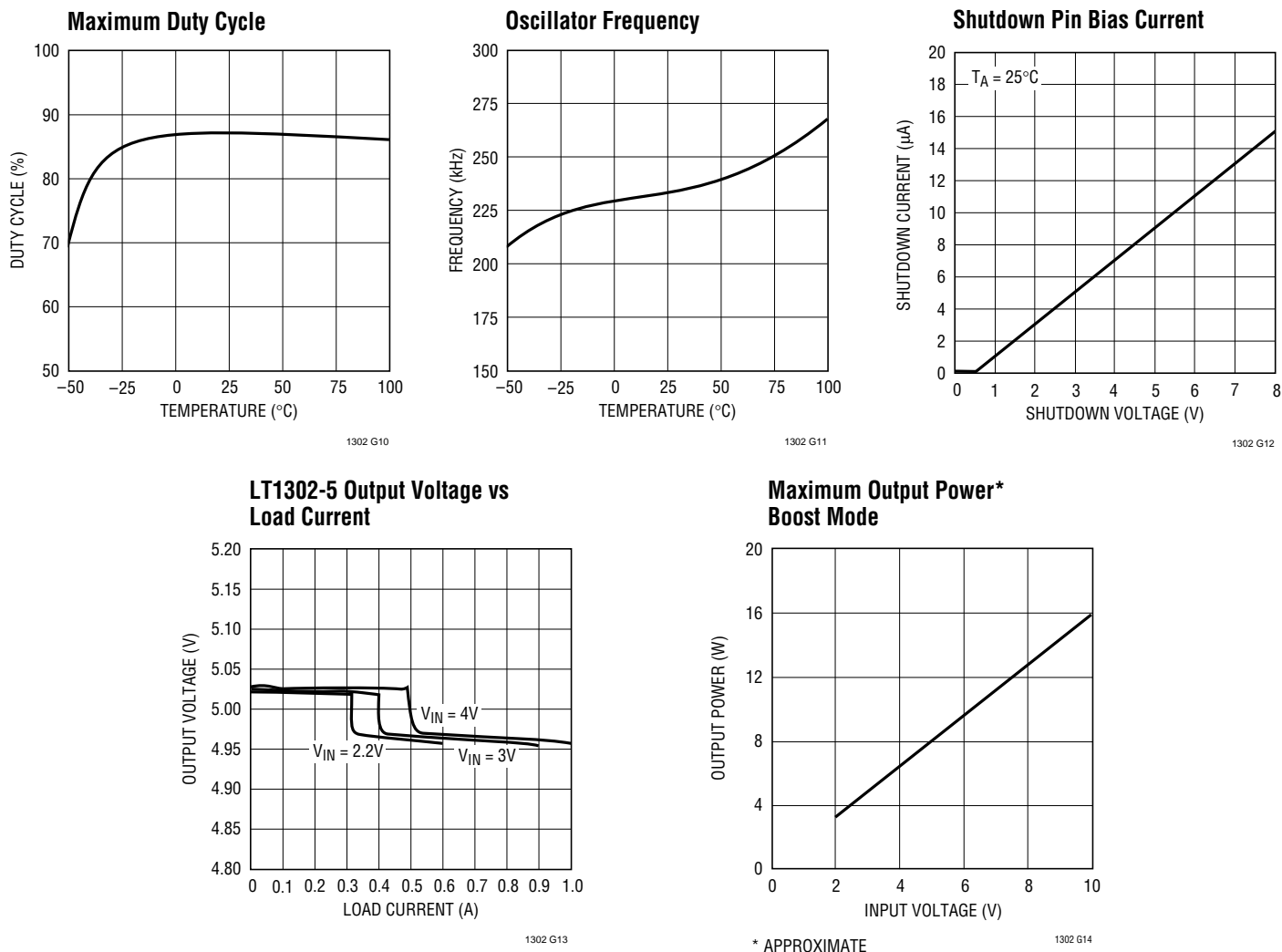
1302 G08

Maximum On-Time



1302 G09

TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

GND (Pin 1): Signal Ground. Feedback resistor and 0.1μF ceramic bypass capacitor from V_{IN} should be connected directly to this pin.

V_C (Pin 2): Frequency Compensation Pin. Connect series RC to GND. Keep trace short.

SHDN (Pin 3): Shutdown. Pull high to effect shutdown; tie to ground for normal operation.

FB/Sense (Pin 4): Feedback/Sense. On the LT1302 this pin connects to CMP1 input. On the LT1302-5 this pin connects to the output resistor string.

I_T (Pin 5): Normally left floating. Addition of a 3.3k resistor to GND forces the LT1302 into current mode at light loads. Efficiency drops at light load but increases at medium loads. See Applications Information section.

V_{IN} (Pin 6): Supply Pin. Must be bypassed with: (1) a 0.1μF ceramic to GND, and (2) a large value electrolytic to PGND. When V_{IN} is greater than 5V, a low value resistor (2Ω to 10Ω) is recommended to isolate the V_{IN} pin from input supply noise.

PIN FUNCTIONS

SW (Pin 7): Switch Pin. Connect inductor and diode here. Keep layout short and direct.

PGND (Pin 8): Power Ground. Pins 8 and 1 should be connected under the package. In the SO package, pins 1

and 8 are thermally connected to the die. One square inch of PCB copper provides an adequate heat sink for the device.

BLOCK DIAGRAMS

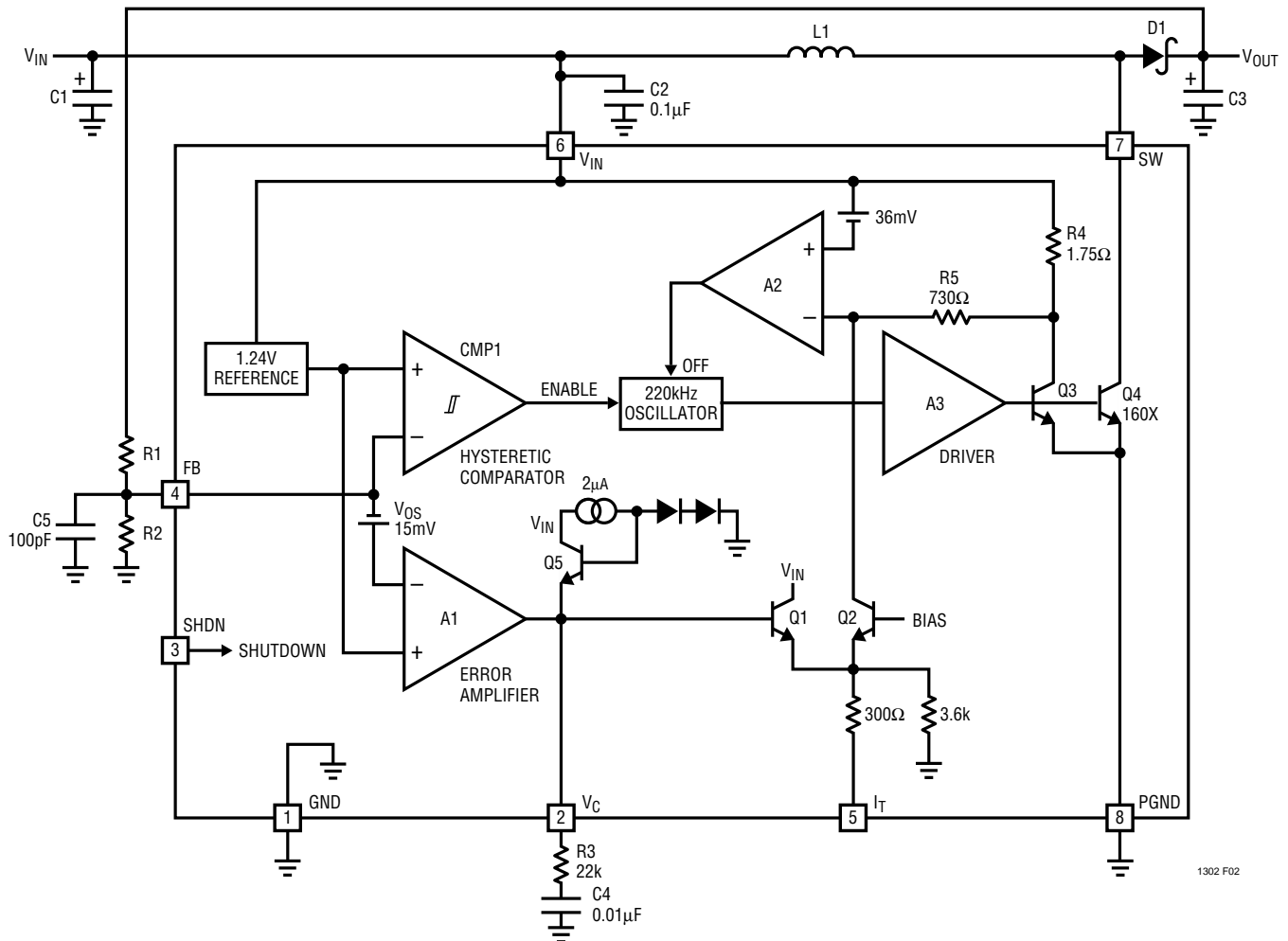


Figure 2. LT1302 Block Diagram

BLOCK DIAGRAMS

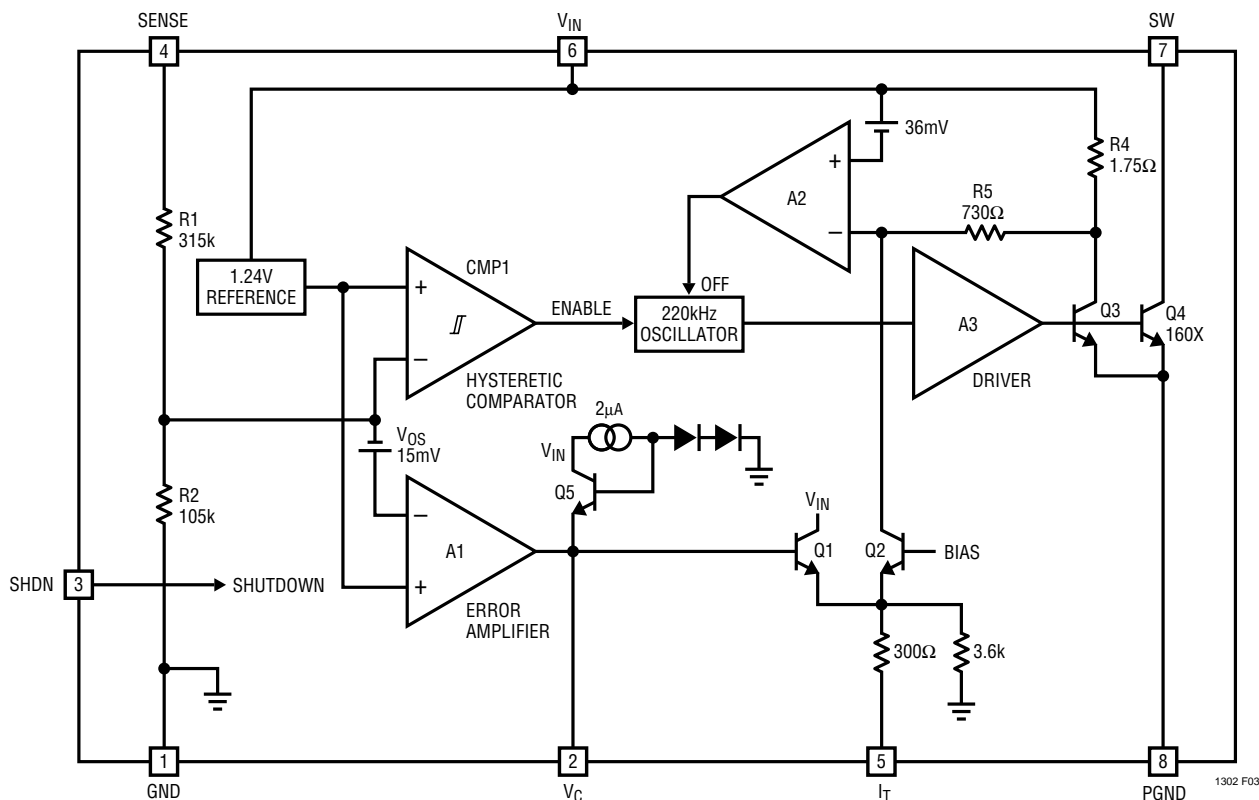


Figure 3. LT1302-5 Block Diagram

OPERATION

The LT1302's operation can best be understood by examining the block diagram in Figure 2. The LT1302 operates in one of two modes, depending on load. With light loads, comparator CMP1 controls the output; with heavy loads, control is passed to error amplifier A1. Burst Mode operation consists of monitoring the FB pin voltage with hysteretic comparator CMP1. When the FB voltage, related to the output voltage by external attenuator R1 and R2, falls below the 1.24V reference voltage, the oscillator is enabled. Switch Q4 alternately turns on, causing current buildup in inductor L1, then turns off, allowing the built-up current to flow into output capacitor C3 via D1. As the output voltage increases, so does the FB voltage; when it exceeds the reference plus

CMP1's hysteresis (about 5mV) CMP1 turns the oscillator off. In this mode, peak switch current is limited to approximately 1A by A2, Q2, and Q3. Q2's current, set at 34μA, flows through R5, causing A2's negative input to be 25mV lower than V_{IN} . This node must fall more than 36mV below V_{IN} for A2 to trip and turn off the oscillator. The remaining 11mV is generated by Q3's current flowing through R4. Emitter-area scaling sets Q3's collector current to 0.625% of switch Q4's current. When Q4's current is 1A, Q3's current is 6.25mA, creating an 11mV drop across R4 which, added to R5's 25mV drop, is enough to trip A2.

When the output load is increased to the point where the 1A peak current cannot support the output voltage,

OPERATION

CMP1 stays on and the peak switch current is regulated by the voltage on the V_C pin (A1's output). V_C drives the base of Q1. As the V_C voltage rises, Q2 conducts less current, resulting in less drop across R5. Q4's peak current must then increase in order for A2 to trip. This current mode control results in good stability and immunity to input voltage variations. Because this is a linear,

closed-loop system, frequency compensation is required. A series RC from V_C to ground provides the necessary pole-zero combination.

The LT1302-5 incorporates feedback resistors R1 and R2 into the device. Output voltage is set at 5.05V in Burst Mode, dropping to 4.97V in current mode.

APPLICATIONS INFORMATION

Inductor Selection

Inductors used with the LT1302 must fulfill two requirements. First, the inductor must be able to handle current of 2.5A to 3A without runaway saturation. Rod or drum core units usually saturate gradually and it is acceptable to exceed manufacturers' published saturation currents by 20% or so. Second, it should have low DCR, under 0.05Ω so that copper loss is kept low. Inductance value is not critical. Generally, for low voltage inputs down to 2V, a $10\mu\text{H}$ inductor is recommended (such as Coilcraft DO3316-103). For inputs above 4V to 5V use a $22\mu\text{H}$ unit (such as Coilcraft DO3316-223). Switching frequency can reach up to 400kHz so the core material should be able to handle high frequency without loss. Ferrite or molypermalloy cores are a better choice than powdered iron. If EMI is a concern a toroidal inductor is suggested, such as Coiltronics CTX20-4.

For a boost converter, duty cycle can be calculated by the following formula:

$$DC = 1 - \left(\frac{V_{IN}}{V_{OUT}} \right)$$

A special situation exists where the V_{OUT}/V_{IN} differential is high, such as a 2V-to-12V converter. The required duty cycle is higher than the LT1302 can provide, so the converter must be designed for *discontinuous* operation. This means that inductor current goes to zero during the switch off-time. In the 2V-to-12V case, inductance must be low enough so that current in the inductor can reach 2A in a single cycle. Inductor value can be defined by:

$$L \leq \frac{(V_{IN} - V_{SW}) \times t_{ON}}{2A}$$

With the 2V input a value of $3.3\mu\text{H}$ is acceptable. Since the inductance is so low, usually a smaller core size can be used. Efficiency will not be as high as for the continuous case since peak currents will necessarily be higher.

Table 1 lists inductor suppliers along with appropriate part numbers.

Table 1. Recommended Inductors

VENDOR	PART NO.	VALUE(μH)	PHONE NO.
Coilcraft	DO3316-103	10	(708) 639-6400
	DO3316-153	15	
	DO3316-223	22	
Coiltronics	CTX10-2	10	(407) 241-7876
	CTX20-4	20	
Dale	LPT4545-100LA	10	(605) 665-9301
	LPT4545-200LA	20	
Sumida	CD105-100	10	(708) 956-0666
	CD105-150	15	
	CDR125-220	22	

Capacitor Selection

The output capacitor should have low ESR for proper performance. A high ESR capacitor can result in "mode-hopping" between current mode and Burst Mode at high load currents because the output voltage will increase by $I_{SW} \times \text{ESR}$ when the inductor current is flowing into the diode. Figure 4 shows output voltage of an LT1302-5 boost converter with two $220\mu\text{F}$ AVX TPS capacitors at the output. Ripple voltage at a 510mA load is about 30mV_{P-P} .

APPLICATIONS INFORMATION

and there is no low frequency component. The total ESR is under 0.03Ω . If a single $100\mu\text{F}$ aluminum electrolytic capacitor is used instead, the converter mode-hops between current mode and Burst Mode due to high ESR, causing the voltage comparator to trip as shown in Figure 5. The ripple voltage is now over $500\text{mV}_{\text{P-P}}$ and contains a low frequency component. Maximum allowable output capacitor ESR can be calculated by the following formula:

$$\text{ESR}_{\text{MAX}} = \frac{V_{\text{OS}} \times V_{\text{OUT}}}{V_{\text{REF}} \times 1\text{A}}$$

where,

$$V_{\text{OS}} = 15\text{mV}$$

$$V_{\text{REF}} = 1.24\text{V}$$

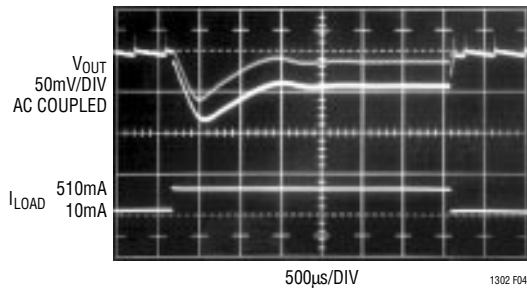


Figure 4. Low ESR Output Capacitor Results in Stable Operation. Ripple Voltage is Under $30\text{mV}_{\text{P-P}}$

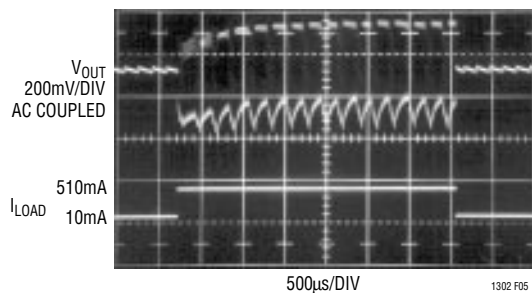


Figure 5. Inexpensive Electrolytic Capacitor Has High ESR, Resulting in Mode-Hop, Ripple Voltage Amplitude Is Over $500\text{mV}_{\text{P-P}}$ and Includes Low Frequency Component

Input Capacitor

The input supply should be decoupled with a good quality electrolytic capacitor close to the LT1302 to provide a stable input supply. Long leads or traces from power source to the switcher can have considerable impedance at the LT1302's switching frequency. The input capacitor provides a low impedance at high frequency. A $0.1\mu\text{F}$ ceramic capacitor is required right at the V_{IN} pin. When the input voltage can be above 5V , a $10\Omega/1\mu\text{F}$ decoupling network for V_{IN} is recommended as detailed in Figure 6. This network is also recommended when driving a transformer.

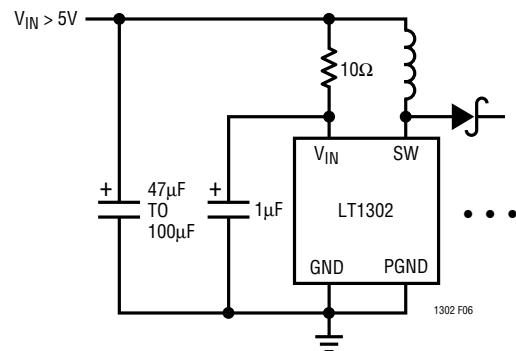


Figure 6. A $10\Omega/1\mu\text{F}$ Decoupling Network at V_{IN} Is Recommended When Input Voltage Is Above 5V

Table 2 lists capacitor vendors along with device types.

Table 2. Recommended Capacitors

VENDOR	SERIES	TYPE	PHONE NO.
AVX	TPS	Surface Mount	(803) 448-9411
Sanyo	OS-CON	Through Hole	(619) 661-6835
Sprague	595D	Surface Mount	(603) 224-1961

Diode Selection

A 2A Schottky diode such as Motorola MBRS130LT3 has been found to be the best available. Other choices include 1N5821 or MBRS130T3. Do not use "general purpose" diodes such as 1N4001. They are much too slow for use in switching regulator applications.

The V_C pin is sensitive to high frequency noise. Some layouts may inject enough noise to modulate peak switch current at 1/2 the switching frequency. A small capacitor connected from V_C to ground will eliminate this. Do not exceed 1/10 of the compensation capacitor value.

APPLICATIONS INFORMATION

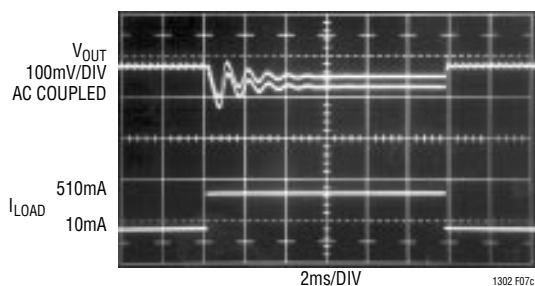


Figure 7c. 0.01µF from V_C to Ground. Underdamped Response Requires Series R

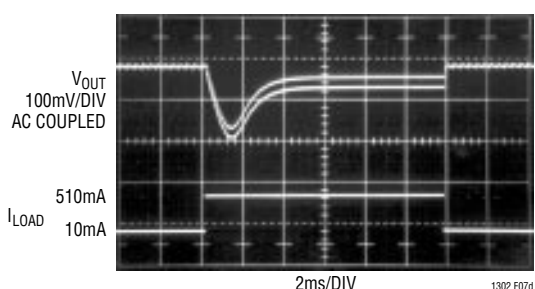


Figure 7d. 0.1µF with 10k Series RC. Classic Overdamped Response

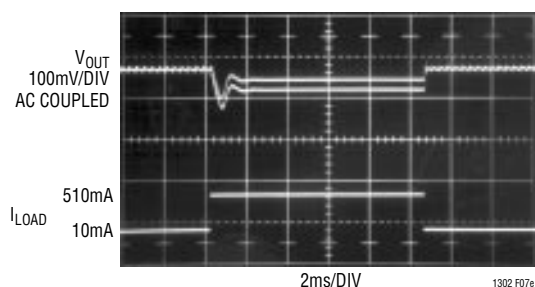


Figure 7e. 0.01µF, 10k Series RC Shows Good Transient Response. Slight Underdamping Still Noticeable

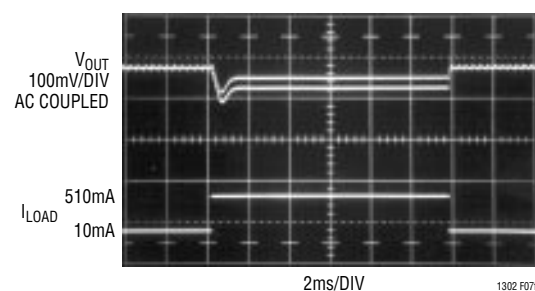


Figure 7f. 0.01µF, 24k Series RC Results in Optimum Response

I_T Pin

The I_T pin is used to disable Burst Mode, forcing the LT1302 to operate in current mode even at light load. To disable Burst Mode, 3.3k resistor R1 is connected from I_T to ground. More conservative frequency compensation must be used when in this mode. A 0.1µF capacitor and 4.7k resistor from V_C to ground has been found to be adequate. Low frequency Burst Mode ripple can be reduced or eliminated using this technique in many applications.

To illustrate, the transient load response of Figure 8's circuit is pictured without and with R1. Figure 8a shows output voltage and inductor current without the resistor. Note the 6kHz burst rate when the converter is delivering 25mA. By adding the 3.3k resistor, the low frequency bursting is eliminated, as shown in Figure 8b. This feature is useful in systems that contain audio circuitry. At very light or zero load, switching frequency drops and eventu-

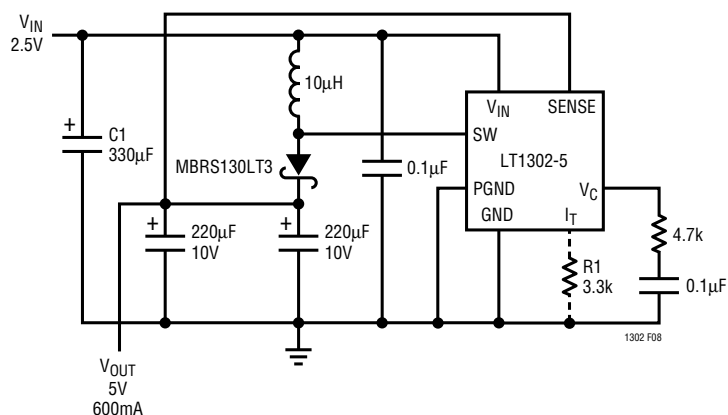


Figure 8. Addition of R1 Eliminates Low Frequency Output Ripple in This 2.5V to 5V Boost Converter

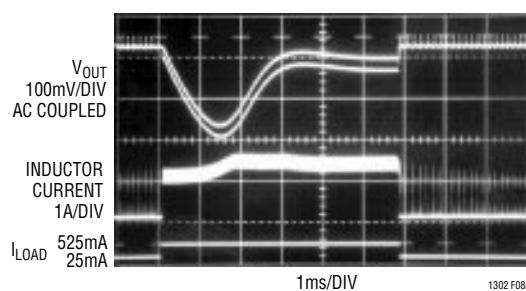


Figure 8a. I_T Pin Floating. Note 6kHz Burst Rate at $I_{LOAD} = 25mA$. 0.1µF/4.7k Compensation Network Causes 220mV Undershoot

APPLICATIONS INFORMATION

ally reaches audio frequencies, but at a much lighter load than without the I_T feature. At some input voltage/load current combinations, some residual bursting may occur at frequencies out of the audio band.

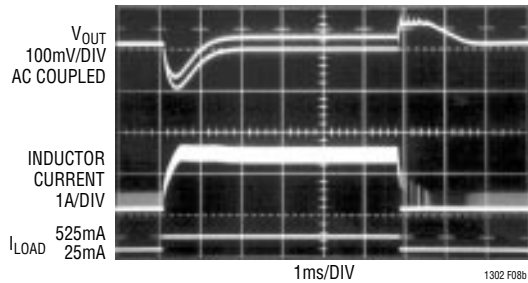


Figure 8b. 3.3k Resistor from I_T Pin to Ground Forces LT1302 into Current Mode Regardless of Load. Audio Frequency Component Eliminated

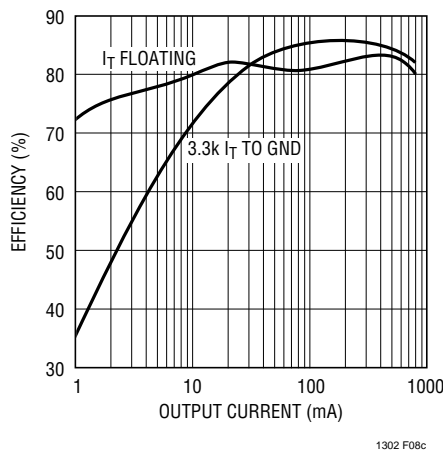


Figure 8c. 3.3k Resistor for I_T to Ground Increases Efficiency at Moderate Load, Decreases at Light Load

The I_T pin cannot be used as a soft-start. Large capacitors connected to the pin will cause erratic operation. If operating the device in Burst Mode, let the pin float. Keep high dV/dt signals away from the pin.

Figure 8c details efficiency with and without the addition of R1. Burst Mode operation keeps efficiency high at light load with I_T floating. Efficiency falls off at light load with R1 added because the LT1302 cannot transition into Burst Mode.

Layout

The high speed, high current switching associated with the LT1302 mandates careful attention to layout. Follow the suggested component placement in Figure 9 for proper operation. High current functions are separated by the package from sensitive control functions. Feedback resistors R1 and R2 should be close to the feedback pin (pin4). Noise can easily be coupled into this pin if care is not taken. A small capacitor (100pF to 200pF) from FB to ground provides a high frequency bypass. If the LT1302 is operated off a three-cell or higher input, R3 (2Ω to 10Ω) in series with V_{IN} is recommended. This isolates the device from noise spikes on the input supply. Do not put in R3 if the device must operate from a 2V input, as input current will cause the voltage at the LT1302's V_{IN} pin to go below 2V. The 0.1 μ F ceramic bypass capacitor C3 (use X7R, not Z5U) should be mounted as close as possible to the package. When R3 is used, C3 should be a 1 μ F tantalum unit. Grounding should be segregated as illustrated. C3's ground trace should not carry switch current. Run a

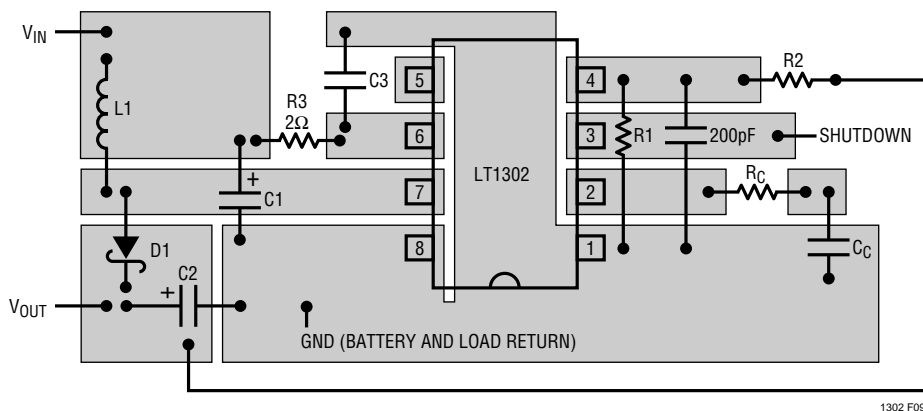


Figure 9. Suggested Component Placement for LT1302

APPLICATIONS INFORMATION

separate ground trace up under the package as shown. The battery and load return should go to the power side of the ground copper.

Thermal Considerations

The LT1302 contains a thermal shutdown feature which protects against excessive internal (junction) temperature. If the junction temperature of the device exceeds the protection threshold, the device will begin cycling between normal operation and an off state. The cycling is not harmful to the part. The thermal cycling occurs at a slow rate, typically 10ms to several seconds, which depends on the power dissipation and the thermal time constants of the package and heat sinking. Raising the ambient temperature until the device begins thermal shutdown gives a good indication of how much margin there is in the thermal design.

For surface mount devices heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Experiments have shown that the heat spreading copper layer does not need to be electrically connected to the tab of the device. The PCB material can be very effective at transmitting heat between the pad area attached to pins 1 and 8 of the device, and a ground or power plane layer either inside or on the opposite side of the board. Although the actual thermal resistance of the PCB material is high, the length/area ratio of the thermal resistance between the layer is small. Copper board stiffeners and plated through holes can also be used to spread the heat generated by the device.

Table 3 lists thermal resistance for the SO package. Measured values of thermal resistance for several different board sizes and copper areas are listed for each surface mount package. All measurements were taken in still air on 3/32" FR-4 board with 1 oz copper. This data can be used as a rough guideline in estimating thermal resistance. The thermal resistance for each application will be affected by thermal interactions with other components as well as board size and shape.

Table 3. S8 Package, 8-Lead Plastic SO

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500 sq. mm	2500 sq. mm	2500 sq. mm	60°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	62°C/W
225 sq. mm	2500 sq. mm	2500 sq. mm	65°C/W
100 sq. mm	2500 sq. mm	2500 sq. mm	69°C/W
100 sq. mm	1000 sq. mm	2500 sq. mm	73°C/W
100 sq. mm	225 sq. mm	2500 sq. mm	80°C/W
100 sq. mm	100 sq. mm	2500 sq. mm	83°C/W

* Pins 1 and 8 attached to topside copper
N8 Package, 8-Lead DIP:
Thermal Resistance (Junction-to-Ambient) = 100°C/W

Calculating Temperature Rise

Power dissipation internal to the LT1302 in a boost regulator configuration is approximately equal to:

$$P_D = I_{OUT}^2 R \left[\left(\frac{V_{OUT} + V_D}{V_{IN} - \frac{I_{OUT} V_{OUT} R}{V_{IN}}} \right)^2 - \left(\frac{V_{OUT} + V_D}{V_{IN} - \frac{I_{OUT} V_{OUT} R}{V_{IN}}} \right) \right] + \frac{I_{OUT} (V_{OUT} + V_D - V_{IN})}{27}$$

The first term in this equation is due to switch "on-resistance." The second term is from the switch driver. R is switch resistance, typically 0.15Ω. V_D is the diode forward drop.

The temperature rise can be calculated from:

$$\Delta T = P_D \times \theta_{JA}$$

where:

ΔT = Temperature Rise

P_D = Device Power Dissipation

θ_{JA} = Thermal Resistance (Junction-to-Ambient)

APPLICATIONS INFORMATION

As an example, consider a boost converter with the following specifications:

$$V_{IN} = 3V$$

$$V_{OUT} = 6V$$

$$I_{OUT} = 700mA$$

Total power loss in the LT1302, assuming $R = 0.15\Omega$ and $V_D = 0.45V$, is:

$$P_D = (700mA)^2 (0.15\Omega) \left[\left(\frac{6 + 0.45}{3 - \frac{0.7 \times 6 \times 0.15}{3}} \right)^2 - \left(\frac{6 + 0.45}{3 - \frac{0.7 \times 6 \times 0.15}{3}} \right) \right] + \frac{(0.7)(6 + 0.45 - 3)}{27}$$

$$= 223mW + 89mW = 312mW$$

Using the CS8 package with 100 sq. mm topside and backside heat sinking:

$$\Delta T = (312mW)(84^\circ C/W) = 25.9^\circ C \text{ rise}$$

With the N8 package:

$$\Delta T = 31.2^\circ C$$

At a $70^\circ C$ ambient, die temperature would be $101.2^\circ C$.

[illegible]

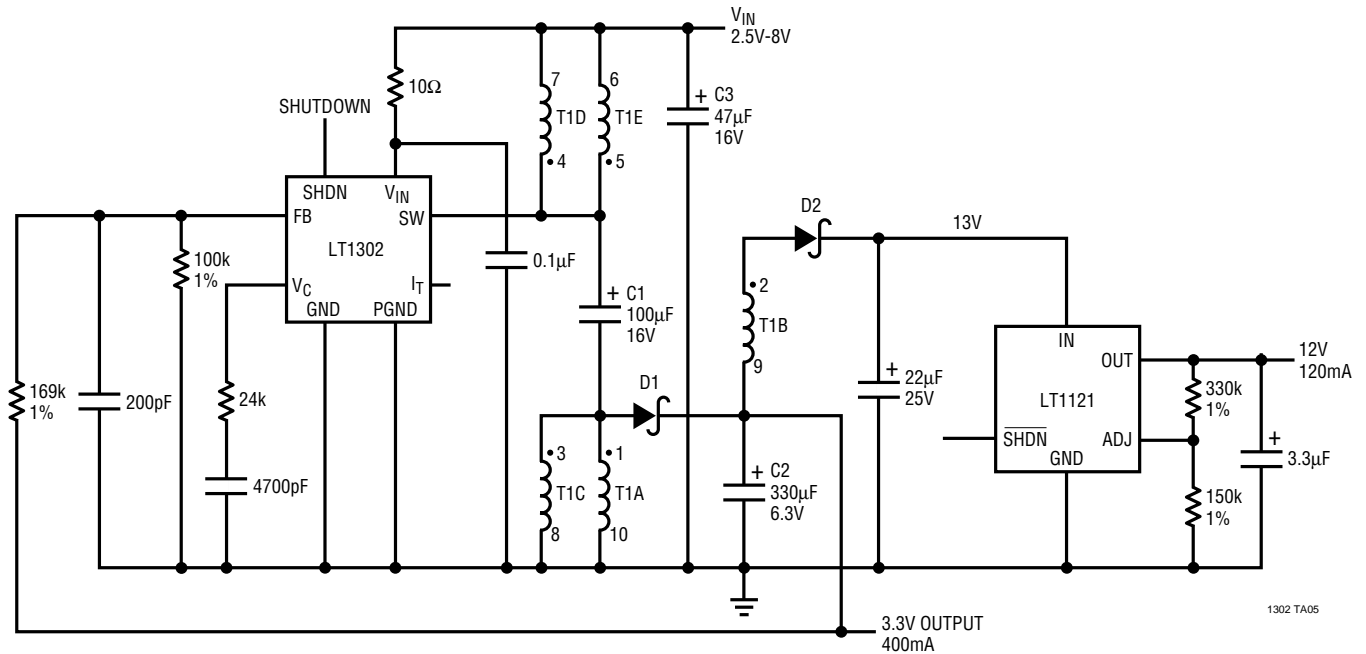
1302 TA03

The schematic diagram illustrates the LT1302 step-down converter circuit. The input is provided by two 1.5V cells (2 CELLS) connected in series. A 100μF capacitor (C1) is connected in parallel with the input. The input voltage (VIN) is connected to pin 7 (SW). A 3.3μH inductor (L1) is connected between pin 7 and the output. A diode (D1) is connected between pin 7 and the output. The output is connected to pin 8 (PGND). The output voltage is 12V at 120mA. The output is connected to a load resistor (R2, 866k, 1%) and a 100pF capacitor. The output is also connected to a feedback network consisting of a 100k resistor (R1, 1%) and a 0.02μF capacitor (CC) connected to pin 4 (FB). The feedback network is also connected to pin 2 (VC). The feedback network is also connected to pin 1 (GND). The feedback network is also connected to pin 3 (SHUTDOWN). The feedback network is also connected to pin 5 (IT). The feedback network is also connected to pin 6 (NC). The feedback network is also connected to pin 7 (VIN). The feedback network is also connected to pin 8 (PGND). The feedback network is also connected to pin 9 (GND). The feedback network is also connected to pin 10 (VOUT).

D1 = MOTOROLA MBRS130LT3
L1 = COILCRAFT DO3316-332

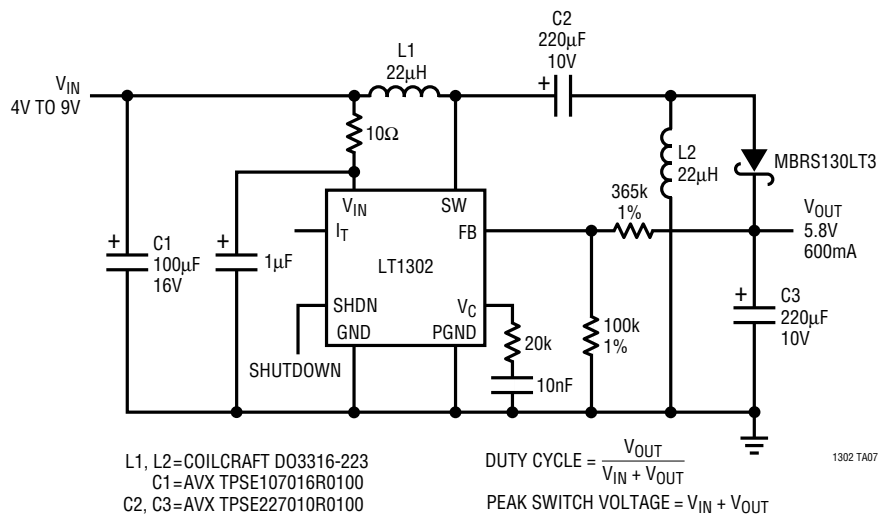
TYPICAL APPLICATIONS

3 Cell to 3.3V Buck-Boost Converter with Auxiliary 12V Regulated Output



T1 = DALE LPE-6562-A069, 1:3:1:1 TURNS RATIO, 10μH PRIMARY. DALE (605) 665-9301
 D1, D2 = MOTOROLA MBRS130LT3
 C1 = AVX TPSE107016R0100
 C2 = AVX TPSE337006R0100
 C3 = AVX TPSD476016R0150

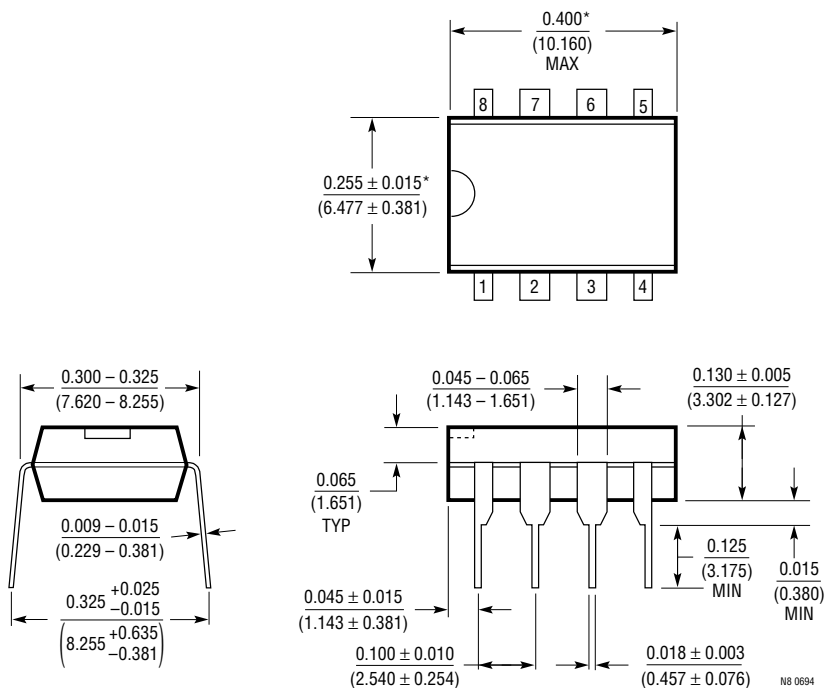
2 Li-Ion Cell to 5.8V/600mA DC/DC Converter



L1, L2=COILCRAFT D03316-223
 C1=AVX TPSE107016R0100
 C2, C3=AVX TPSE227010R0100

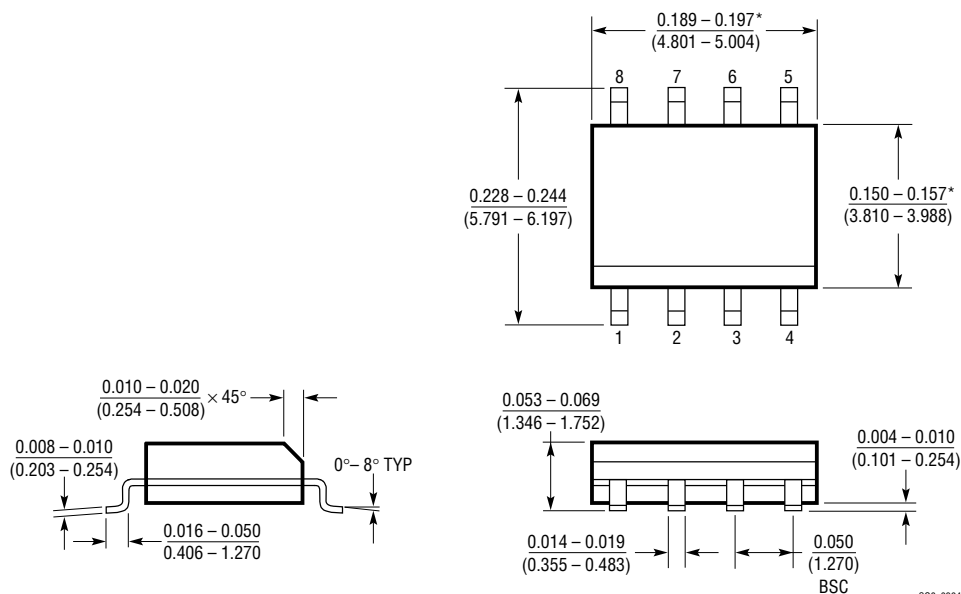
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N8 Package 8-Lead Plastic DIP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

S8 Package 8-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).