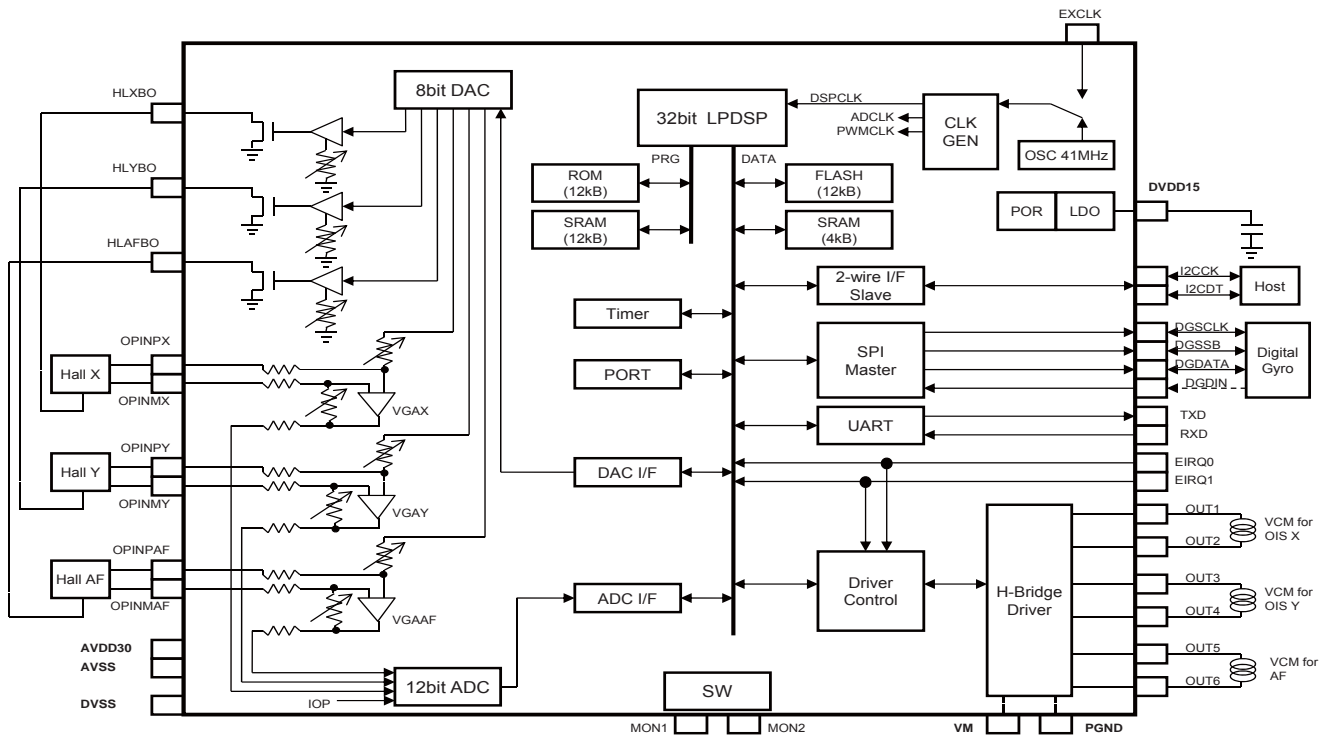
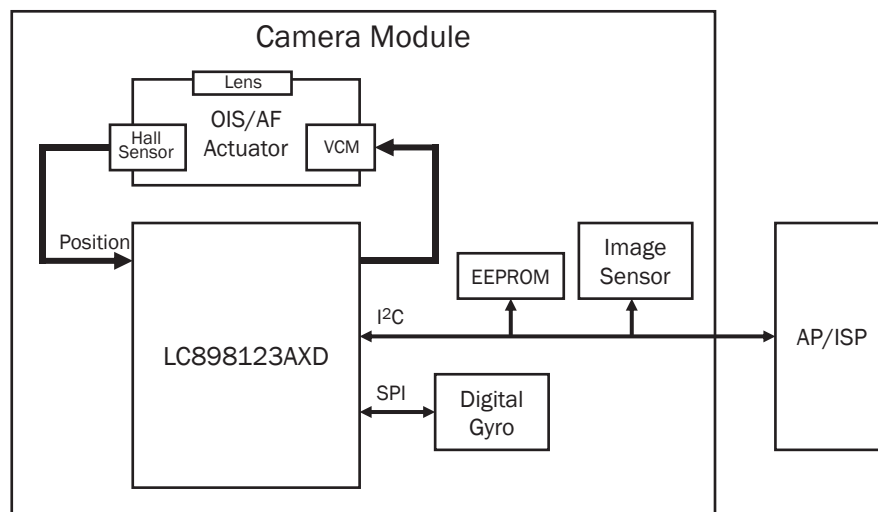


LC898123AXD

Block Diagram



Application Diagram



LC898123AXD

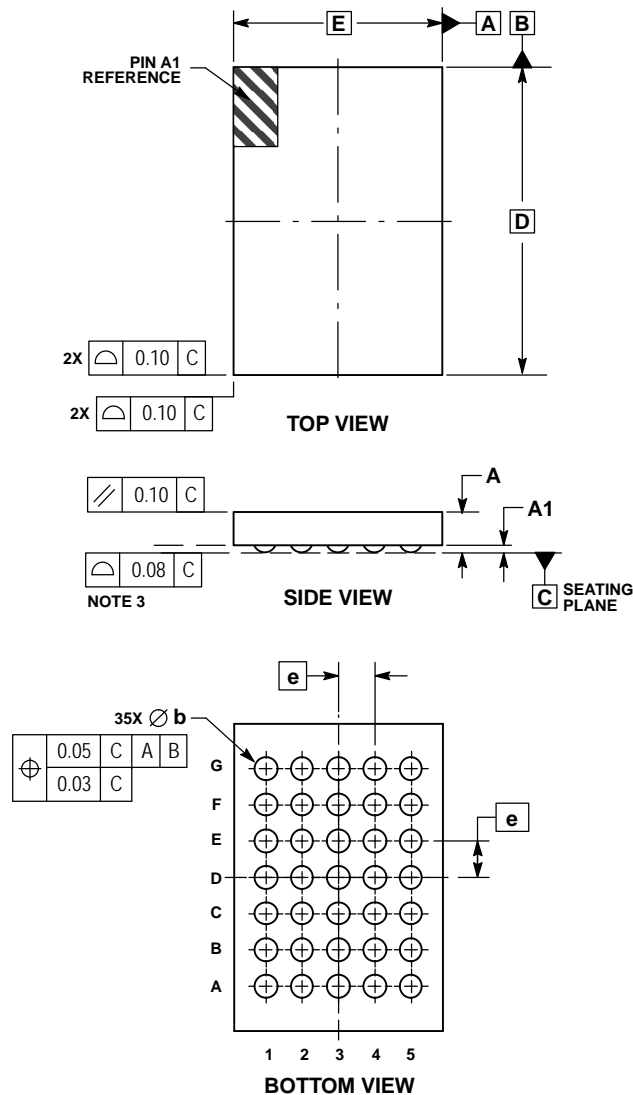
Package Dimensions

unit : mm

WLCSP35, 3.39x2.3

CASE 567JG

ISSUE O

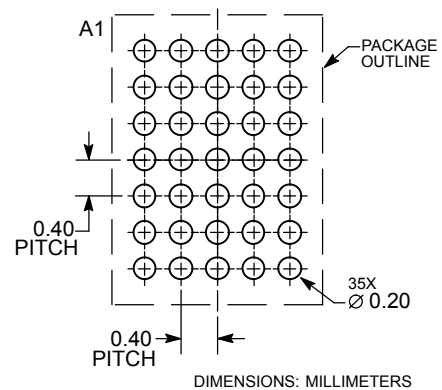


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.45
A1	0.03	0.13
b	0.15	0.25
D	3.39 BSC	
E	2.30 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Pin Assignment

Bottom View

5	OUT5	OUT3	OUT4	PGND	OUT2	OUT1	WPB
4	OUT6	DGDATA	DGSSB	VM	I2CDT	I2CCK	TXD
3	HLAFBO	DGSCLK	DVSS	NC	EXCLK	DGDIN	EIRQ1
2	HLXBO	HLXBO	OPINM AF	OPINMX	OPINMY	EIRQ0	MON2
1	OPINP AF	OPINPX	OPINPY	AVSS	AVDD30	DVDD15	MON1
	G	F	E	D	C	B	A

Driver

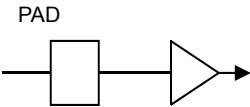
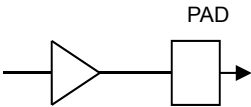
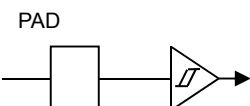
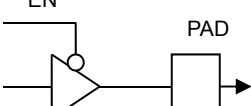
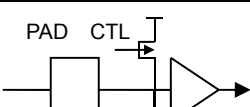
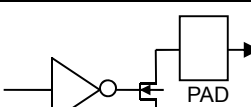
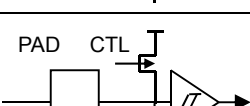
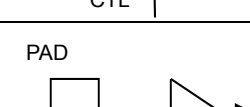
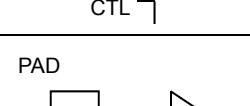
V_{DD} / V_{SS}

Internal Digital V_{DD} Output

LC898123AXD

Pin Description

I/O		Pin Specification			
I	Input	3IC	3V CMOS Input	3IA	3V Analog Input
O	Output	3IS	3V CMOS Schmitt Input	3OA	3V Analog Output
B	Bidirection	3ICUD	3V CMOS Input with PullUp/PullDown		
P	Power	3ISUD	3V CMOS Schmitt Input with PullUp/PullDown		
		3ICD	3V CMOS Input with PullDown		
		3ISD	3V CMOS Schmitt Input with PullDown		
		3O2	3V 2mA Output		
		3T2	3V 2mA TriState Output	Z/U/D	HiZ/PullUp/PullDown
		3OD	3V 2mA Open Drain Output	H/L	HIGH/LOW

3IC	3V CMOS Input		3O2	3V 2mA Output	
3IS	3V Schmitt Input		3T2	3V 2mA TriState Output	
3ICUD	3V CMOS Input with PullUp/ Pulldown		3OD	3V 2mA Open Drain Output	
3ISUD	3V Schmitt Input with PullUp/ Pulldown				
3ICD	3V CMOS Input with Pulldown				
3ISD	3V Schmitt Input with Pulldown				

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	Pin	I/O	I/O Spec		Primary Function	Sub Functions	Init
A1	MON1	B	3ICUD	3T2 30A	(Debugger Data Output)	I2C Data I/O for DAC Monitor Servo Monitor Analog Out Internal Signal Monitor	L
A2	MON2	B	3ICUD	3T2 30A	(Debugger Data Input)	I2C Data I/O for DAC Monitor Servo Monitor Analog Out Internal Signal Monitor	Z
A3	EIRQ1	B	3ISUD	3T2 30A	External IRQ1 External Clock Input	I2C Data I/O for DAC Monitor UART Data Output(TXD) Internal Signal Monitor Servo Monitor Analog Input	Z
A4	TXD	B	3ICUD	3T2	UART Data Output	I2C Data I/O for DAC Monitor I2C Clock for I2C Slave Internal Signal Monitor	Z
A5	WPB	I	3ICD		Write Protect Input		-
B1	DVDD15	P			Internal LDO Power Output		-
B2	EIRQ0	B	3ICD	3OD	External IRQ0	I2C Data I/O for DAC Monitor UART Data Input(RXD) Internal Signal Monitor	Z
B3	DGDIN	B	3ICUD	3T2	Digital Gyro Data Input (4 Wired)	I2C Data I/O for DAC Monitor Internal Signal Monitor	U
B4	I2CCK	B	3IS	3OD	I2C Clock		Z
B5	OUT1	O		30A	OIS Driver Output (H-Bridge or Linear)		-
C1	AVDD30	P			Analog Power (2.6 to 3.6V)		-
C2	OPINMY	I	3IA		OIS Hall Y Op-amp Input Minus		-
C3	EXCLK	B	3ISD	3OD	External Clock Input External IRQ1	I2C Data I/O for DAC Monitor Internal Signal Monitor	Z
C4	I2CDT	B	3IS	3OD	I2C Data		Z
C5	OUT2	O		30A	OIS Driver Output (H-Bridge or Linear)		-
D1	AVSS	P			Analog GND		-
D2	OPINMX	I	3IA		OIS Hall X Op-amp Input Minus		-
D3	NC	-			No Connection		-
D4	VM	P			Driver Power (2.6V to 3.6V)		-
D5	PGND	P			Driver GND		-

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	Pin	I/O	I/O Spec		Primary Function	Sub Functions	Init
E1	OPINPY	I	3IA		OIS Hall Y Op-amp Input Plus		-
E2	OPINMAF	I	3IA		AF Hall Op-amp Input Minus		-
E3	DVSS	P			Logic GND		-
E4	DGSSB	B	3ICUD	3T2	Digital Gyro I/F Chip Select Input	Digital Gyro I/F Chip Select Output	U
					Digital Gyro I/F Chip Select Output	Internal Signal Monitor	
E5	OUT4	O		3OA	OIS Driver Output (H-Bridge or Linear)		-
F1	OPINPX	I	3IA		OIS Hall X Op-amp Input Plus		-
F2	HLXBO	O		3OA	OIS Hall X Bias Output		-
F3	DGCLK	B	3ICUD	3T2	Digital Gyro I/F Clock Input	Digital Gyro Clock Output	U
					Digital Gyro I/F Clock Output	I2C Clock for I2C Slave	
F4	DGDATA	B	3ICUD	3T2	Digital Gyro Data I/F Output (4 Wired)	Digital Gyro I/F Data I/O(3 Wired)	U
						I2C Data for I2C Slave	
F5	OUT3	O		3OA	OIS Driver Output (H-Bridge or Linear)		-
G1	OPINPAF	I	3IA		AF Hall Op-amp Input Plus		-
G2	HLYBO	O		3OA	OIS Hall Y Bias Output		-
G3	HLAFBO	O		3OA	AF Hall Bias Output		-
G4	OUT6	O		3OA	AF Driver Output (H-Bridge, Linear)		-
G5	OUT5	O		3OA	AF Driver Output (H-Bridge, Linear)		-

[How to select the function]

The initial function right after reset is set to be "Function A1" in the below table.
You can change the function by CmIOPN, CmMstMode, CmExtClkSel.

One of Function A,B,C... can be selected by CmIOPN [N=0,1,2,...10] register.

	Primary Function	Sub Functions
PINNAME	Function A1	Function B
	Function A2	Function C

DGSSB, DGCLK: CmMstMode selects A1 or A2.
EXCLK, EIRQ1: CmExtClkSel selects A1 or A2.

LC898123AXD

Electrical Characteristics

Logic

Absolute Maximum Rating at $V_{SS}=0V$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{AD30} max	$T_a \leq 25^\circ C$	-0.3 to 4.6	V
Input/Output voltage	V_{AI30}, V_{AO30}	$T_a \leq 25^\circ C$	-0.3 to $V_{AD30}+0.3$	V
	V_{DI30}, V_{DO30}	$T_a \leq 25^\circ C$	-0.3 to $V_{AD30}+0.3$	V
Storage temperature	T_{stg}		-55 to 125	$^\circ C$
Operating temperature	T_{opr}		-30 to 85	$^\circ C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ratings at $T_a=-30$ to $85^\circ C$, $V_{SS}=0V$

3.0V Power Supply (AV_{DD30})

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{AD30}	2.6	2.8	3.6	V
Input voltage range	V_{IN}	0	-	V_{AD30}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

D.C. Characteristics at Input/Output $V_{SS}=0V$, $AV_{DD30}=2.6$ to $3.6V$, $T_a=-30$ to $85^\circ C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable I/O
High-level input voltage	V_{IH}	CMOS schmitt	1.48			V	3IS, 3ISUD, 3ISD
Low-level input voltage	V_{IL}				0.37	V	
High-level input voltage	V_{IH}	CMOS supported	1.40				3IC, 3ICUD, 3ICD
Low-level input voltage	V_{IL}				0.51	V	
High-level output voltage	V_{OH}	$I_{OH}=-2mA$	$AV_{DD30}-0.4$			V	3O2, 3T2
Low-level output voltage	V_{OL}	$I_{OL}=2mA$			0.4	V	
Low-level output voltage	V_{OL}	$I_{OL}=2mA$			0.2	V	3OD
Analog input voltage	V_{AI}		AV_{SS}		AV_{DD30}	V	3IA
PullUp resistor	R_{up}		50		200	k Ω	3ICUD, 3ISUD
PullDown resistor	R_{dn}		50		220	k Ω	3ICUD, 3ISUD, 3ISD, 3ICD

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Non-volatile Memory Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Endurance	EN				1000	Cycles
Data retention	RT		10			Years

LC898123AXD

Driver

Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Symbol
Power supply voltage	VM max		4.6	V
Output peak current	I _{opeak}	OUT1 to 4 T ≤ 10ms, ON-duty ≤ 20%	300	mA
		OUT5, OUT6 t ≤ 10ms, ON-duty ≤ 20%	200	mA
Output continuous current	I _{omax}	OUT1 to 4	220	mA
		OUT5, OUT6	150	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Range

Parameter	Symbol	Condition	Ratings	Symbol
Ambient temperature	Topg		−30 to +85	°C
Power supply voltage	VM		2.6 to 3.6	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

H-Bridge Driver Output Characteristics at Ta=25°C, AV_{DD30}=VM=3.0V

Parameter	Symbol	Condition	Ratings (Ω)	Symbol
Output ON resistance OUT1 to OUT4	R _{onu}	I _o =220mA (Pch)	1.1	Ω
	R _{ond}	I _o =220mA (Nch)	1.3(*)	Ω
Output ON resistance OUT5, OUT6	R _{onu}	I _o =150mA (Pch)	1.5	Ω
	R _{ond}	I _o =150mA (Nch)	1.4(*)	Ω

(*) include Constant current detect resistance

Constant Current Driver Output at Ta=25°C, AV_{DD30}=VM=2.8V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Current OUT1 to OUT4	I _{full}	OIS_DA[10:0]=7FFh OIS_DB[10:0]=7FFh	185.5	195.0	205.0	mA
Output Current OUT5, OUT6		OP-AF(unidirection) AF_D[9:0]=3FFh		125.0		mA
		OP-AF(bidirection) CL-AF AF_D[9:0]=3FFh		120.0		mA
Compliance Voltage OUT1 to OUT4	V _{comp}		0.4			V
Compliance Voltage OUT5,OUT6		OP-AF(unidirection)	0.4			V
		OP-AF(bidirection) CL-AF	0.5			V

Total output current is less than 500mA.

OP-AF (unidirection)

$$V_{CM} \text{ resistance } (R_{vcm}) = (VM - V_{comp}) / I_o [\Omega]$$

OP-AF (bidirection) / CL-AF / OIS

$$V_{CM} \text{ resistance } (R_{vcm}) = (VM - (R_{onu} \times I_o + V_{comp})) / I_o [\Omega]$$

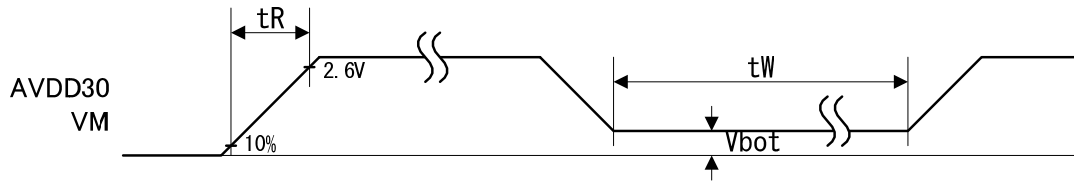
$$\text{Output ON resistance } (R_{on}) = VM / I_o - R_{vcm} [\Omega]$$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

LC898123AXD

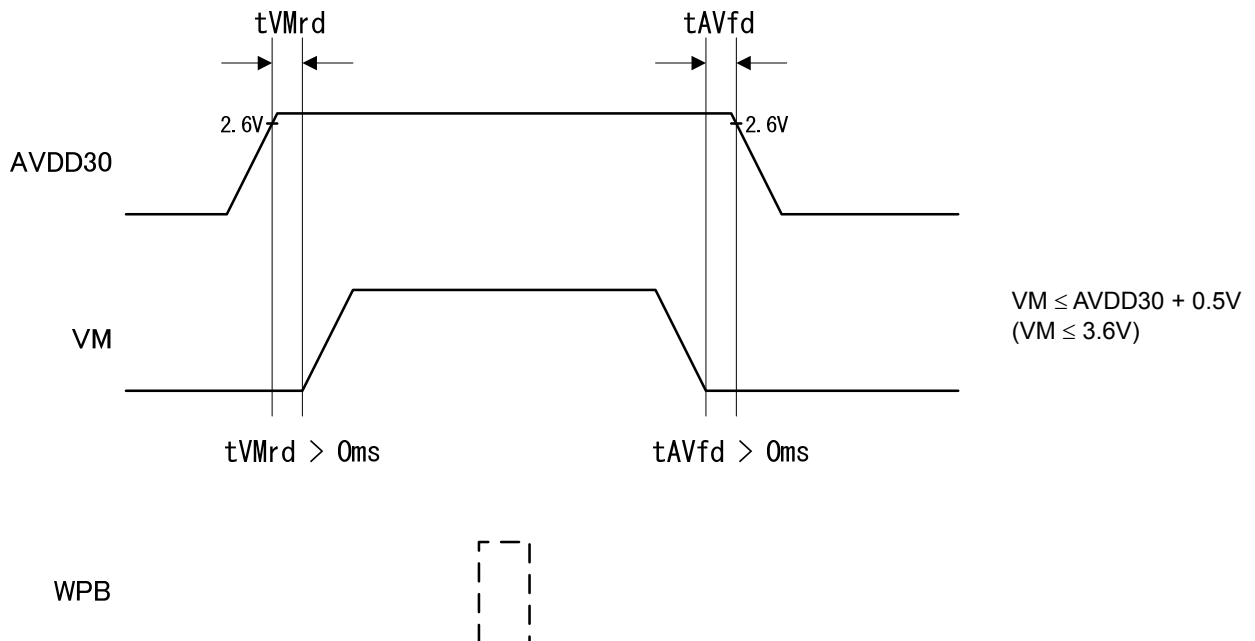
AC Characteristics

Power Sequence



Item	Symbol	Min	Typ	Max	Units
Rise time	t_R			5	ms
Wait time	t_W	100			ms
Bottom Voltage	V_{bot}			0.2	V

Injection order between AVDD30 and VM is below.



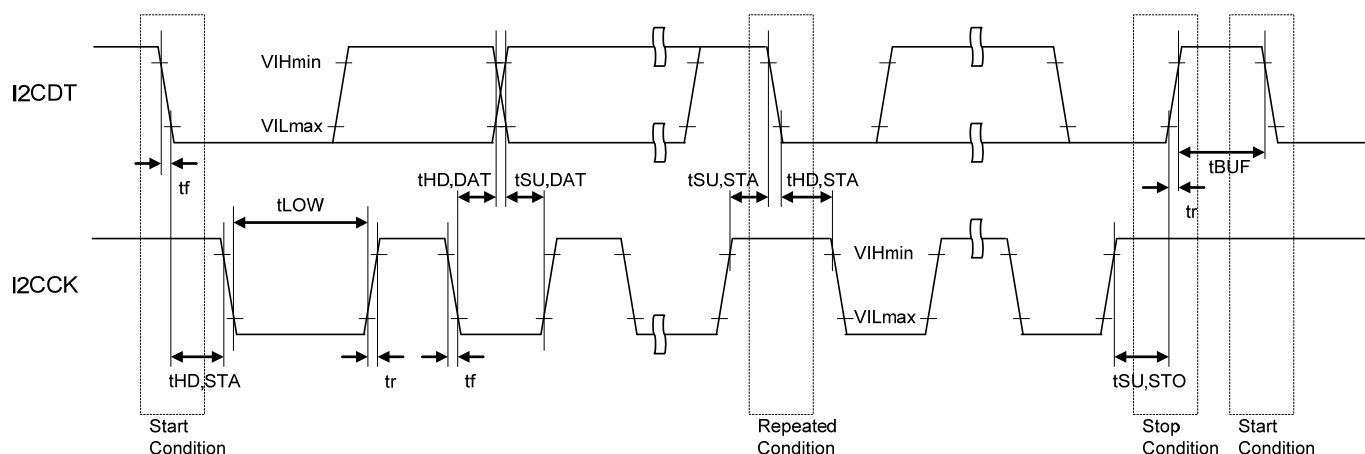
WPB must be open or pull down normally. When Erase or Program is made to Flash, WPB have to be High. Before power off of AVDD, Flash I/F must reset and OSC must set to standby. I2CDT, I2CCK, EXCLK and EIRQ0 tolerate 3V input at the time of power off.

The data in the flash memory may be rewritten if you do not keep specifications. And it is forbidden to power off during flash access. The data in the flash memory may be rewritten.

LC898123AXD

2-wire serial Interface Timing

The communication protocol is compatible with I²C (Fast mode Plus). This circuit has clock stretch function.



I²C interface timing definition

Item	Symbol	Pin name	Min	Typ	Max	Units
SCL clock frequency	Fscl	I2CCK			1000	kHz
START condition hold time	tHD,STA	I2CCK I2CDT	0.26			μs
SCL clock Low period	tLOW	I2CCK	0.5			μs
SCL clock High period	tHIGH	I2CCK	0.26			μs
Setup time for repetition START condition	tSU,STA	I2CCK I2CDT	0.26			μs
Data hold time	tHD,DAT	I2CCK I2CDT	0 (*1)		0.9	μs
Data setup time	tSU,DAT	I2CCK I2CDT	50			ns
SDA, SCL rising time	tr	I2CCK I2CDT			120	ns
SDA, SCL falling time	tf	I2CCK I2CDT			120	ns
STOP condition setup time	tSU,STO	I2CCK I2CDT	0.26			μs
Bus free time between STOP and START	tBUF	I2CCK I2CDT	0.5			μs

(*1) Although the I²C specification defines a condition that 300 ns of hold time is required internally, LC898123AXD is designed for a condition with typ. 100 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

LC898123AXD

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC898123AXD-VH	WLCSP35, 3.39x2.3 (Pb-Free / Halogen Free)	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

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