

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Test conditions	Value	Unit
$V_S$	Supply Voltage	$V_{SA} = V_{SB} = V_S$	60	V
$V_{OD}$	Differential Voltage between $V_{SA}$ , $OUT1_A$ , $OUT2_A$ , $SENSE_A$ and $V_{SB}$ , $OUT1_B$ , $OUT2_B$ , $SENSE_B$	$V_{SA} = V_{SB} = V_S = 60V$ ; $V_{SENSE_A} = V_{SENSE_B} = GND$	60	V
$V_{BOOT}$	Bootstrap Peak Voltage	$V_{SA} = V_{SB} = V_S$	$V_S + 10$	V
$V_{IN}, V_{EN}$	Input and Enable Voltage Range		-0.3 to +7	V
$V_{SENSE_A}$ , $V_{SENSE_B}$	Voltage Range at pins $SENSE_A$ and $SENSE_B$		-1 to +4	V
$I_{S(peak)}$	Pulsed Supply Current (for each $V_S$ pin), internally limited by the overcurrent protection	$V_{SA} = V_{SB} = V_S$ ; $t_{PULSE} < 1ms$	7.1	A
$I_S$	RMS Supply Current (for each $V_S$ pin)	$V_{SA} = V_{SB} = V_S$	2.8	A
$T_{stg, TOP}$	Storage and Operating Temperature Range		-40 to 150	°C

**RECOMMENDED OPERATING CONDITIONS**

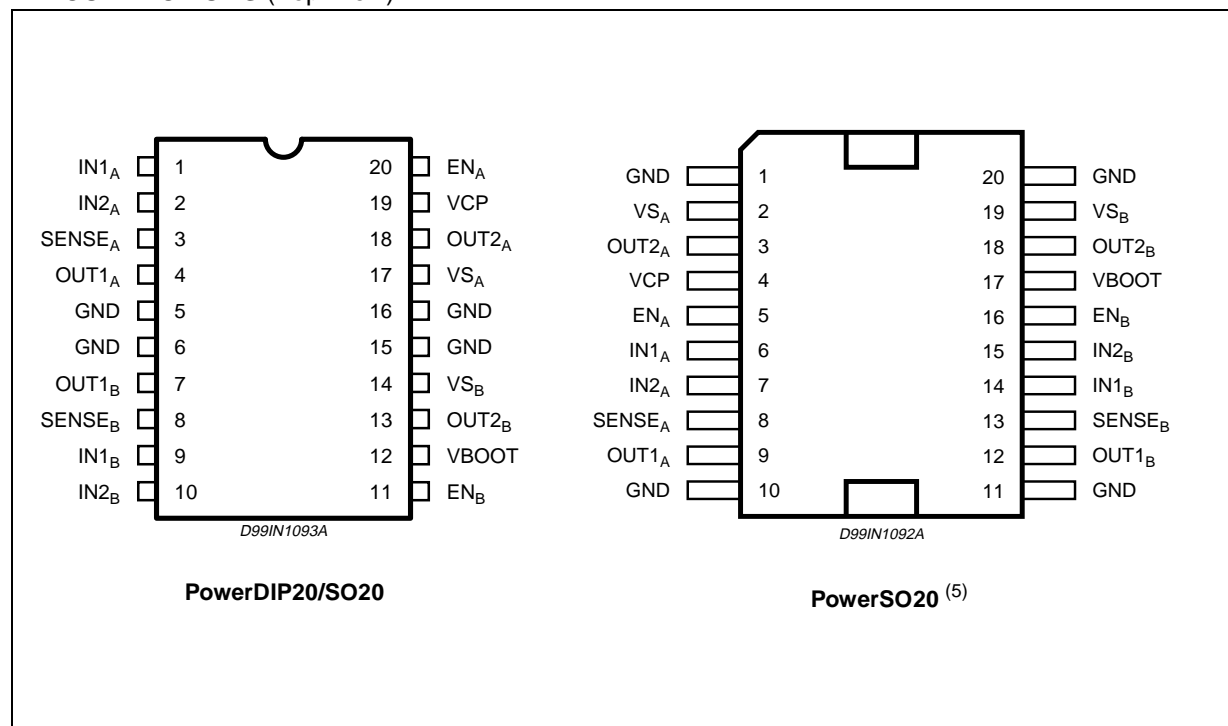
Symbol	Parameter	Test Conditions	MIN	MAX	Unit
$V_S$	Supply Voltage	$V_{SA} = V_{SB} = V_S$	8	52	V
$V_{OD}$	Differential Voltage Between $V_{SA}$ , $OUT1_A$ , $OUT2_A$ , $SENSE_A$ and $V_{SB}$ , $OUT1_B$ , $OUT2_B$ , $SENSE_B$	$V_{SA} = V_{SB} = V_S$ ; $V_{SENSE_A} = V_{SENSE_B}$		52	V
$V_{SENSE_A}$ , $V_{SENSE_B}$	Voltage Range at pins $SENSE_A$ and $SENSE_B$	(pulsed $t_W < t_{rr}$ ) (DC)	-6 -1	6 1	V V
$I_{OUT}$	RMS Output Current			2.8	A
$T_j$	Operating Junction Temperature		-25	+125	°C
$f_{sw}$	Switching Frequency			100	KHz

## THERMAL DATA

Symbol	Description	PowerDIP20	SO20	PowerSO20	Unit
R <sub>th-j-pins</sub>	Maximum Thermal Resistance Junction-Pins	12	14	-	°C/W
R <sub>th-j-case</sub>	Maximum Thermal Resistance Junction-Case	-	-	1	°C/W
R <sub>th-j-amb1</sub>	Maximum Thermal Resistance Junction-Ambient <sup>1</sup>	40	51	-	°C/W
R <sub>th-j-amb1</sub>	Maximum Thermal Resistance Junction-Ambient <sup>2</sup>	-	-	35	°C/W
R <sub>th-j-amb1</sub>	Maximum Thermal Resistance Junction-Ambient <sup>3</sup>	-	-	15	°C/W
R <sub>th-j-amb2</sub>	Maximum Thermal Resistance Junction-Ambient <sup>4</sup>	56	77	62	°C/W

- (1) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the bottom side of 6cm<sup>2</sup> (with a thickness of 35µm).  
(2) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6cm<sup>2</sup> (with a thickness of 35µm).  
(3) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6cm<sup>2</sup> (with a thickness of 35µm), 16 via holes and a ground layer.  
(4) Mounted on a multi-layer FR4 PCB without any heat sinking surface on the board.

## PIN CONNECTIONS (Top View)



## PIN DESCRIPTION

PACKAGE		Name	Type	Function
SO20/ PowerDIP20	PowerSO20			
PIN #	PIN #			
1	6	IN1 <sub>A</sub>	Logic Input	Bridge A Logic Input 1.
2	7	IN2 <sub>A</sub>	Logic Input	Bridge A Logic Input 2.
3	8	SENSE <sub>A</sub>	Power Supply	Bridge A Source Pin. This pin must be connected to Power Ground directly or through a sensing power resistor.
4	9	OUT1 <sub>A</sub>	Power Output	Bridge A Output 1.
5, 6, 15, 16	1, 10, 11, 20	GND	GND	Signal Ground terminals. In PowerDIP and SO packages, these pins are also used for heat dissipation toward the PCB.
7	12	OUT1 <sub>B</sub>	Power Output	Bridge B Output 1.
8	13	SENSE <sub>B</sub>	Power Supply	Bridge B Source Pin. This pin must be connected to Power Ground directly or through a sensing power resistor.
9	14	IN1 <sub>B</sub>	Logic Input	Bridge B Logic Input 1.
10	15	IN2 <sub>B</sub>	Logic Input	Bridge B Logic Input 2.
11	16	EN <sub>B</sub>	Logic Input <sup>(6)</sup>	Bridge B Enable. LOW logic level switches OFF all Power MOSFETs of Bridge B. This pin is also connected to the collector of the Overcurrent and Thermal Protection transistor to implement over current protection. If not used, it has to be connected to +5V through a resistor.
12	17	VBOOT	Supply Voltage	Bootstrap Voltage needed for driving the upper PowerMOSFETs of both Bridge A and Bridge B.
13	18	OUT2 <sub>B</sub>	Power Output	Bridge B Output 2.
14	19	VS <sub>B</sub>	Power Supply	Bridge B Power Supply Voltage. It must be connected to the supply voltage together with pin VS <sub>A</sub> .
17	2	VS <sub>A</sub>	Power Supply	Bridge A Power Supply Voltage. It must be connected to the supply voltage together with pin VS <sub>B</sub> .
18	3	OUT2 <sub>A</sub>	Power Output	Bridge A Output 2.
19	4	VCP	Output	Charge Pump Oscillator Output.
20	5	EN <sub>A</sub>	Logic Input <sup>(6)</sup>	Bridge A Enable. LOW logic level switches OFF all Power MOSFETs of Bridge A. This pin is also connected to the collector of the Overcurrent and Thermal Protection transistor to implement over current protection. If not used, it has to be connected to +5V through a resistor.

(6) Also connected at the output drain of the Overcurrent and Thermal protection MOSFET. Therefore, it has to be driven putting in series a resistor with a value in the range of 2.2kΩ - 180kΩ, recommended 100kΩ

**ELECTRICAL CHARACTERISTICS**(T<sub>amb</sub> = 25 °C, V<sub>S</sub> = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>StH(ON)</sub>	Turn-on Threshold		6.6	7	7.4	V
V <sub>StH(OFF)</sub>	Turn-off Threshold		5.6	6	6.4	V
I <sub>S</sub>	Quiescent Supply Current	All Bridges OFF; T <sub>j</sub> = -25°C to 125°C <sup>(7)</sup>		5	10	mA
T <sub>j(OFF)</sub>	Thermal Shutdown Temperature			165		°C

**Output DMOS Transistors**

R <sub>DS(ON)</sub>	High-Side Switch ON Resistance	T <sub>j</sub> = 25 °C		0.34	0.4	Ω
		T <sub>j</sub> = 125 °C <sup>(7)</sup>		0.53	0.59	Ω
	Low-Side Switch ON Resistance	T <sub>j</sub> = 25 °C		0.28	0.34	Ω
		T <sub>j</sub> = 125 °C <sup>(7)</sup>		0.47	0.53	Ω
I <sub>DSS</sub>	Leakage Current	EN = Low; OUT = V <sub>S</sub>			2	mA
		EN = Low; OUT = GND	-0.15			mA

**Source Drain Diodes**

V <sub>SD</sub>	Forward ON Voltage	I <sub>SD</sub> = 2.8A, EN = LOW		1.15	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>f</sub> = 2.8A		300		ns
t <sub>fr</sub>	Forward Recovery Time			200		ns

**Logic Input**

V <sub>IL</sub>	Low level logic input voltage		-0.3		0.8	V
V <sub>IH</sub>	High level logic input voltage		2		7	V
I <sub>IL</sub>	Low Level Logic Input Current	GND Logic Input Voltage	-10			μA
I <sub>IH</sub>	High Level Logic Input Current	7V Logic Input Voltage			10	μA
V <sub>th(ON)</sub>	Turn-on Input Threshold			1.8	2.0	V
V <sub>th(OFF)</sub>	Turn-off Input Threshold		0.8	1.3		V
V <sub>th(HYS)</sub>	Input Threshold Hysteresis		0.25	0.5		V

**Switching Characteristics**

t <sub>D(on)EN</sub>	Enable to out turn ON delay time <sup>(8)</sup>	I <sub>LOAD</sub> = 2.8A, Resistive Load	100	250	400	ns
t <sub>D(on)IN</sub>	Input to out turn ON delay time	I <sub>LOAD</sub> = 2.8A, Resistive Load (dead time included)		1.6		μs
t <sub>RISE</sub>	Output rise time <sup>(8)</sup>	I <sub>LOAD</sub> = 2.8A, Resistive Load	40		250	ns
t <sub>D(off)EN</sub>	Enable to out turn OFF delay time <sup>(8)</sup>	I <sub>LOAD</sub> = 2.8A, Resistive Load	300	550	800	ns

**ELECTRICAL CHARACTERISTICS** (continued)

( $T_{amb} = 25\text{ }^{\circ}\text{C}$ ,  $V_s = 48\text{V}$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{D(OFF)IN}$	Input to out turn OFF delay time	$I_{LOAD} = 2.8\text{A}$ , Resistive Load		600		ns
$t_{FALL}$	Output Fall Time <sup>(8)</sup>	$I_{LOAD} = 2.8\text{A}$ , Resistive Load	40		250	ns
$t_{dt}$	Dead Time Protection		0.5	1		$\mu\text{s}$
$f_{CP}$	Charge pump frequency	$-25^{\circ}\text{C} < T_j < 125^{\circ}\text{C}$		0.6	1	MHz

**Over Current Protection**

$I_{SOVER}$	Input Supply Overcurrent Protection Threshold	$T_j = -25^{\circ}\text{C}$ to $125^{\circ}\text{C}$ <sup>(7)</sup>	4	5.6	7.1	A
$R_{OPDR}$	Open Drain ON Resistance	$I = 4\text{mA}$		40	60	$\Omega$
$t_{OCD(ON)}$	OCD Turn-on Delay Time <sup>(9)</sup>	$I = 4\text{mA}$ ; $C_{EN} < 100\text{pF}$		200		ns
$t_{OCD(OFF)}$	OCD Turn-off Delay Time <sup>(9)</sup>	$I = 4\text{mA}$ ; $C_{EN} < 100\text{pF}$		100		ns

(7) Tested at 25°C in a restricted range and guaranteed by characterization.

(8) See Fig. 1.

(9) See Fig. 2.

**Figure 1. Switching Characteristic Definition**

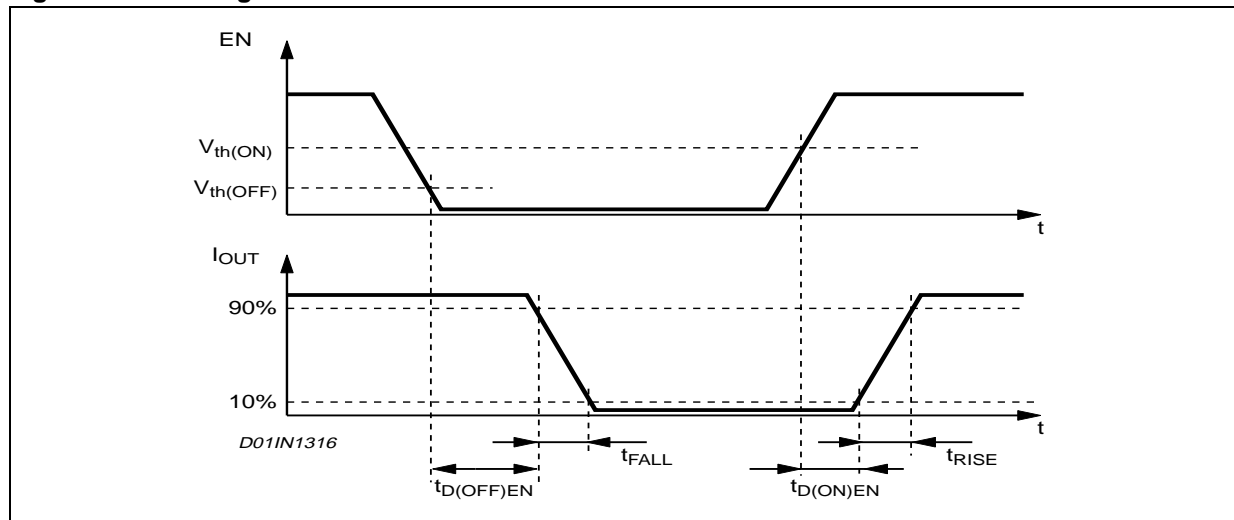
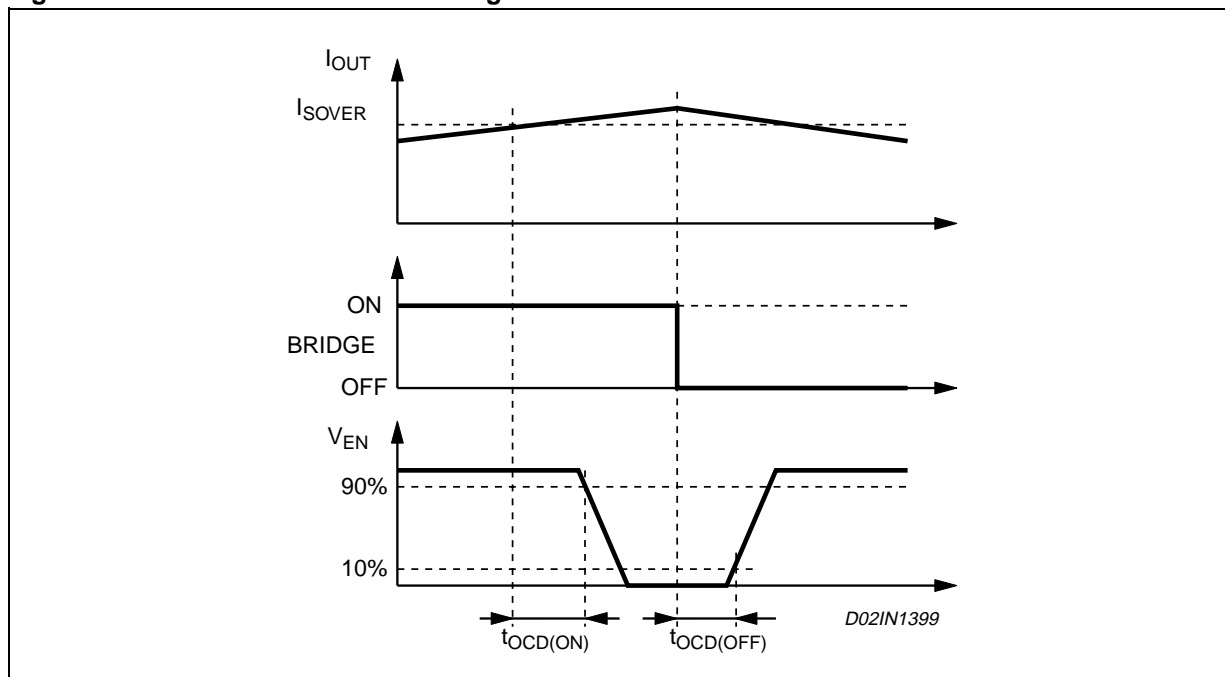


Figure 2. Overcurrent Detection Timing Definition



**CIRCUIT DESCRIPTION**

**POWER STAGES and CHARGE PUMP**

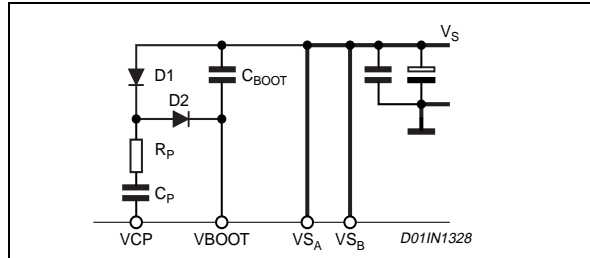
The L6205 integrates two independent Power MOS Full Bridges. Each Power MOS has an  $R_{dson}=0.3\text{ohm}$  (typical value @ 25°C), with intrinsic fast freewheeling diode. Cross conduction protection is achieved using a dead time ( $t_d = 1\mu\text{s}$  typical) between the switch off and switch on of two Power MOS in one leg of a bridge.

Using N Channel Power MOS for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The Bootstrapped (Vboot) supply is obtained through an internal Oscillator and few external components to realize a charge pump circuit as shown in Figure 3. The oscillator output (VCP) is a square wave at 600kHz (typical) with 10V amplitude. Recommended values/part numbers for the charge pump circuit are shown in Table1.

**Table 1. Charge Pump External Components Values**

C <sub>BOOT</sub>	220nF
C <sub>P</sub>	10nF
R <sub>P</sub>	100Ω
D1	1N4148
D2	1N4148

**Figure 3. Charge Pump Circuit**



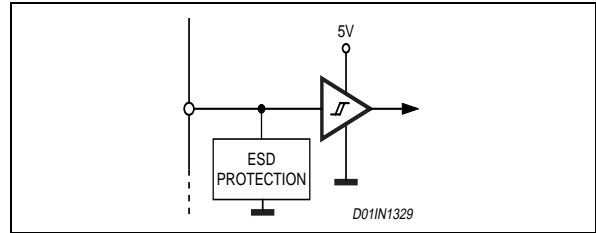
**LOGIC INPUTS**

Pins IN1<sub>A</sub>, IN2<sub>A</sub>, IN1<sub>B</sub> and IN2<sub>B</sub> are TTL/CMOS and μC compatible logic inputs. The internal structure is shown in Fig. 4. Typical value for turn-on and turn-off thresholds are respectively  $V_{thon}=1.8\text{V}$  and  $V_{thoff}=1.3\text{V}$ .

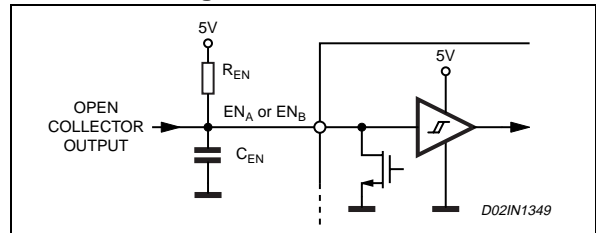
Pins EN<sub>A</sub> and EN<sub>B</sub> have identical input structure with the exception that the drains of the Overcurrent and thermal protection MOSFETs (one for the Bridge A and one for the Bridge B) are also connected to these pins. Due to these connections some care needs to be taken in driving these pins. The EN<sub>A</sub> and EN<sub>B</sub> inputs may be driven in one of two configurations as shown in figures 5 or 6. If driven by an open drain

(collector) structure, a pull-up resistor  $R_{EN}$  and a capacitor  $C_{EN}$  are connected as shown in Fig. 5. If the driver is a standard Push-Pull structure the resistor  $R_{EN}$  and the capacitor  $C_{EN}$  are connected as shown in Fig. 6. The resistor  $R_{EN}$  should be chosen in the range from 2.2kΩ to 180KΩ. Recommended values for  $R_{EN}$  and  $C_{EN}$  are respectively 100KΩ and 5.6nF. More information on selecting the values is found in the Overcurrent Protection section.

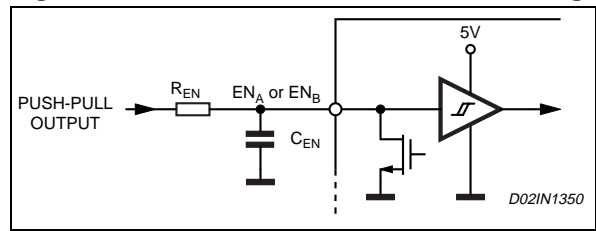
**Figure 4. Logic Inputs Internal Structure**



**Figure 5. EN<sub>A</sub> and EN<sub>B</sub> Pins Open Collector Driving**



**Figure 6. EN<sub>A</sub> and EN<sub>B</sub> Pins Push-Pull Driving**



**TRUTH TABLE**

INPUTS			OUTPUTS	
EN	IN1	IN2	OUT1	OUT2
L	X	X	High Z	High Z
H	L	L	GND	GND
H	H	L	V <sub>s</sub>	GND
H	L	H	GND	V <sub>s</sub>
H	H	H	V <sub>s</sub>	V <sub>s</sub>

X = Don't care

High Z = High Impedance Output

## NON-DISSIPATIVE OVERCURRENT PROTECTION

The L6205 integrates an Overcurrent Detection Circuit (OCD). This circuit provides protection against a short circuit to ground or between two phases of the bridge. With this internal over current detection, the external current sense resistor normally used and its associated power dissipation are eliminated. Figure 7 shows a simplified schematic of the overcurrent detection circuit.

To implement the over current detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high side power MOS. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current  $I_{REF}$ . When the output current in one bridge reaches the detection threshold (typically 5.6A) the relative OCD comparator signals a fault condition. When a fault condition is detected, the EN pin is pulled below the turn off threshold (1.3V typical) by an internal open drain MOS with a pull down capability of 4mA. By using an external R-C on the EN pin, the off time before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs.

**Figure 7. Overcurrent Protection Simplified Schematic**

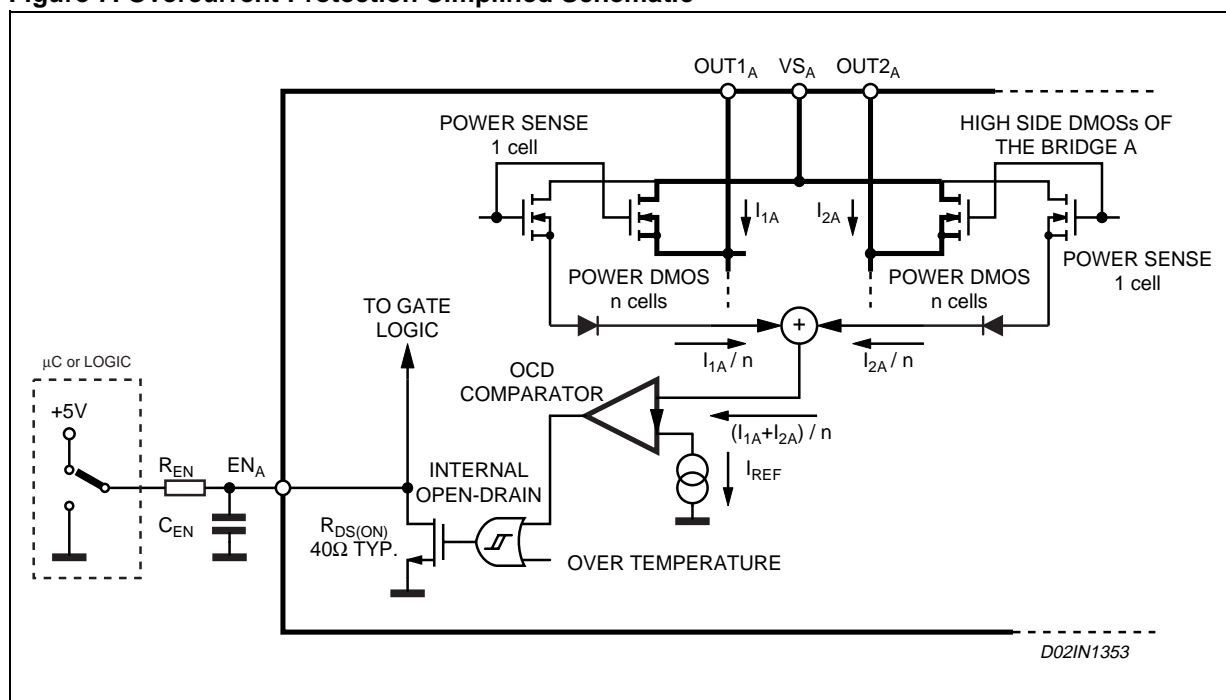


Figure 8 shows the Overcurrent Detection operation. The Disable Time  $t_{DISABLE}$  before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected whether by  $C_{EN}$  and  $R_{EN}$  values and its magnitude is reported in Figure 9. The Delay Time  $t_{DELAY}$  before turning off the bridge when an overcurrent has been detected depends only by  $C_{EN}$  value. Its magnitude is reported in Figure 10.

$C_{EN}$  is also used for providing immunity to pin EN against fast transient noises. Therefore the value of  $C_{EN}$  should be chosen as big as possible according to the maximum tolerable Delay Time and the  $R_{EN}$  value should be chosen according to the desired Disable Time.

The resistor  $R_{EN}$  should be chosen in the range from 2.2KΩ to 180KΩ. Recommended values for  $R_{EN}$  and  $C_{EN}$  are respectively 100KΩ and 5.6nF that allow obtaining 200μs Disable Time.



Figure 8. Overcurrent Protection Waveforms

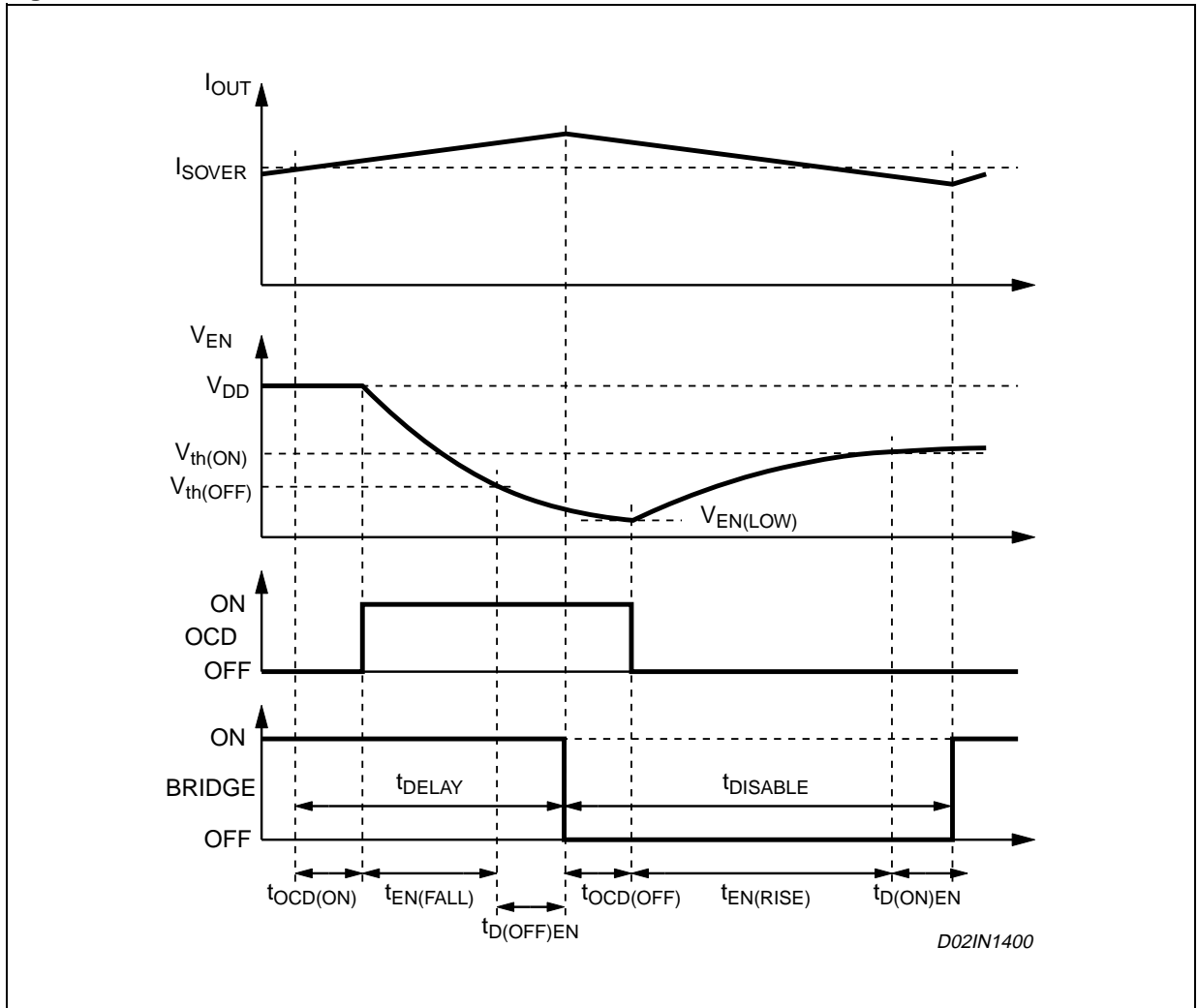
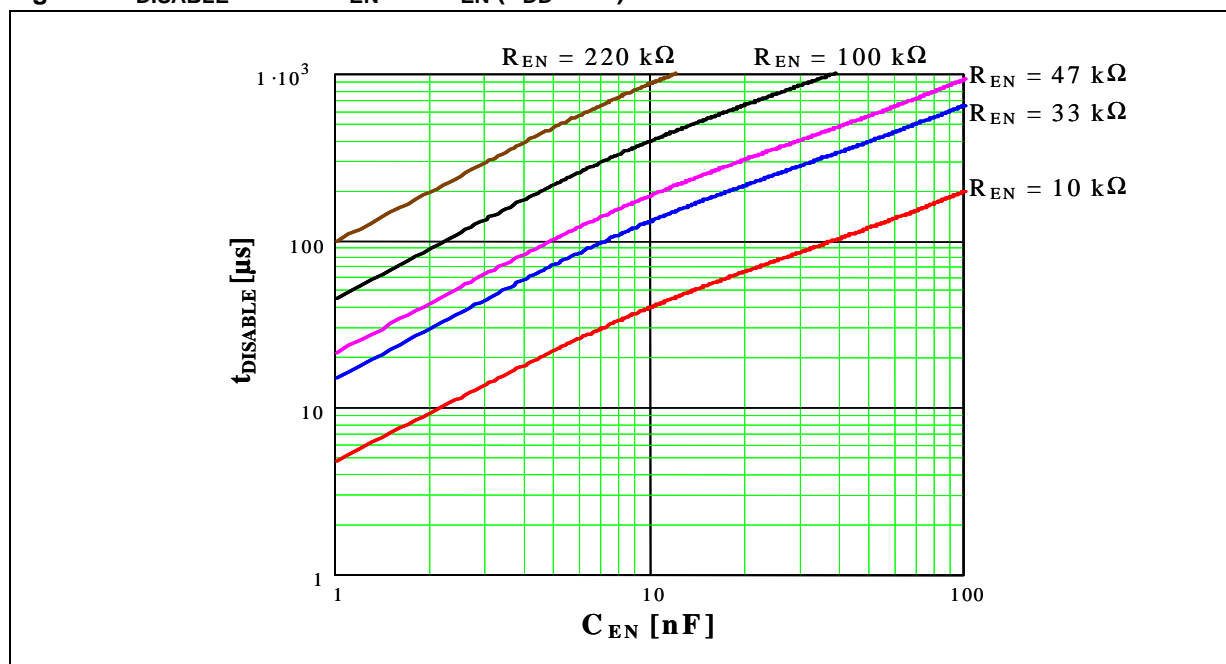
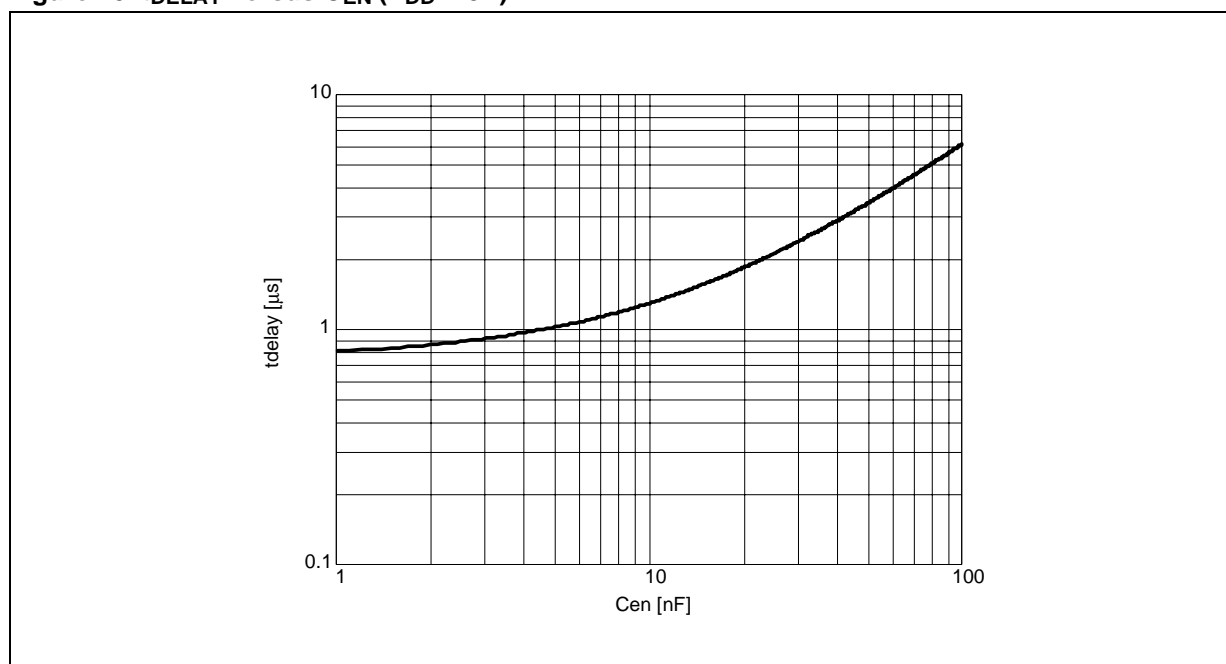


Figure 9.  $t_{\text{DISABLE}}$  versus  $C_{\text{EN}}$  and  $R_{\text{EN}}$  ( $V_{\text{DD}} = 5\text{V}$ ).Figure 10.  $t_{\text{DELAY}}$  versus  $C_{\text{EN}}$  ( $V_{\text{DD}} = 5\text{V}$ ).

### THERMAL PROTECTION

In addition to the Overcurrent Protection, the L6205 integrates a Thermal Protection for preventing the device destruction in case of junction over temperature. It works sensing the die temperature by means of a sensible element integrated in the die. The device switch-off when the junction temperature reaches 165°C (typ. value) with 15°C hysteresis (typ. value).

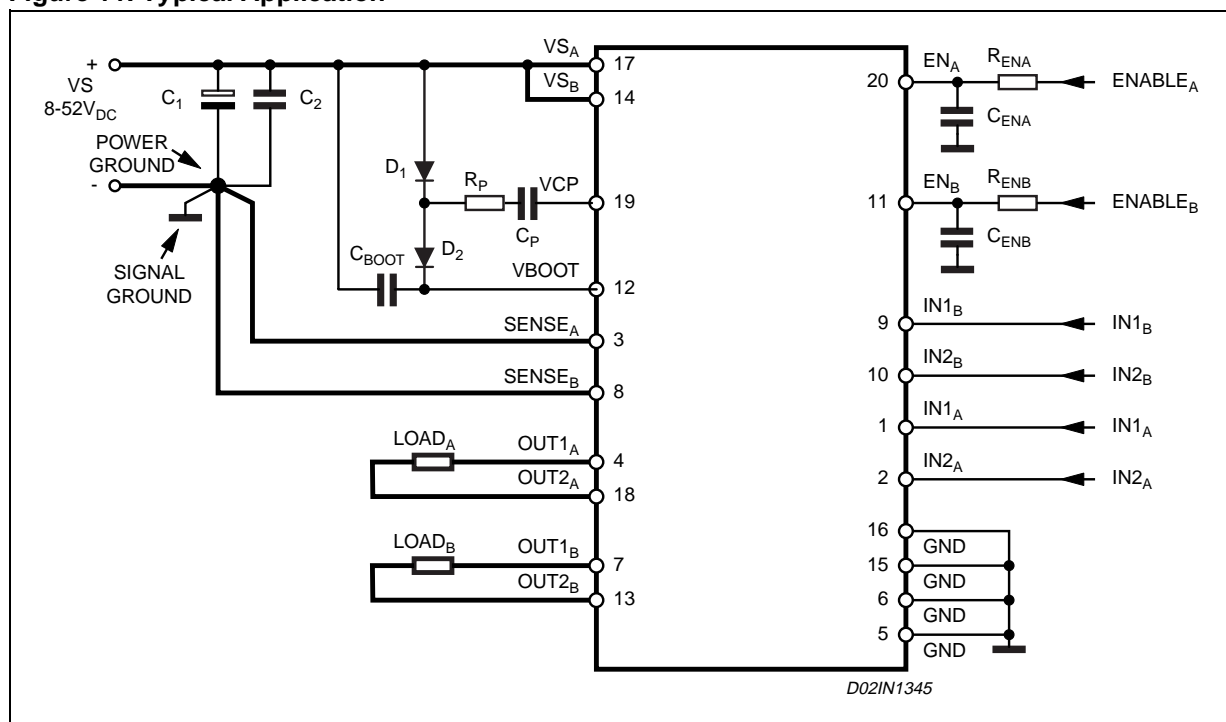
**APPLICATION INFORMATION**

A typical application using L6205 is shown in Fig. 11. Typical component values for the application are shown in Table 2. A high quality ceramic capacitor in the range of 100 to 200 nF should be placed between the power pins ( $VS_A$  and  $VS_B$ ) and ground near the L6205 to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitors connected from the  $EN_A$  and  $EN_B$  inputs to ground set the shut down time for the Bridge A and Bridge B respectively when an over current is detected (see Overcurrent Protection). The two current sources ( $SENSE_A$  and  $SENSE_B$ ) should be connected to Power Ground with a trace length as short as possible in the layout. To increase noise immunity, unused logic pins (except  $EN_A$  and  $EN_B$ ) are best connected to 5V (High Logic Level) or GND (Low Logic Level) (see pin description). It is recommended to keep Power Ground and Signal Ground separated on PCB.

**Table 2. Component Values for Typical Application**

$C_1$	100uF	$D_1$	1N4148
$C_2$	100nF	$D_2$	1N4148
$C_{BOOT}$	220nF	$R_{ENA}$	100k $\Omega$
$C_P$	10nF	$R_{ENB}$	100k $\Omega$
$C_{ENA}$	5.6nF	$R_P$	100 $\Omega$
$C_{ENB}$	5.6nF		

**Figure 11. Typical Application**



## PARALLELED OPERATION

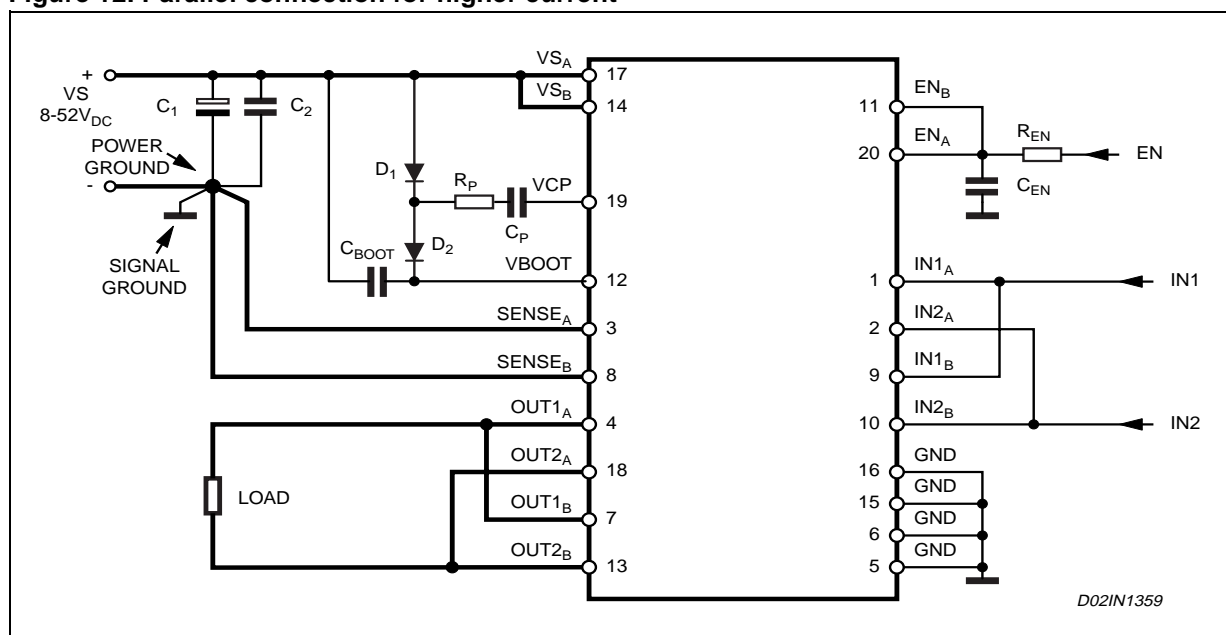
The outputs of the L6205 can be paralleled to increase the output current capability or reduce the power dissipation in the device at a given current level. It must be noted, however, that the internal wire bond connections from the die to the power or sense pins of the package must carry current in both of the associated half bridges. When the two halves of one full bridge (for example OUT1<sub>A</sub> and OUT2<sub>A</sub>) are connected in parallel, the peak current rating is not increased since the total current must still flow through one bond wire on the power supply or sense pin. In addition, the over current detection senses the sum of the current in the upper devices of each bridge (A or B) so connecting the two halves of one bridge in parallel does not increase the over current detection threshold.

For most applications the recommended configuration is Half Bridge 1 of Bridge A paralleled with the Half Bridge 1 of the Bridge B, and the same for the Half Bridges 2 as shown in Figure 12. The current in the two devices connected in parallel will share very well since the  $R_{DS(ON)}$  of the devices on the same die is well matched.

In this configuration the resulting Bridge has the following characteristics.

- Equivalent Device: FULL BRIDGE
- $R_{DS(ON)}$  0.15 $\Omega$  Typ. Value @  $T_J = 25^\circ\text{C}$
- 5.6A max RMS Load Current
- 11.2A OCD Threshold

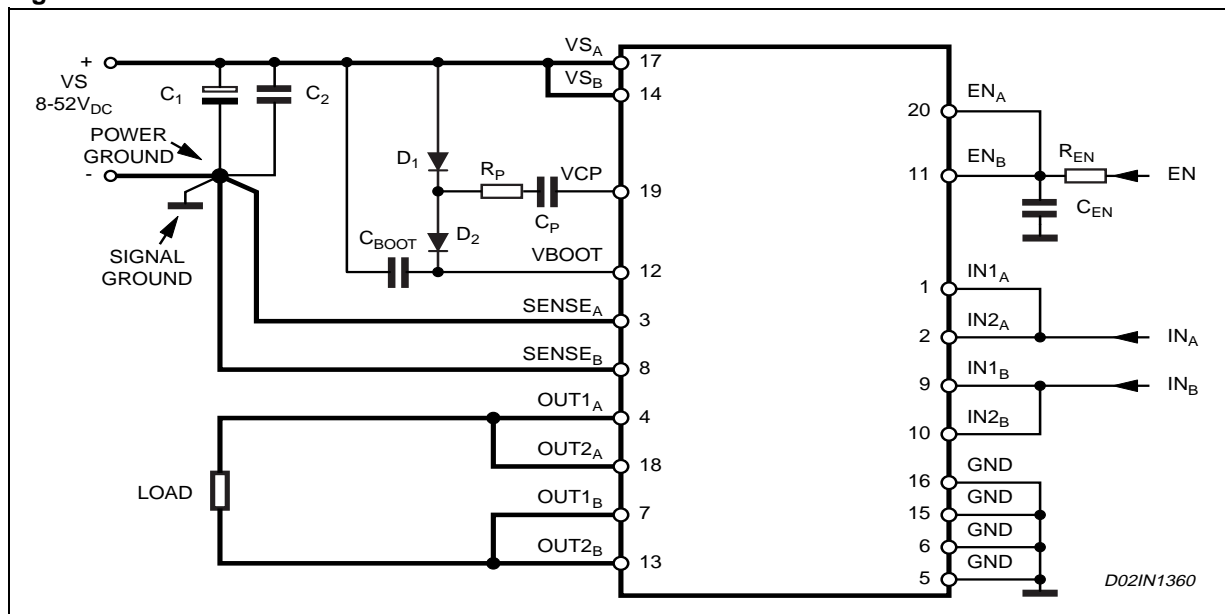
**Figure 12. Parallel connection for higher current**



To operate the device in parallel and maintain a lower over current threshold, Half Bridge 1 and the Half Bridge 2 of the Bridge A can be connected in parallel and the same done for the Bridge B as shown in Figure 13. In this configuration, the peak current for each half bridge is still limited by the bond wires for the supply and sense pins so the dissipation in the device will be reduced, but the peak current rating is not increased. This configuration, the resulting bridge has the following characteristics.

- Equivalent Device: FULL BRIDGE
- $R_{DS(ON)}$  0.15 $\Omega$  Typ. Value @  $T_J = 25^\circ\text{C}$
- 2.8A max RMS Load Current
- 5.6A OCD Threshold

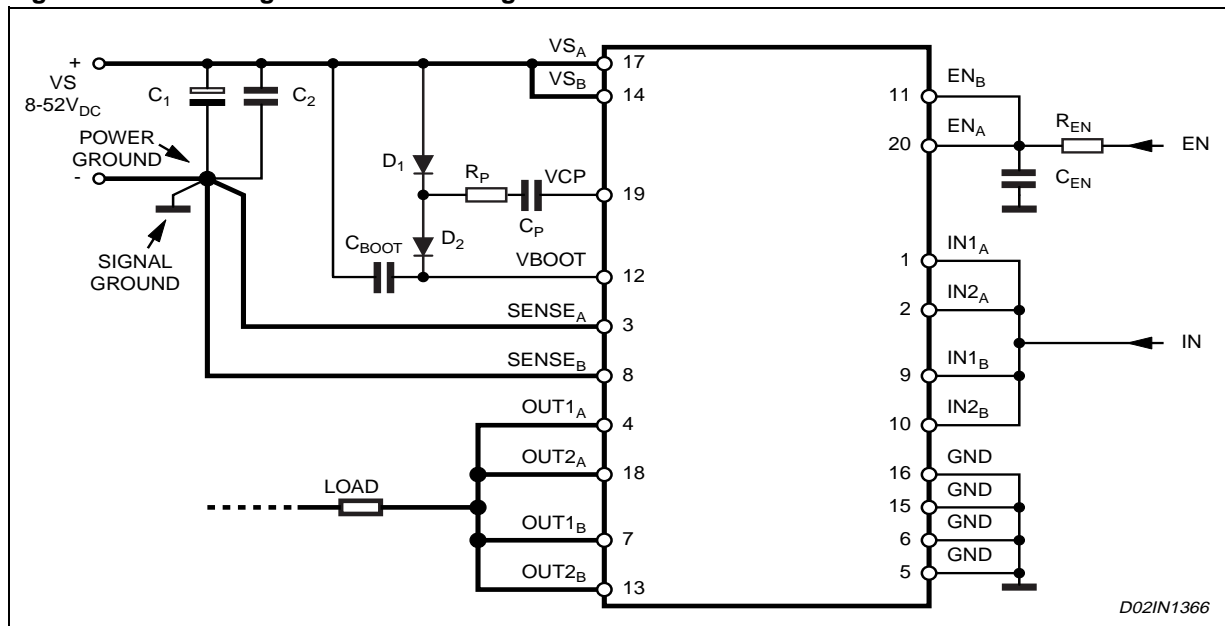
Figure 13. Parallel connection with lower Overcurrent Threshold



It is also possible to parallel the four Half Bridges to obtain a simple Half Bridge as shown in Fig. 14. The resulting half bridge has the following characteristics.

- Equivalent Device: HALF BRIDGE
- $R_{DS(ON)}$  0.075Ω Typ. Value @  $T_J = 25^\circ\text{C}$
- 5.6A max RMS Load Current
- 11.2A OCD Threshold

Figure 14. Paralleling the four Half Bridges

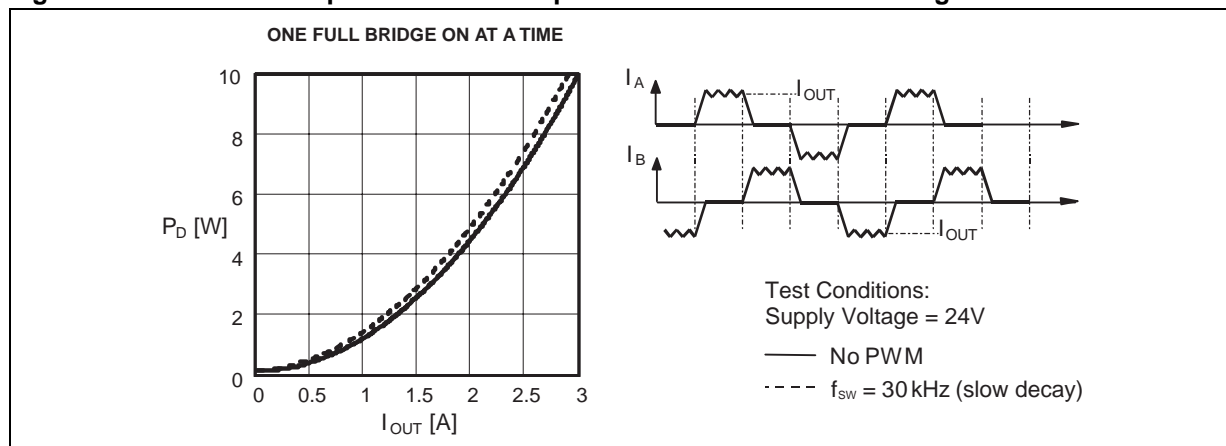


### OUTPUT CURRENT CAPABILITY AND IC POWER DISSIPATION

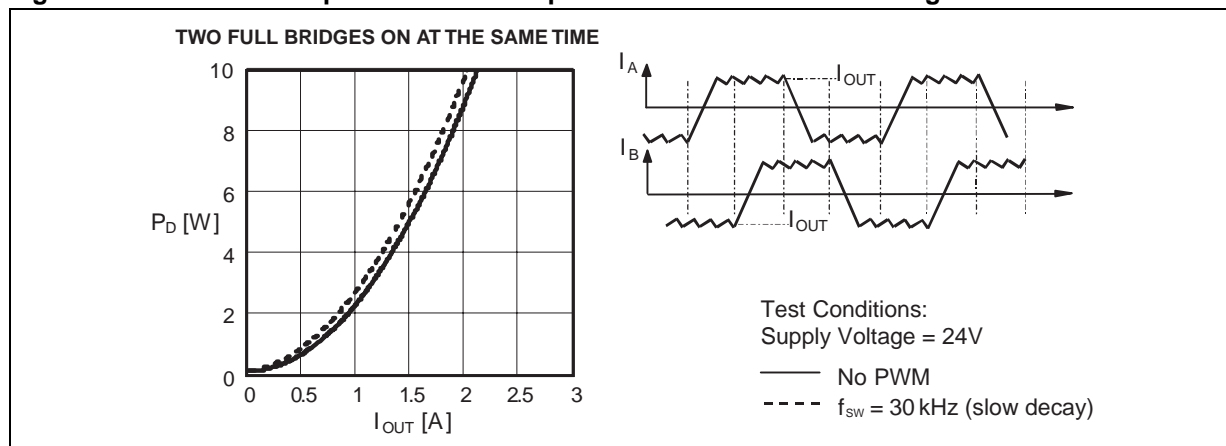
In Fig. 15 and Fig. 16 are shown the approximate relation between the output current and the IC power dissipation using PWM current control driving two loads, for two different driving types:

- One Full Bridge ON at a time (Fig. 15) in which only one load at a time is energized.
  - Two Full Bridges ON at the same time (Fig. 16) in which two loads at the same time are energized.
- For a given output current and driving type the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large must be the on-board copper dissipating area to guarantee a safe operating junction temperature (125°C maximum).

**Figure 15. IC Power Dissipation versus Output Current with One Full Bridge ON at a time.**



**Figure 16. IC Power Dissipation versus Output Current with Two Full Bridges ON at the same time.**



### THERMAL MANAGEMENT

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Therefore, it has to be taken into account very carefully. Besides the available space on the PCB, the right package should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness. Figures 18, 19 and 20 show the Junction-to-Ambient Thermal Resistance values for the PowerSO20, PowerDIP20 and SO20 packages.

For instance, using a PowerSO package with copper slug soldered on a 1.5 mm copper thickness FR4 board with 6cm<sup>2</sup> dissipating footprint (copper thickness of 35µm), the  $R_{thj-amb}$  is about 35°C/W. Fig. 17 shows mounting methods for this package. Using a multi-layer board with vias to a ground plane, thermal impedance can be reduced down to 15°C/W.

Figure 17. Mounting the PowerSO package.

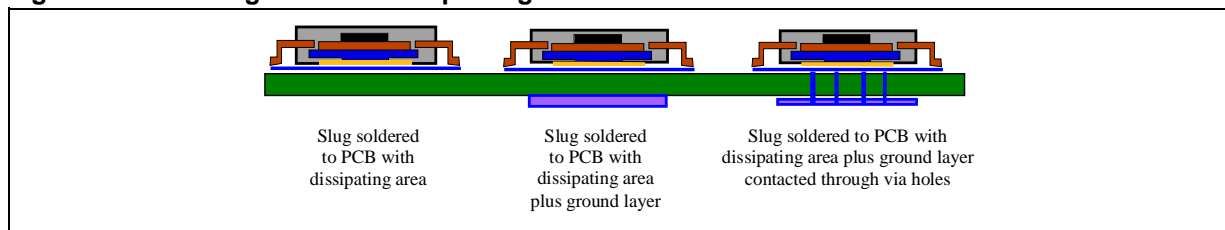


Figure 18. PowerSO20 Junction-Ambient thermal resistance versus on-board copper area.

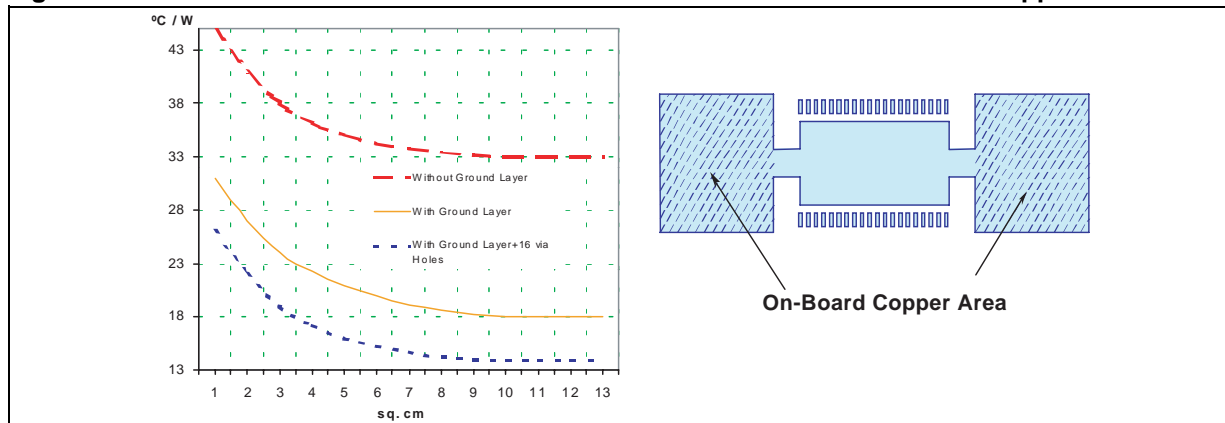


Figure 19. PowerDIP20 Junction-Ambient thermal resistance versus on-board copper area.

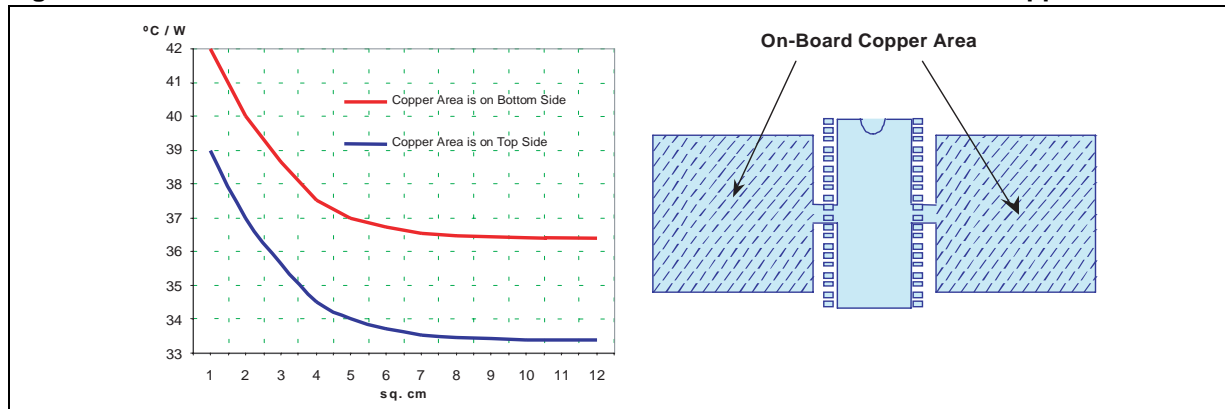
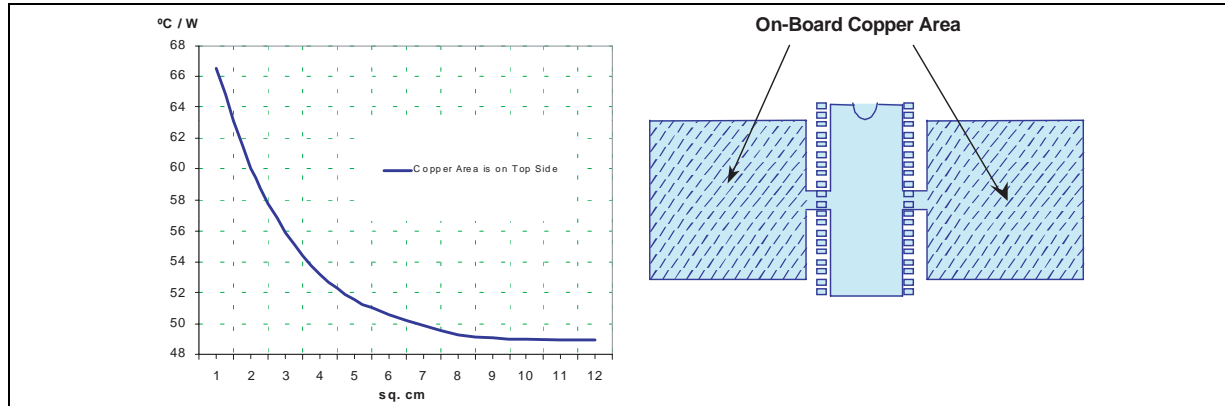
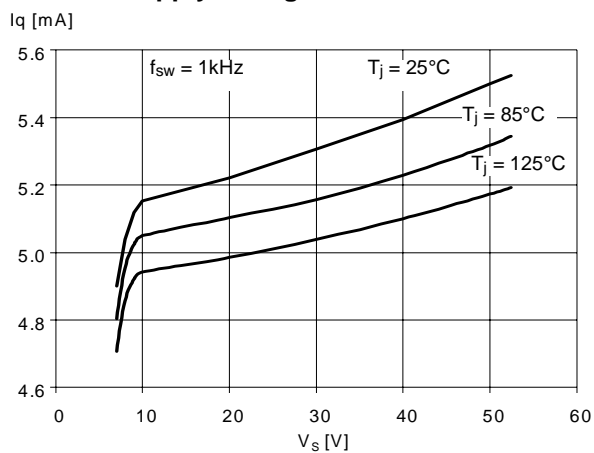


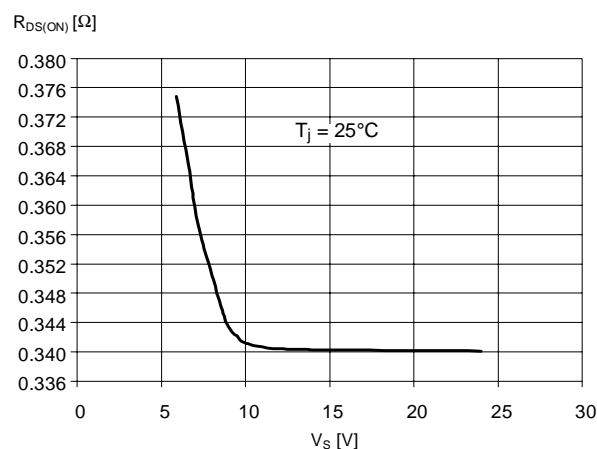
Figure 20. SO20 Junction-Ambient thermal resistance versus on-board copper area.



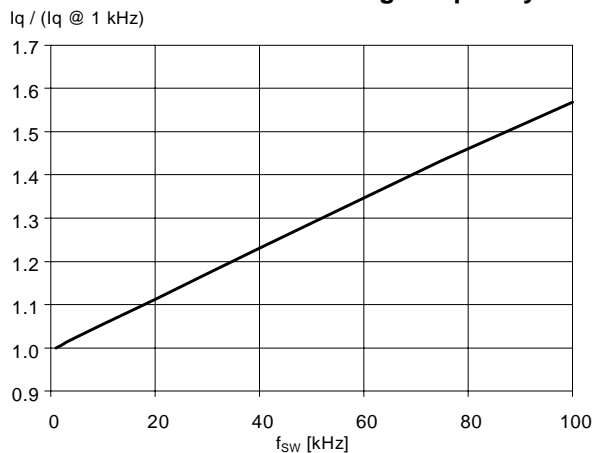
**Figure 21. Typical Quiescent Current vs. Supply Voltage**



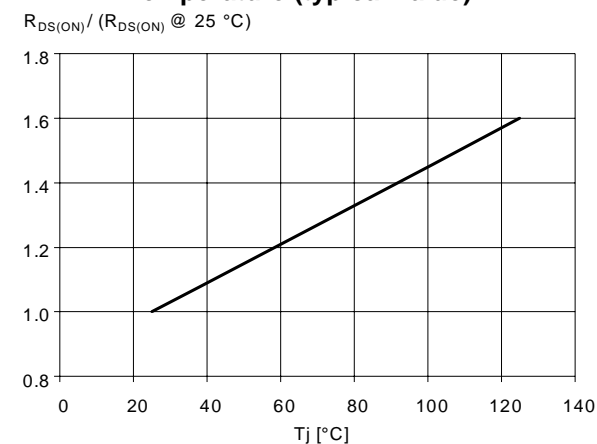
**Figure 24. Typical High-Side  $R_{DS(ON)}$  vs. Supply Voltage**



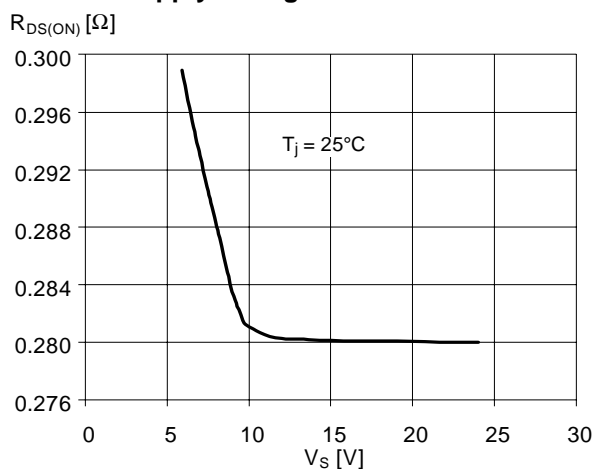
**Figure 22. Normalized Typical Quiescent Current vs. Switching Frequency**



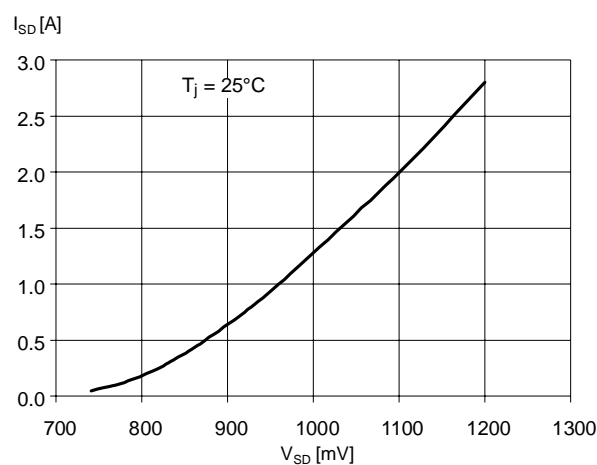
**Figure 25. Normalized  $R_{DS(ON)}$  vs. Junction Temperature (typical value)**



**Figure 23. Typical Low-Side  $R_{DS(ON)}$  vs. Supply Voltage**



**Figure 26. Typical Drain-Source Diode Forward ON Characteristic**



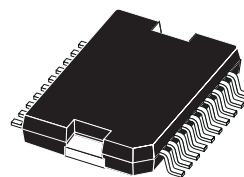


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8° (typ.)					
S	8° (max.)					
T		10			0.394	

(1) "D and E1" do not include mold flash or protusions.  
 - Mold flash or protusions shall not exceed 0.15mm (0.006")  
 - Critical dimensions: "E", "G" and "a3".

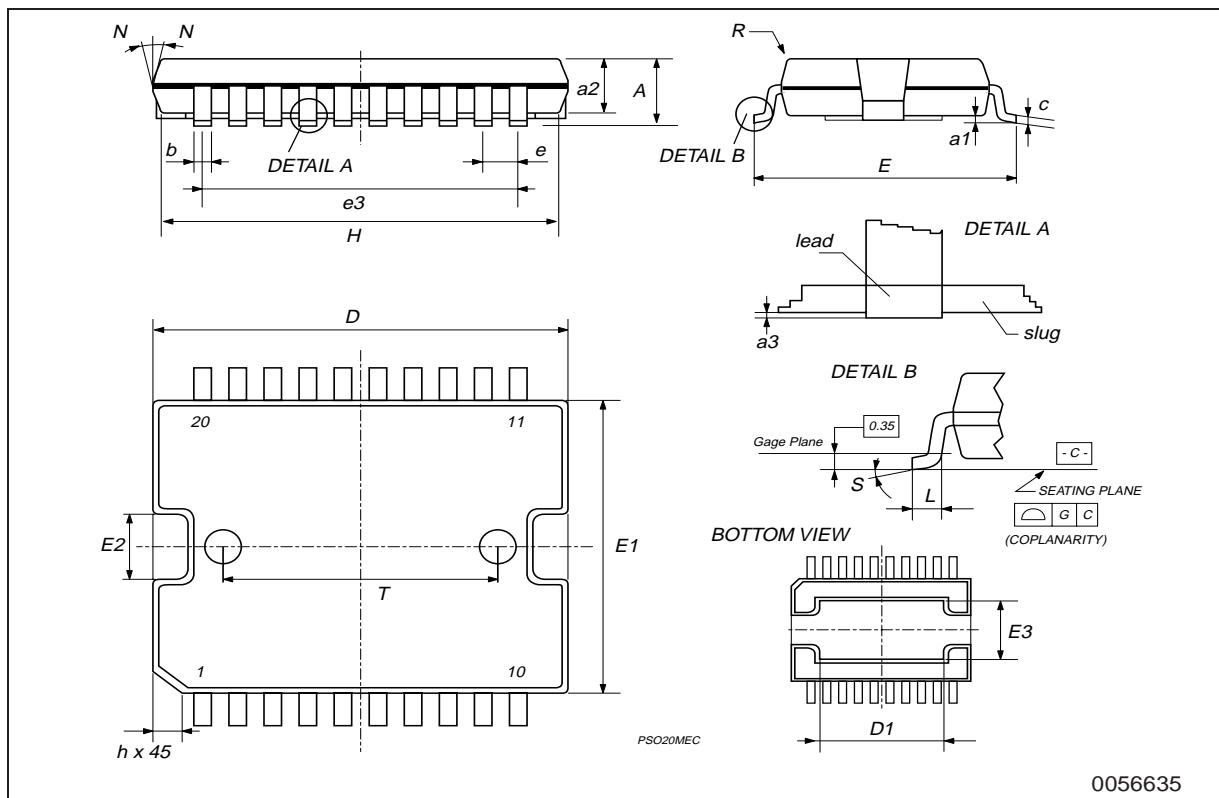
### OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



JEDEC MO-166

PowerSO20

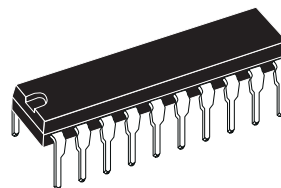


0056635

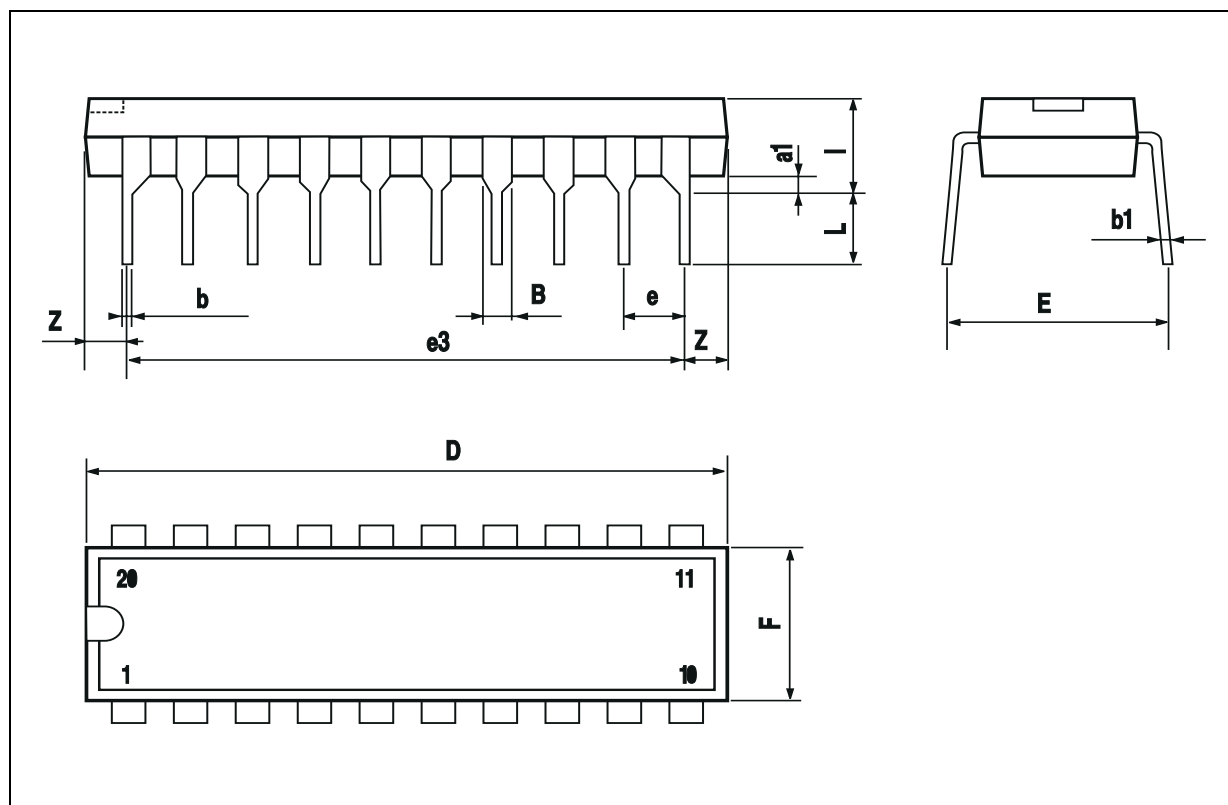


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

## OUTLINE AND MECHANICAL DATA

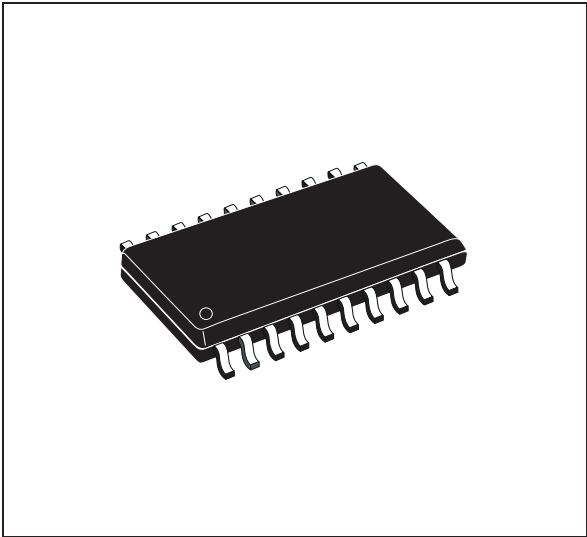


**Powerdip 20**

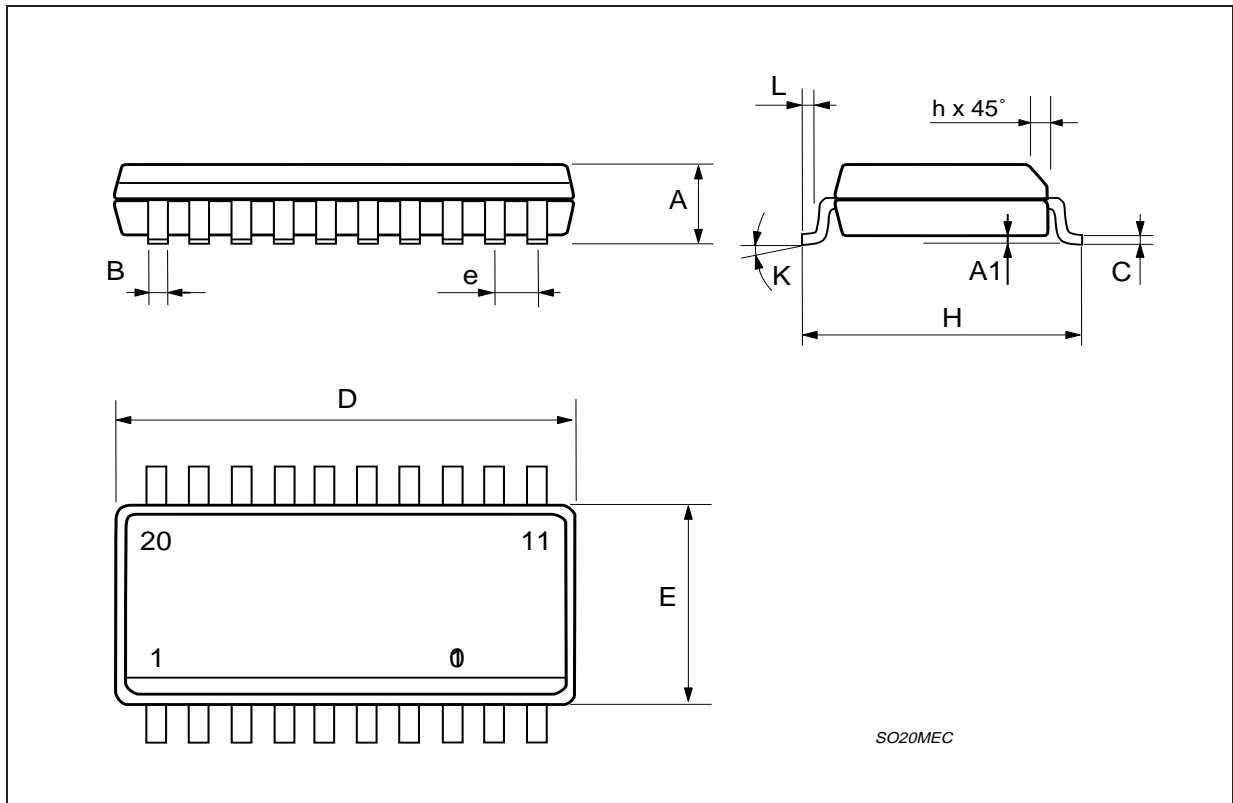


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0° (min.)8° (max.)					

**OUTLINE AND MECHANICAL DATA**



**SO20**



SO20MEC

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.  
All other names are the property of their respective owners

© 2003 STMicroelectronics - All rights reserved

**STMicroelectronics GROUP OF COMPANIES**

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -  
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States  
**www.st.com**

