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1 Block diagram and pin descriptions

Figure 1. Block diagram

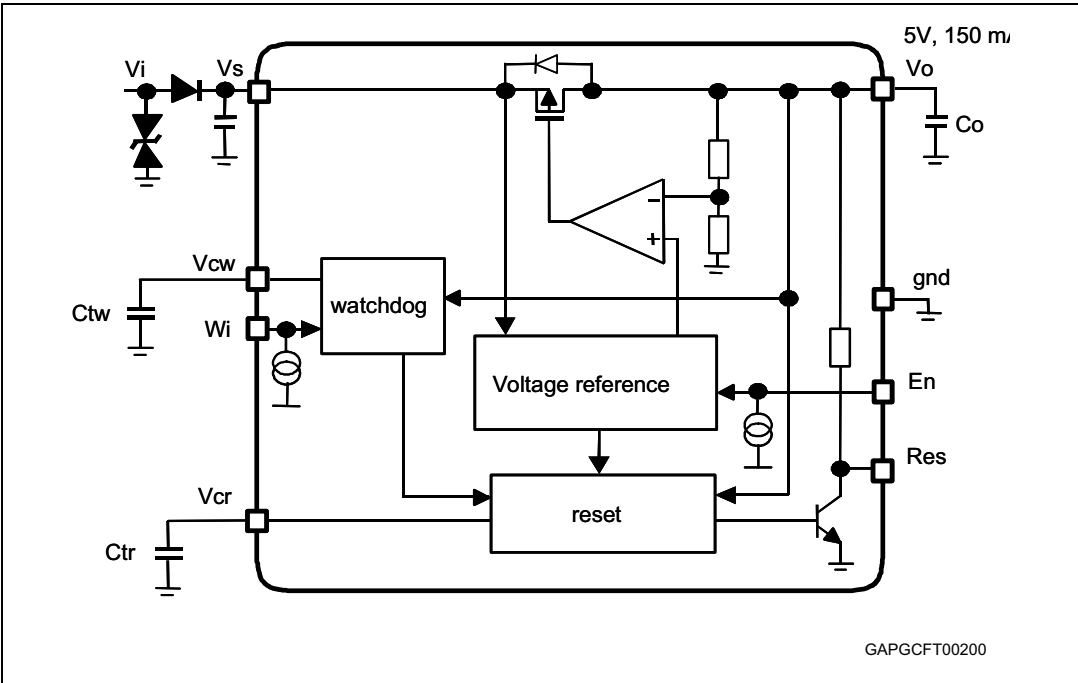


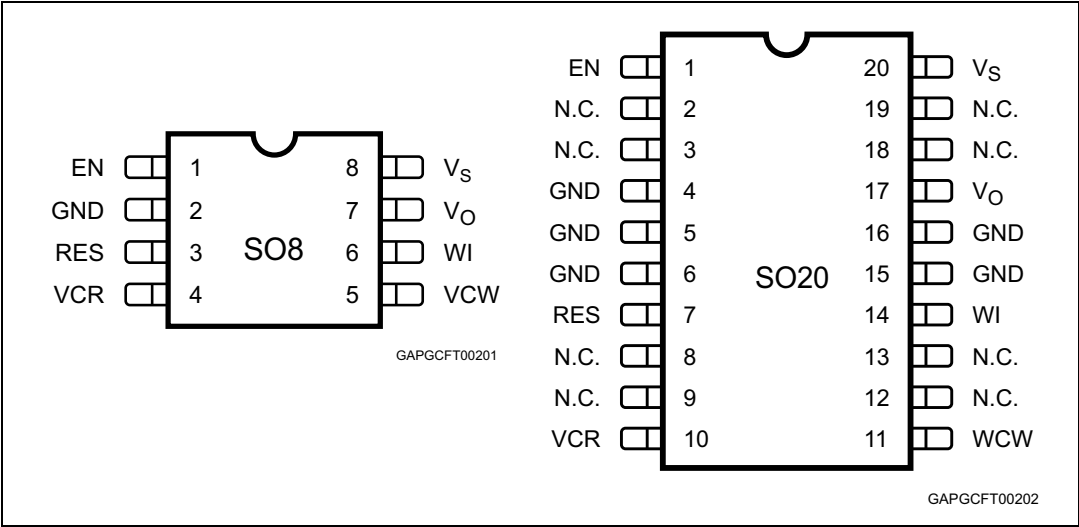
Table 2. Pin function

SO8 pin number	SO20 pin number	Pin name	Function
1	1	En	Enable input. If high, regulator, watchdog and reset are operating. If low, regulator, watchdog and reset are shut down.
2	4	gnd	Ground reference
	5,6,15,16	gnd	Ground. These pins are to be connected to a heat spreader electrically grounded
3	7	Res	Reset output. It is pulled down when output voltage drops below $V_{O_{th}}$ or frequency at W_i is too low.
4	10	Vcr	Reset timing adjust. A capacitor between Vcr pin and gnd sets the reset delay time (t_{rd}).
5	11	Vcw	Watchdog timer adjust. A capacitor between Vcw pin and gnd sets the time response of the watchdog monitor.
6	14	Wi	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.
7	17	Vo	Voltage regulator output. Output capacitor >100 nF is needed for regulator stability.

Table 2. Pin function (continued)

SO8 pin number	SO20 pin number	Pin name	Function
8	20	Vs	Supply voltage Supply capacitor (e.g. 200 nF) is needed for regulator stability.
	2, 3, 8, 9, 12, 13, 18, 19	N. C.	Not connected

Figure 2. Pins connection (top view)



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{VSDC}	DC supply voltage	-0.3 to 40	V
I_{VSDC}	Input current	Internally limited	
V_{VO}	DC output voltage	-0.3 to 6 ⁽¹⁾	V
I_{VO}	DC output current	Internally limited	
V_{WI}	Watchdog input voltage	-0.3 to $V_{\text{VO}} + 0.3$	V
V_{OD}	Open drain output voltage (RES)	-0.3 to $V_{\text{VO}} + 0.3$	V
I_{OD}	Open drain output current (RES)	Internally limited	
V_{CR}	Reset delay voltage	-0.3 to $V_{\text{VO}} + 0.3$	V
V_{CW}	Watchdog delay voltage	-0.3 to $V_{\text{VO}} + 0.3$	V
V_{EN}	Enable input voltage	-0.3 to 40	V
T_{J}	Junction temperature	-40 to 150	°C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	±2	kV

1. Using the typical application schematic with $C_{\text{out}} = 10 \mu\text{F}$ and $I_{\text{out}} = 0 \text{ A}$, when the regulator is switched-on, an overshoot exceeding 6 V could occur. This behavior does not impact the reliability of the regulator.

Table 4. Thermal data

Symbol	Parameter	SO8	SO16+2+2	Unit
$R_{\text{th j-amb}}$	Thermal resistance junction to ambient	130 to 180	50 to 80	°C/W

2.2 Electrical characteristics

$V_s = 5.6 \text{ V}$ to 31 V ; $T_j = -40 \text{ }^\circ\text{C}$ to $150 \text{ }^\circ\text{C}$, unless otherwise specified.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_s, V_o	I_q	Quiescent current	$V_s = 13.5 \text{ V}$, $I_o = 150 \text{ mA}$, enable high all I/O currents = 0		1.5	3	mA
V_s, V_o	I_q	Quiescent current	$V_s = 13.5 \text{ V}$, $I_o = 0 \text{ mA}$, enable high all I/O currents = 0		100	200	μA
V_s, V_o	I_q	Quiescent current	$V_s = 13.5 \text{ V}$, $I_o = 0 \text{ mA}$, enable low all I/O currents = 0		6	20	μA
	T_w	Thermal protection temperature		150		190	$^\circ\text{C}$
	T_{w_hy}	Thermal protection temperature hysteresis			10		$^\circ\text{C}$

Table 6. Voltage regulator

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_o	V_{o_ref}	Output voltage	$V_s = 5.6$ to 31 V ; $I_o = 1$ to 150 mA	4.90	5.00	5.10	V
V_o	I_{short}	Output short circuit current ⁽¹⁾	$V_s = 13.5 \text{ V}$	150	280	400	mA
V_o	I_{lim}	Output current limitation ⁽¹⁾	$V_s = 13.5 \text{ V}$	150	320	500	mA
V_s, V_o	V_{line}	Line regulation voltage	$V_s = 5.6$ to 31 V $I_o = 1$ to 150 mA			25	mV
V_o	V_{load}	Load regulation voltage	$I_o = 1$ to 150 mA			25	mV
V_s, V_o	V_{dp}	Drop voltage	$I_o = 150 \text{ mA}$		200	400	mV
V_s, V_o	SVR	Ripple rejection ⁽²⁾	$f_r = 100 \text{ Hz}$	55			dB

1. See [Figure 3: Behavior of output current versus regulated voltage \$V_o\$](#) .

2. Guaranteed by design.

Table 7. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{es}	V_{res_l}	Reset output low voltage	$R_{ext} = 5 \text{ k}\Omega$ to V_o ; $V_o > 1 \text{ V}$			0.4	V
R_{es}	I_{res_h}	Reset output high leakage current	$V_{res} = 5 \text{ V}$			1	μA

Table 7. Reset (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R _{es}	R _{p_u}	Internal pull-up resistance	With respect to V _o	12	25	50	kΩ
R _{es}	V _{o_th}	Reset threshold voltage	V _s = 5.6 to 31 V I _o = 1 to 150 mA	6% below V _{o_ref}	8% below V _{o_ref}	10% below V _{o_ref}	
V _{cr}	V _{rhth}	Reset timing high threshold	V _s = 13.5 V	44% V _{o_ref}	47% V _{o_ref}	50% V _{o_ref}	
V _{cr}	V _{rlth}	Reset timing low threshold	V _s = 13.5 V	10% V _{o_ref}	13% V _{o_ref}	16% V _{o_ref}	
V _{cr}	I _{cr}	Charge current	V _s = 13.5 V	8	17	30	μA
V _{cr}	I _{dr}	Discharge current	V _s = 13.5 V	8	17	30	μA
R _{es}	t _{rr_2}	Reset delay time ⁽¹⁾	V _o = V _{o_th} - 100 mV	100	250	700	μs
R _{es}	t _{rd}	Reset pulse delay	V _s = 13.5 V; C _{tr} = 1 nF	65		150	ms

1. When V_o becomes lower than 4 V, the reset reaction time decreases down to 2 μs assuring a faster reset condition in this particular case.

Table 8. Watchdog

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
W _i	V _{ih}	Input high voltage	V _s = 13.5 V	3.5			V
W _i	V _{il}	Input low voltage	V _s = 13.5 V			1.5	V
W _i	V _{ih}	Input hysteresis	V _s = 13.5 V		300		mV
W _i	I _i	Pull down current	V _s = 13.5 V		10	20	μA
V _{cw}	V _{whth}	High threshold	V _s = 13.5 V	2.20	2.35	2.50	V
V _{cw}	V _{wlth}	Low threshold	V _s = 13.5 V	0.50	0.65	0.80	V
V _{cw}	I _{cwc}	Charge current	V _s = 13.5 V; V _{cw} = 0.1 V	4	7.5	14	μA
V _{cw}	I _{cwd}	Discharge current	V _s = 13.5 V; V _{cw} = 2.5 V	1.0	2.4	4.5	μA
V _{cw}	T _{wop}	Watchdog period	V _s = 13.5 V; C _{tw} = 47 nF	25	50	90	ms
R _{es}	t _{wol}	Watchdog output low time	V _s = 13.5 V; C _{tw} = 47 nF	6	10	22	ms

Table 9. Enable

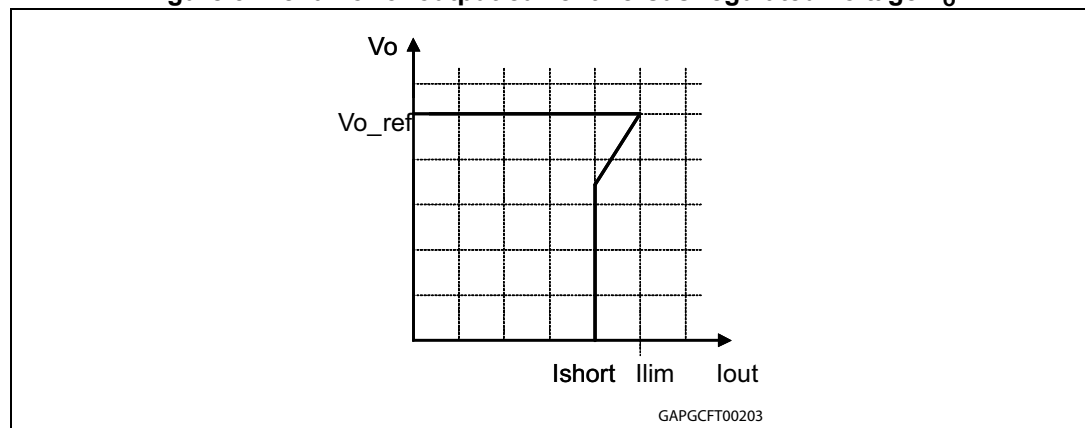
Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E _n	V _{en_l}	Enable input low voltage				1	V
E _n	V _{en_h}	Enable input high voltage		3			V
E _n	V _{en_hy}	Enable input hysteresis		700	1000	1100	mV
E _n	I _{leak}	Pull down current	E _n = 5 V	2	10	20	μA

3 Application information

3.1 Voltage regulator

The voltage regulator uses a p-channel MOS transistor as a regulating element. With this structure a low dropout voltage at current up to 150 mA is achieved. The output voltage is regulated up to transient input supply voltage of 40 V. No functional interruption due to over-voltage pulses is generated. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. A short circuit protection to GND is provided.

Figure 3. Behavior of output current versus regulated voltage V_o



3.2 Reset

The reset circuit monitors the output voltage V_o . If the output voltage drops below V_{o_th} then R_{es} becomes low with a delay time t_{rr} . Real t_{rr} value changes as a non-linear function of delta ($V_{o_th} - V_o$). The reset low signal is guaranteed for an output voltage V_o greater than 1 V.

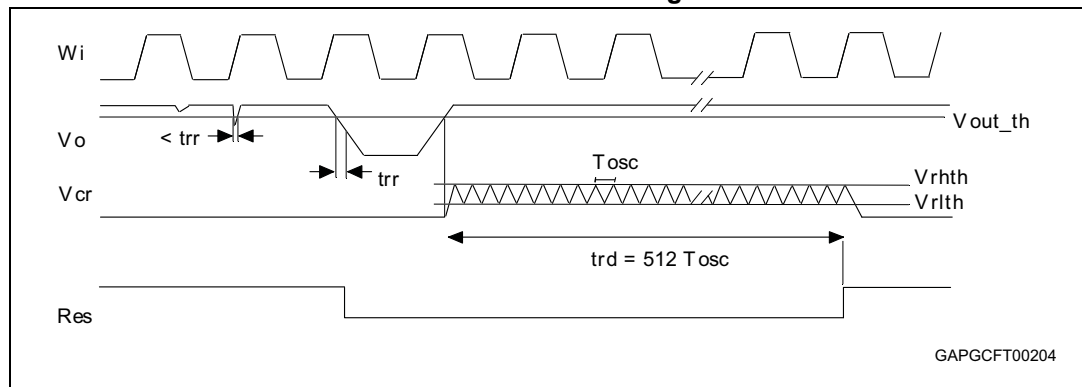
When the output voltage becomes higher than V_{o_th} then R_{es} goes high with a delay t_{rd} . This delay is obtained by 512 periods of an oscillator (see fig. 5). The oscillator period is given by:

$$T_{OSC} = \frac{[(V_{rth} - V_{rlth}) \cdot C_{tr}]}{I_{cr}} + \frac{[(V_{rth} - V_{rlth}) \cdot C_{tr}]}{I_{dr}}$$

and reset pulse delay t_{rd} is given by:

$$t_{rd} = 512 \times T_{OSC}$$

Table 10. Reset time diagram



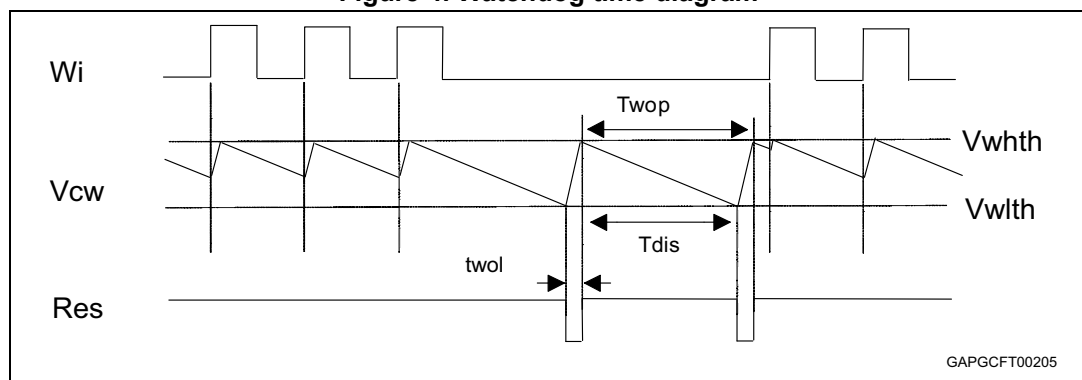
3.3 Watchdog

The watchdog input W_i monitors a connected microcontroller. If pulses are missing, the reset output R_{es} is set to low. The pulse sequence time can be set within a wide range through the external capacitor C_{tw} . The watchdog circuit discharges the capacitor C_{tw} with the constant current I_{cwd} . If the lower threshold V_{wlth} is reached, a watchdog reset is generated. To prevent this reset, the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{wlth} . In order to calculate the minimum time T_{dis} during which the microcontroller must generate the positive edge, the following equation can be used:

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cwd} \times T_{dis}$$

Each W_i positive edge switches the current source from discharging to charging; the same happens when the lower V_{wlth} threshold is reached. When the voltage reaches the upper threshold V_{whth} the current switches from charging to discharging. The result is a saw tooth voltage at the watchdog timer capacitor C_{tw} .

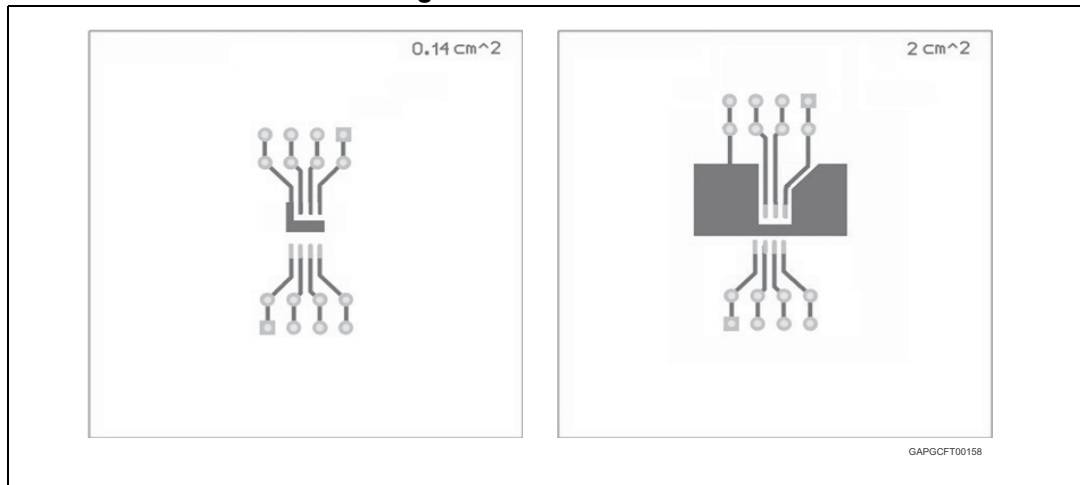
Figure 4. Watchdog time diagram



4 Package and PCB thermal data

4.1 SO-8 thermal data

Figure 5. SO-8 PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB: FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 mm, Copper areas: from minimum pad lay-out to 2cm²).

Figure 6. $R_{thj-amb}$ vs PCB copper area in open box free air condition

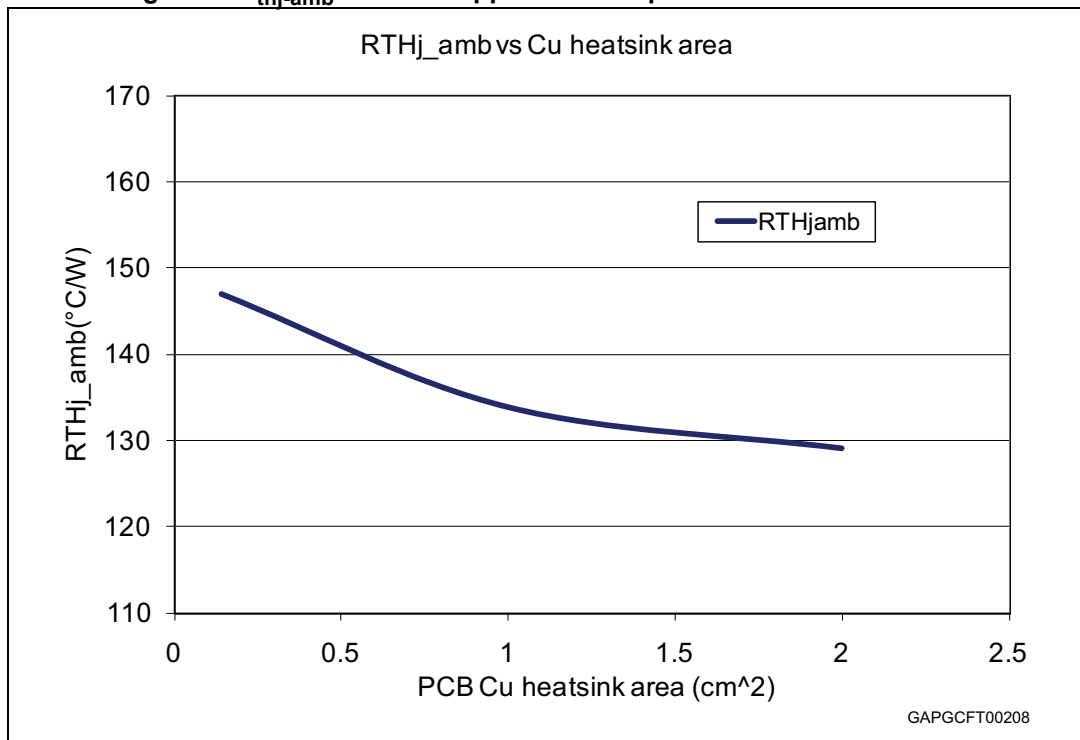
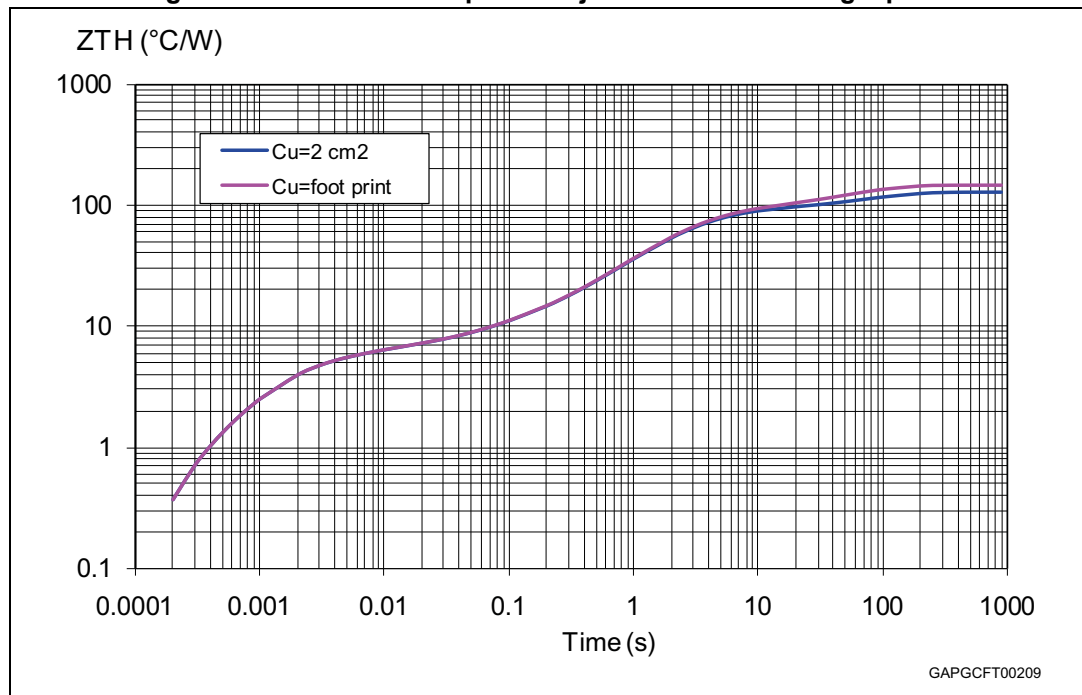


Figure 7. SO-8 thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

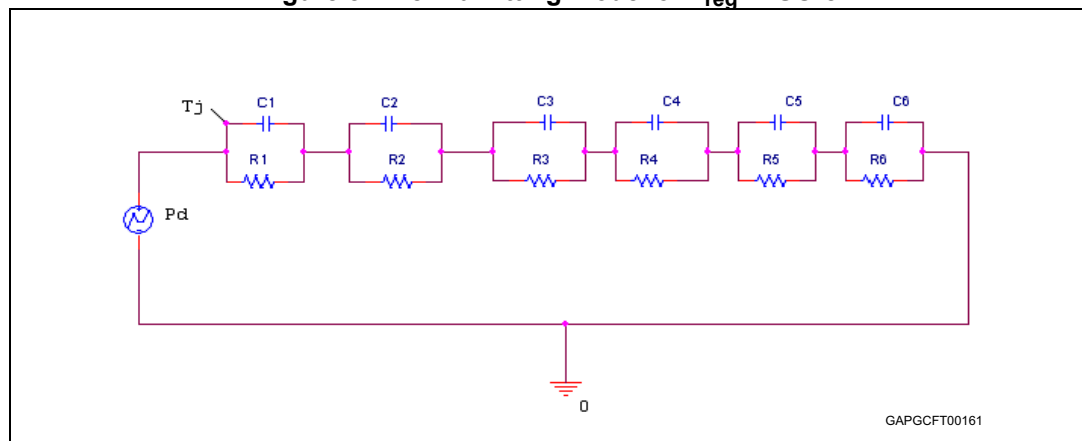
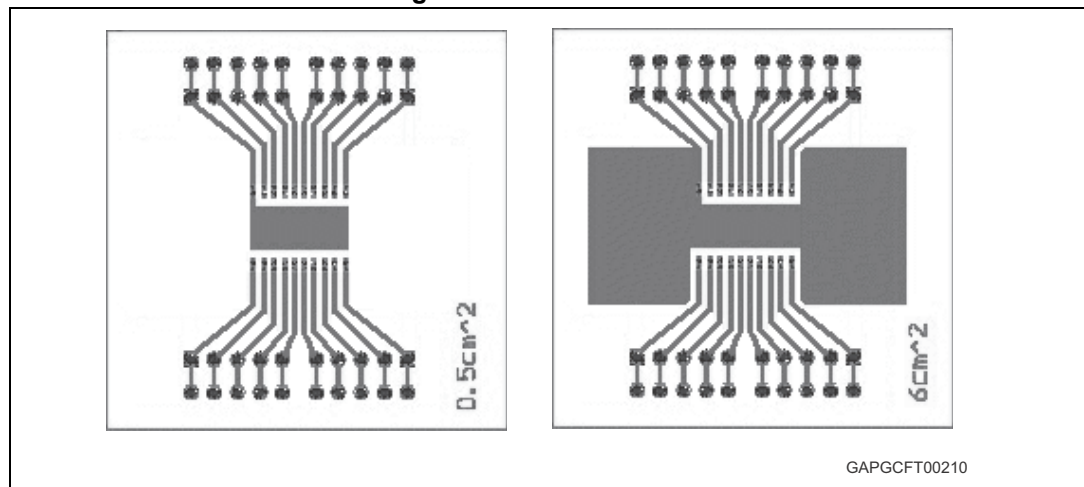
where $\delta = t_p/T$ Figure 8. Thermal fitting model of V_{reg} in SO-8

Table 11. SO-8 thermal parameter

Area (cm ²)	Footprint	2
R1 (°C/W)	4	
R2 (°C/W)	2	
R3 (°C/W)	2	
R4 (°C/W)	41	
R5 (°C/W)	40	
R6 (°C/W)	58	40
C1 (W.s/°C)	0.0003	
C2 (W.s/°C)	0.0025	
C3 (W.s/°C)	0.03	
C4 (W.s/°C)	0.04	
C5 (W.s/°C)	0.1	
C6 (W.s/°C)	1.05	2

4.2 SO-20 thermal data

Figure 9. SO-20 PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB: FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 mm, Copper areas: from minimum pad lay-out to 6cm²).

Figure 10. $R_{thj-amb}$ vs PCB copper area in open box free air condition

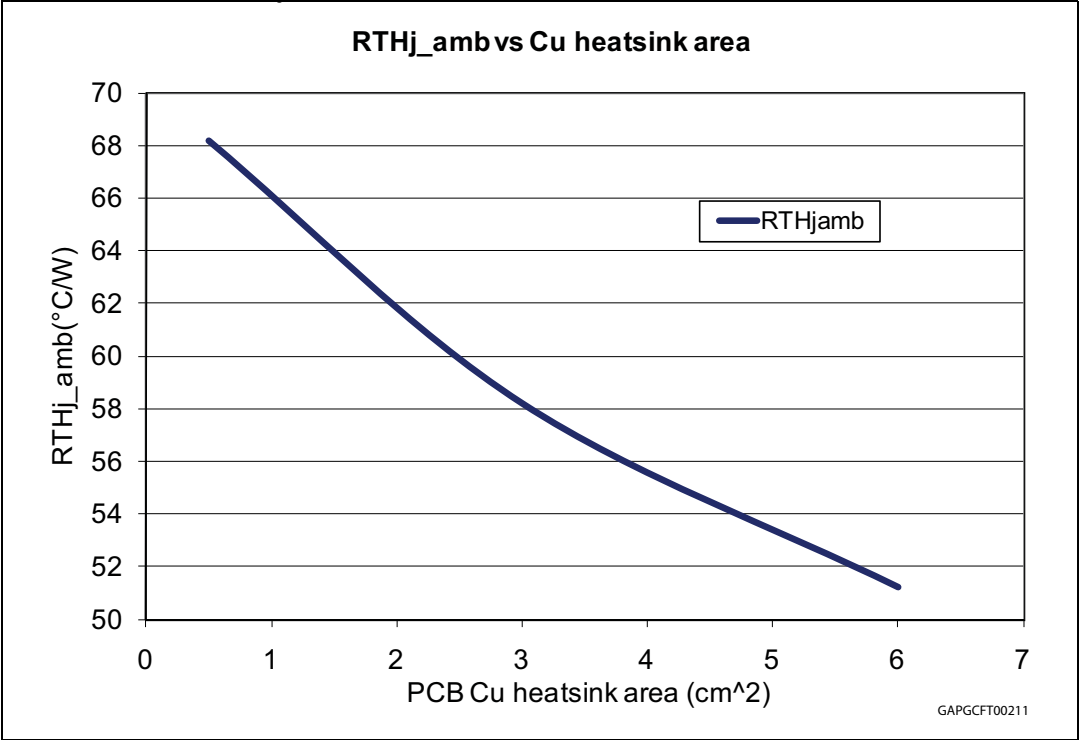
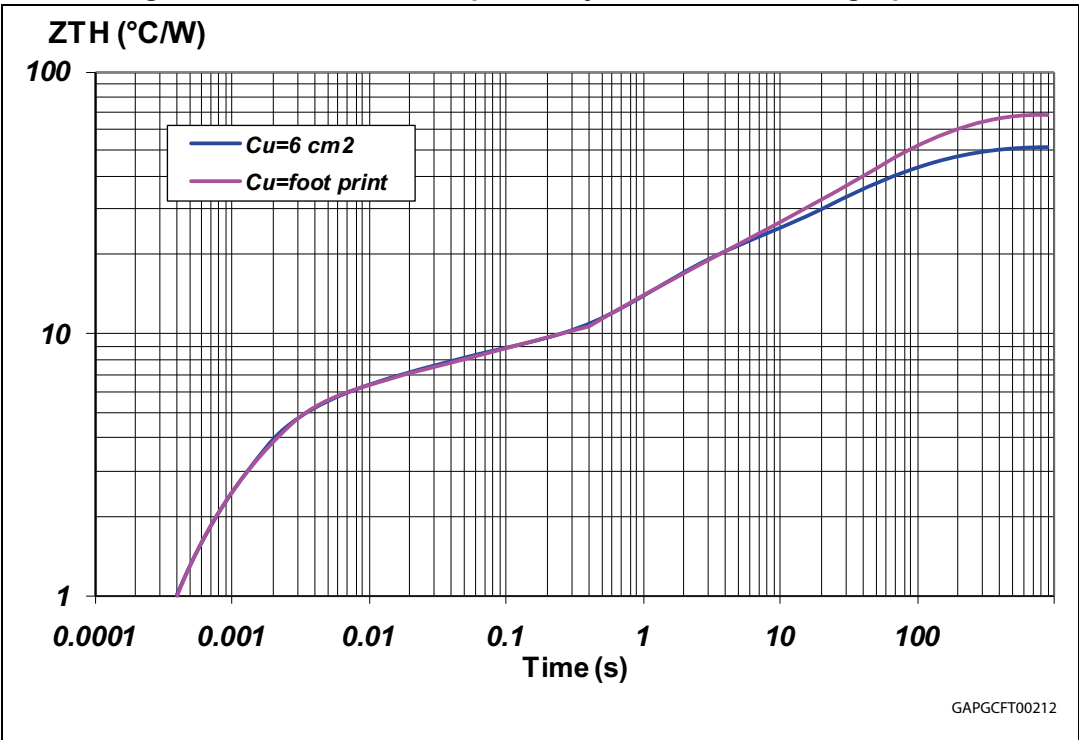


Figure 11. SO-20 thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 12. Thermal fitting model of V_{reg} in SO-20

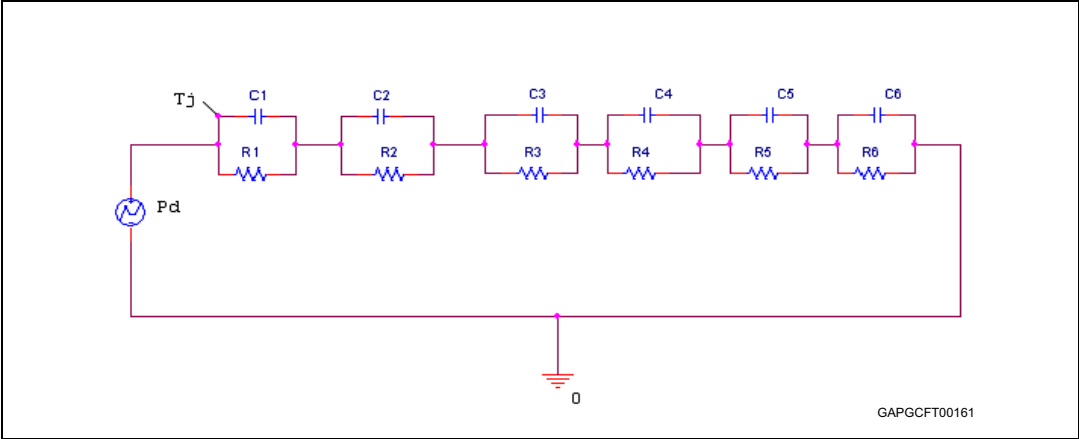


Table 12. SO-20 thermal parameter

Area (cm ²)	Footprint	2
R1 (°C/W)	4	
R2 (°C/W)	2	
R3 (°C/W)	2.2	
R4 (°C/W)	10	
R5 (°C/W)	15	
R6 (°C/W)	35	18
C1 (W.s/°C)	0.0003	
C2 (W.s/°C)	0.0025	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.15	
C5 (W.s/°C)	1.5	
C6 (W.s/°C)	4	7

5 Package information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 SO-8 package information

Figure 13. SO-8 package dimensions

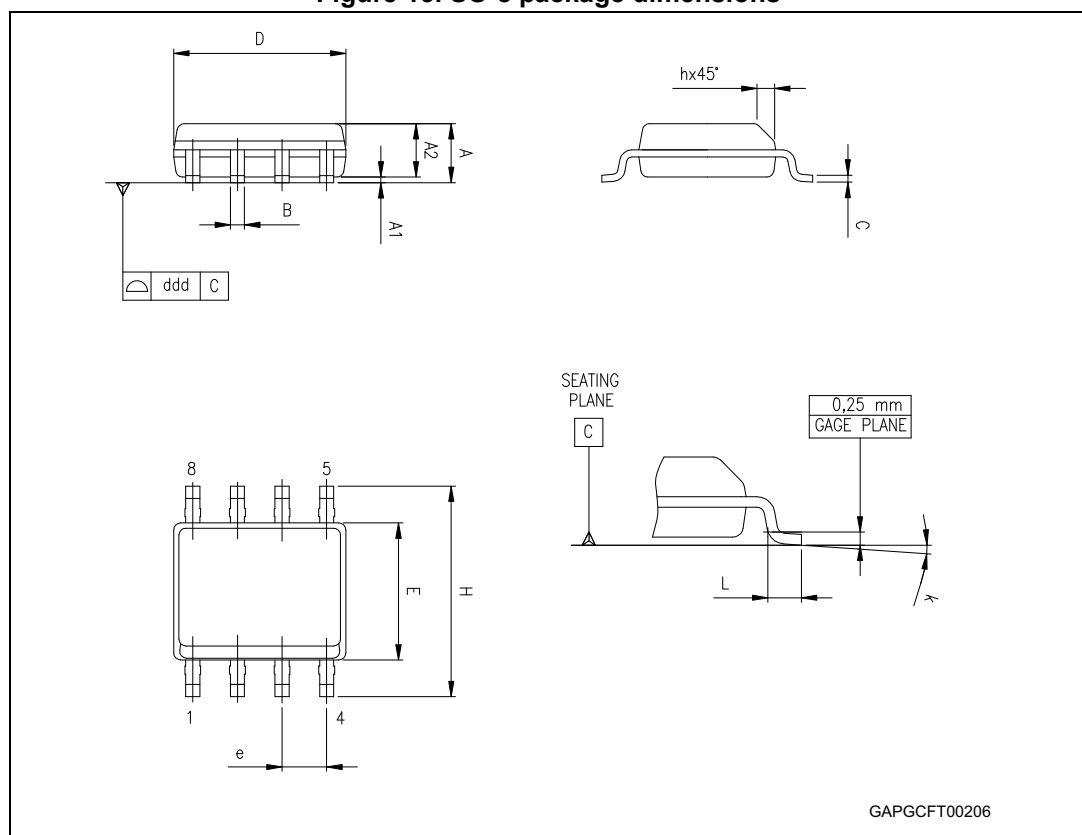


Table 13. SO-8 mechanical data

Symbol	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D ⁽¹⁾	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 inch) in total (both side).

5.3 SO-20 package information

Figure 14. SO-20 package dimensions

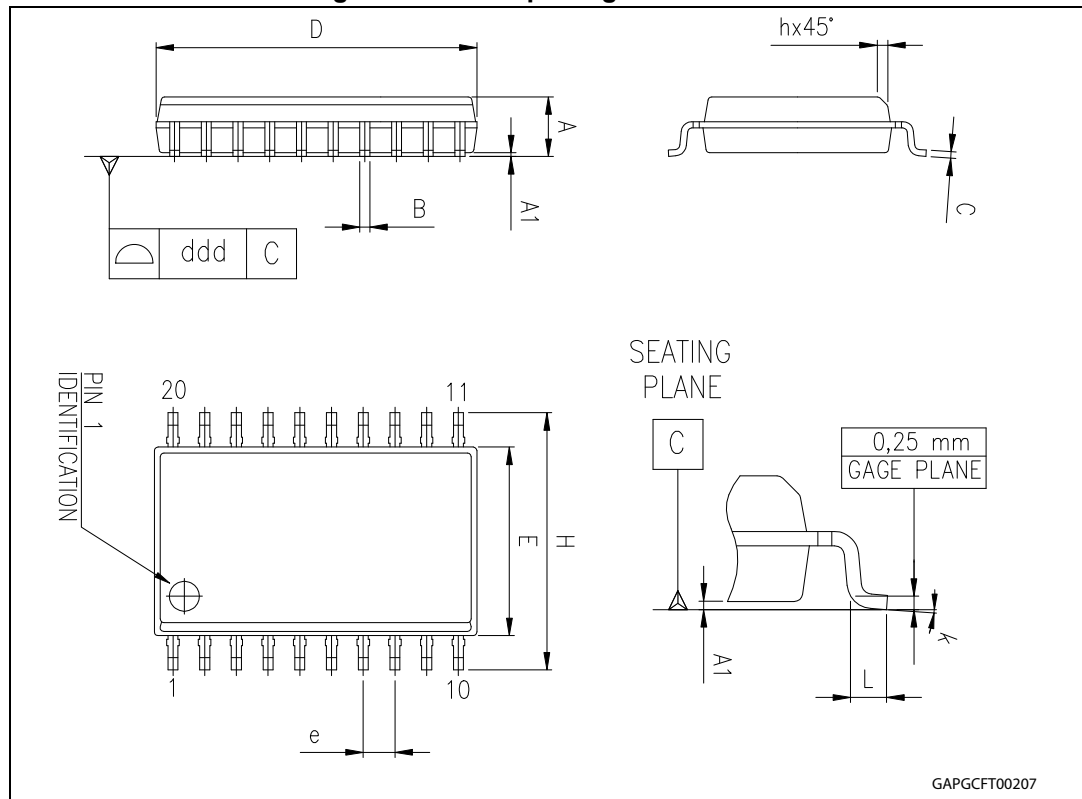


Table 14. SO-20 mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D ⁽¹⁾	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. "D" dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

6 Revision history

Table 15. Document revision history

Date	Revision	Changes
01-Jun-2004	3	Changed the values of the parameter "Reset timing high/low threshold.
01-Jul-2004	4	Pin Connection SO-20 changed. Changed some textes in the Features and table 2. Changed some values in the tables 3, 4 and 5. Changed some textes in the sections 2, 3 and 4.
01-Oct-2004	5	Changed from Product Preview to final datasheet.
01-Feb-2006	6	Modified the orderable part numbers for Tape & Reel.
04-Apr-2011	7	Changed document template. Added Chapter 4: Package and PCB thermal data
27-Mar-2012	8	Update Table 3: Absolute maximum ratings
19-Sep-2013	9	Updated Disclaimer.
23-Feb-2018	10	Updated template. Removed the tube version on the SO-8 package on the Table 1: Device summary . Updated Section 2.1: Absolute maximum ratings
20-Sep-2018	11	Added the feature "AEC-Q100 qualified" in cover page with the logo automotive.

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