

**ELECTRICAL CHARACTERISTICS** (Tj= 25°C unless otherwise noticed)

**L30ESD5V0C3-2**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse standoff voltage	V <sub>DRM</sub>	---	---	---	5	V
Reverse leakage current	I <sub>RM</sub>	V <sub>DRM</sub> = 5V	---	---	1	uA
Peak pulse Current	I <sub>pp</sub>	t <sub>p</sub> = 8/20us	---	---	17	A
Breakdown voltage	V <sub>BR</sub>	I <sub>R</sub> = 1 mA	6.4	---	7.2	V
Diode capacitance	C <sub>J</sub>	V <sub>R</sub> = 0 V , f = 1MHz	---	156	160	pF
Clamping Voltage	V <sub>CL</sub>	I <sub>pp</sub> = 1 A, t <sub>p</sub> = 8/20us	---	---	9.8	V
Clamping Voltage	V <sub>CL</sub>	I <sub>pp</sub> = 15 A, t <sub>p</sub> = 8/20us	---	---	20	V

**L30ESD12VC3-2**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse standoff voltage	V <sub>DRM</sub>	---	---	---	12	V
Reverse leakage current	I <sub>RM</sub>	V <sub>DRM</sub> = 12 V	---	---	1	uA
Peak pulse Current	I <sub>pp</sub>	t <sub>p</sub> = 8/20us	---	---	12	A
Breakdown voltage	V <sub>BR</sub>	I <sub>R</sub> = 1 mA	14.2	---	15.8	V
Diode capacitance	C <sub>J</sub>	V <sub>R</sub> = 0 V , f = 1MHz	---	78	100	pF
Clamping Voltage	V <sub>CL</sub>	I <sub>pp</sub> = 1 A, t <sub>p</sub> = 8/20us	---	---	19	V
Clamping Voltage	V <sub>CL</sub>	I <sub>pp</sub> = 12 A, t <sub>p</sub> = 8/20us	---	---	25	V

**L30ESD24VC3-2**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse standoff voltage	V <sub>DRM</sub>	---	---	---	24	V
Reverse leakage current	I <sub>RM</sub>	V <sub>DRM</sub> = 24V	---	---	1	uA
Peak pulse Current	I <sub>pp</sub>	t <sub>p</sub> = 8/20us	---	---	4	A
Breakdown voltage	V <sub>BR</sub>	I <sub>R</sub> = 1 mA	26.7	---	29.6	V
Diode capacitance	C <sub>J</sub>	V <sub>R</sub> = 0 V , f = 1MHz	---	30	60	pF
Clamping Voltage	V <sub>CL</sub>	I <sub>pp</sub> = 1 A, t <sub>p</sub> = 8/20us	---	---	36	V
Clamping Voltage	V <sub>CL</sub>	I <sub>pp</sub> = 4 A, t <sub>p</sub> = 8/20us	---	---	43	V

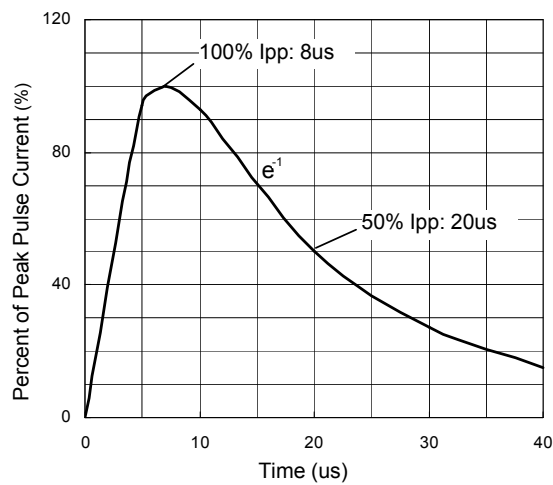


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

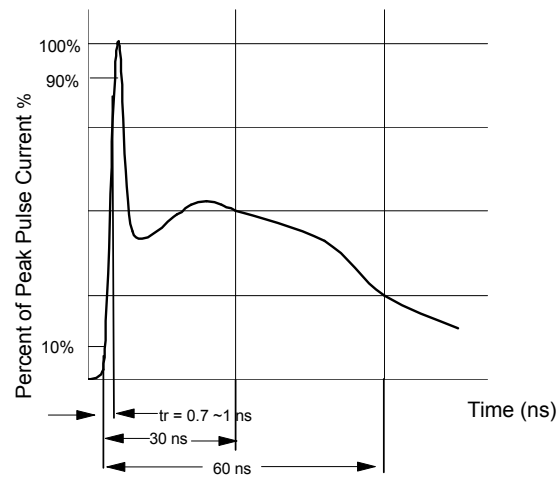


Figure 2. ESD pulse waveform according to IEC 61000-4-2

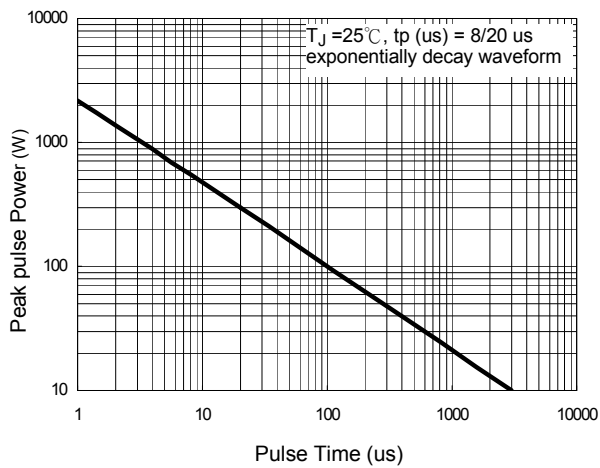


Figure 3. Power Dissipation versus Pulse Time

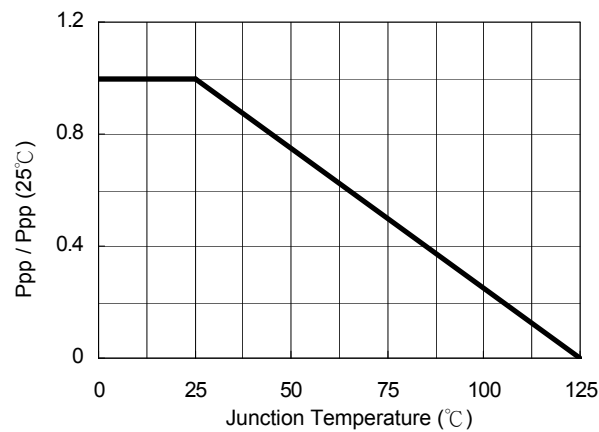


Figure 4. Peak pulse power versus  $T_J$

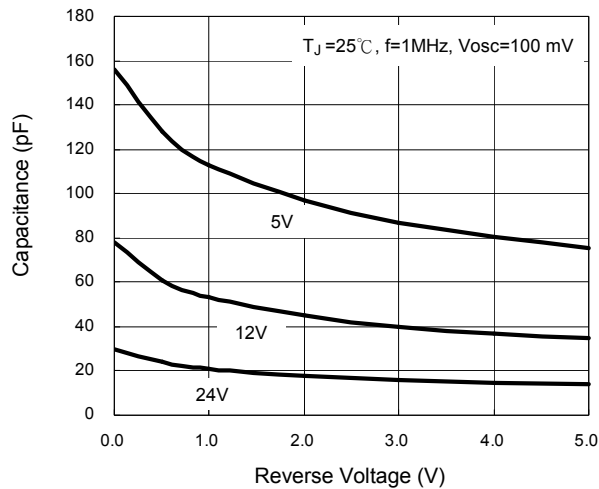


Figure 5. Typical Junction Capacitance

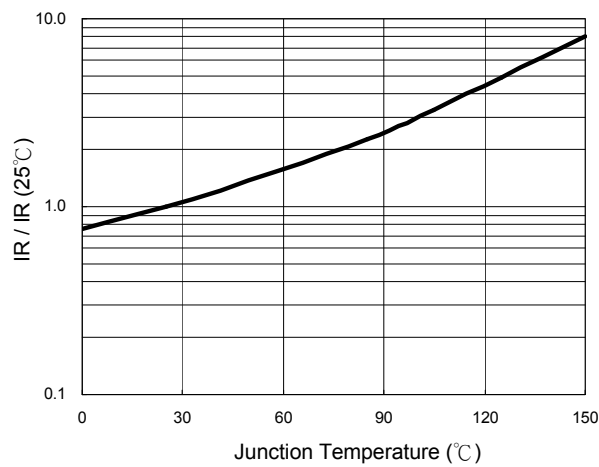


Figure 6. Reverse Leakage Current versus  $T_J$

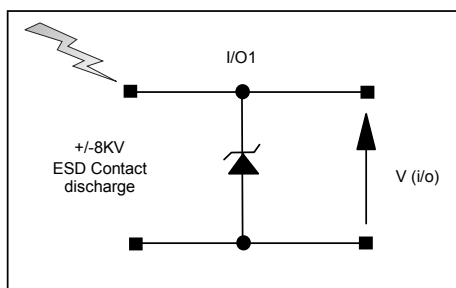


Figure 7. ESD Test Configuration

**L30ESD5V0C3-2**

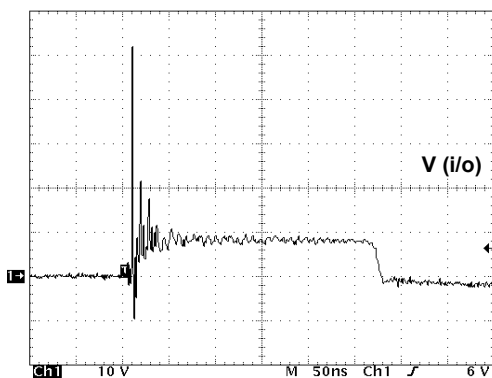


Figure 8. Clamped +8 kV ESD voltage waveform

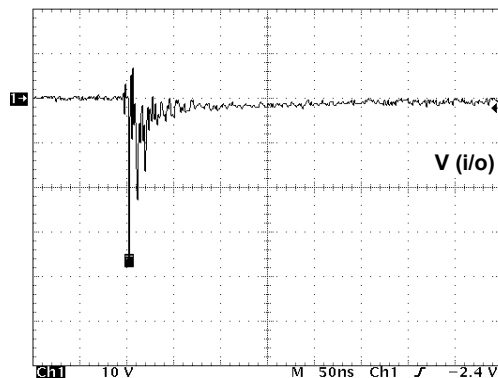


Figure 9. Clamped -8 kV ESD voltage waveform

**L30ESD12VC3-2**

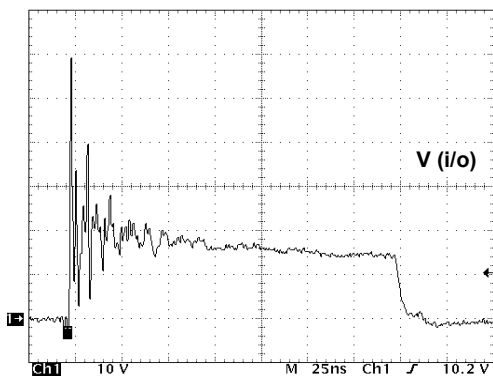


Figure 10. Clamped +8 kV ESD voltage waveform

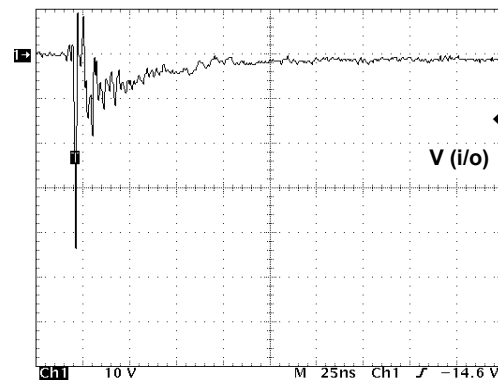


Figure 11. Clamped -8 kV ESD voltage waveform

**L30ESD24VC3-2**

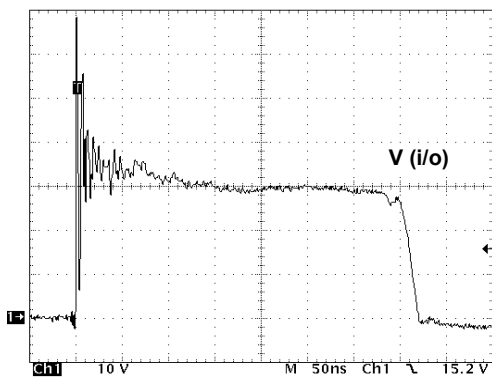


Figure 12. Clamped +8 kV ESD voltage waveform

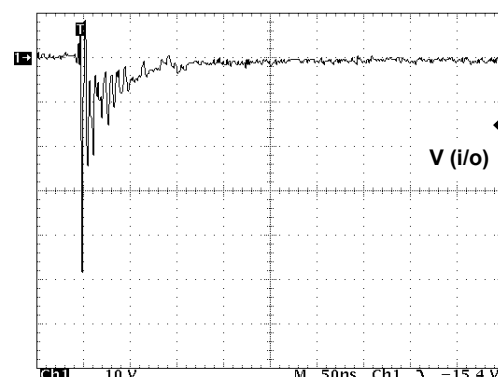


Figure 13. Clamped -8 kV ESD voltage waveform

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