PIN CONFIGURATION
28-Pin SOJ and SOP

|			
A14	1	28	VCC
A12	2	27	$\overline{WE}$
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{OE}$
A2	8	21	A10
A1	9	20	$\overline{CE}$
A0	10	19	I/O7
I/O0	11	18	I/O6
I/O1	12	17	I/O5
I/O2	13	16	I/O4
GND	14	15	I/O3
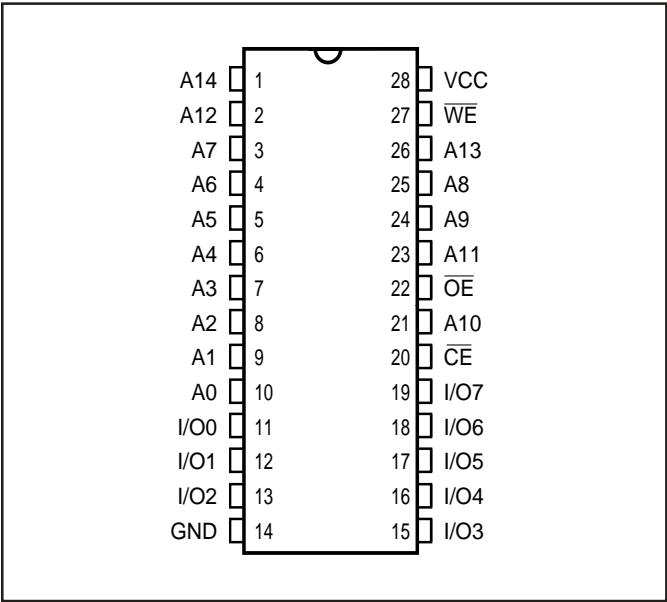
28-Pin TSOP (Type I) (Normal Bent)

$\overline{OE}$	22	21	A10
A11	23	20	$\overline{CE}$
A9	24	19	I/O7
A8	25	18	I/O6
A13	26	17	I/O5
$\overline{WE}$	27	16	I/O4
VCC	28	15	I/O3
A14	1	14	GND
A12	2	13	I/O2
A7	3	12	I/O1
A6	4	11	I/O0
A5	5	10	A0
A4	6	9	A1
A3	7	8	A2

28-Pin TSOP (Type I) (Reverse Bent)

A3	7	8	A2
A4	6	9	A1
A5	5	10	A0
A6	4	11	I/O0
A7	3	12	I/O1
A12	2	13	I/O2
A14	1	14	GND
VCC	28	15	I/O3
WE	27	16	I/O4
A13	26	17	I/O5
A8	25	18	I/O6
A9	24	19	I/O7
A11	23	20	CE
OE	22	21	A10

PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground
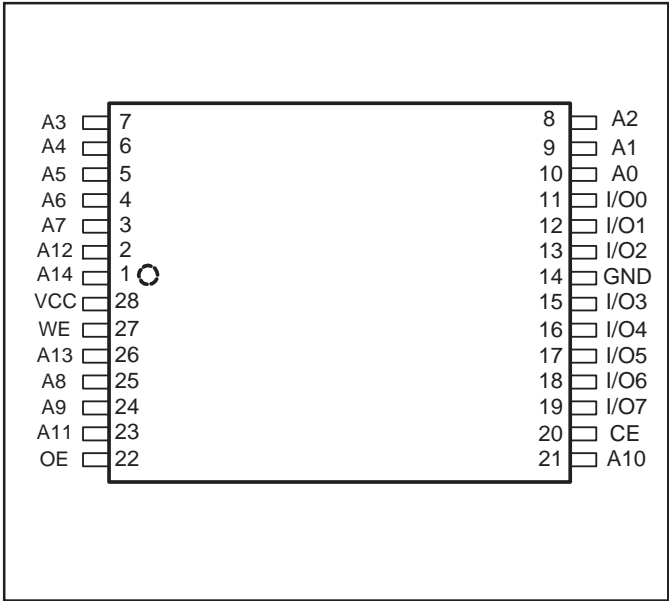
TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V$_{TERM}$	Terminal Voltage with Respect to GND	−0.5 to +4.6	V
T$_{BIAS}$	Temperature Under Bias	−55 to +125	°C
T$_{STG}$	Storage Temperature	−65 to +150	°C
P$_T$	Power Dissipation	0.5	W
I$_{OUT}$	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V$_{CC}$
Commercial	0°C to +70°C	3.3V ± 5%
Industrial	−40°C to +85°C	3.3V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V$_{OH}$	Output HIGH Voltage	V$_{CC}$ = Min., I$_{OH}$ = −1.0 mA		2.4	—	V
V$_{OL}$	Output LOW Voltage	V$_{CC}$ = Min., I$_{OL}$ = 2.1 mA		—	0.4	V
V$_{IH}$	Input HIGH Voltage			2.2	V$_{CC}$ + 0.3	V
V$_{IL}$	Input LOW Voltage[1]			−0.3	0.8	V
I$_{LI}$	Input Leakage	GND ≤ V$_{IN}$ ≤ V$_{CC}$	Com. Ind.	−2 −5	2 5	µA
I$_{LO}$	Output Leakage	GND ≤ V$_{OUT}$ ≤ V$_{CC}$, Outputs Disabled	Com. Ind.	−2 −5	2 5	µA

Notes:
1. V$_{IL}$ = −3.0V for pulse width less than 10 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

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POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-45 ns Min.	-45 ns Max.	-70 ns Min.	-70 ns Max.	Unit
I_{CC1}	Vcc Operating Supply Current	Vcc = Max., $\overline{CE}$ = VIL IOUT = 0 mA, f = 0	Com. Ind.	— —	20 30	— —	20 30	mA
I_{CC2}	Vcc Dynamic Operating Supply Current	Vcc = Max., $\overline{CE}$ = VIL IOUT = 0 mA, f = fMAX	Com. Ind.	— —	35 45	— —	30 40	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	Vcc = Max., VIN = VIH or VIL $\overline{CE}$ ≥ VIH, f = 0	Com. Ind.	— —	2 5	— —	2 5	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	Vcc = Max., $\overline{CE}$ ≥ Vcc – 0.2V, VIN ≥ Vcc – 0.2V, or VIN ≤ 0.2V, f = 0	Com. Ind.	— —	90 200	— —	90 200	μA

Notes:
1. At f = fMAX, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1,2]

| Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	VIN = 0V	6	pF
C_{OUT}	Output Capacitance	VOUT = 0V	5	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: TA = 25°C, f = 1 MHz, Vcc =3.3V.

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AC TEST CONDITIONS

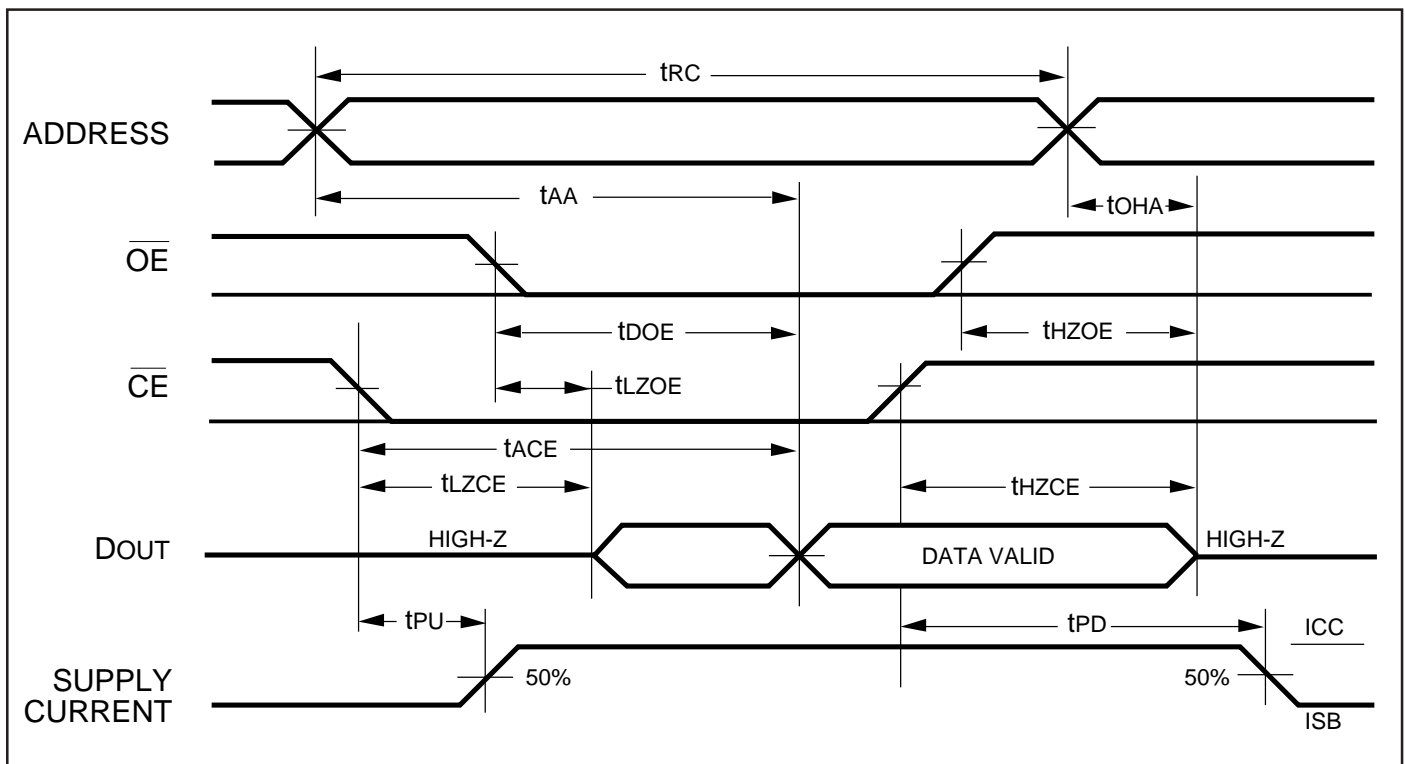| Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1a and 1b
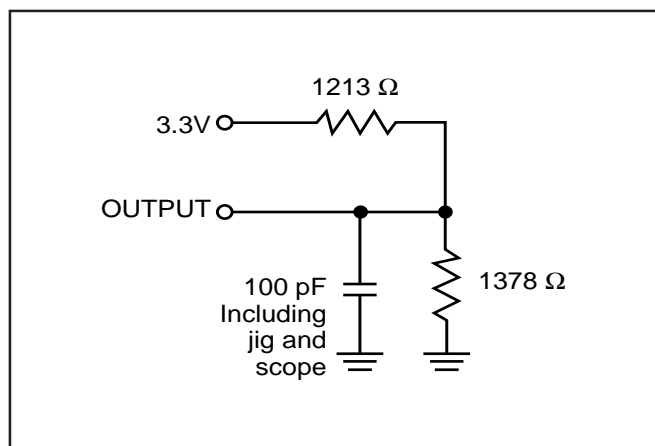
Figures 1a
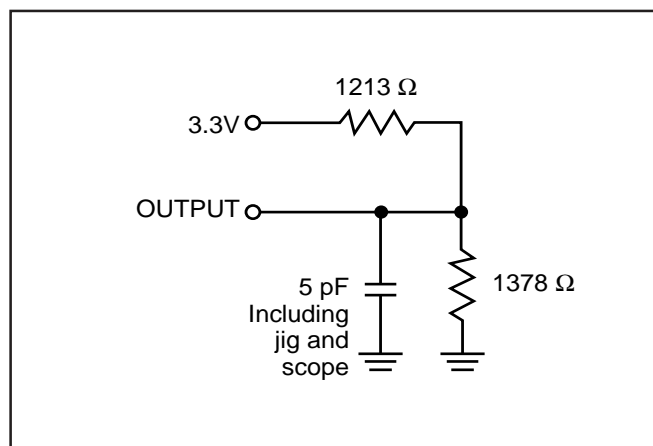
Figures 1b

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-45 ns Min.	-45 ns Max.	-70 ns Min.	-70 ns Max.	Unit
t_{RC}	Read Cycle Time	45	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	70	ns
t_{OHA}	Output Hold Time	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	45	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	20	0	25	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	20	0	25	ns
t_{PU}[3]	$\overline{CE}$ to Power-Up	0	—	0	—	ns
t_{PD}[3]	$\overline{CE}$ to Power-Down	—	30	—	50	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]
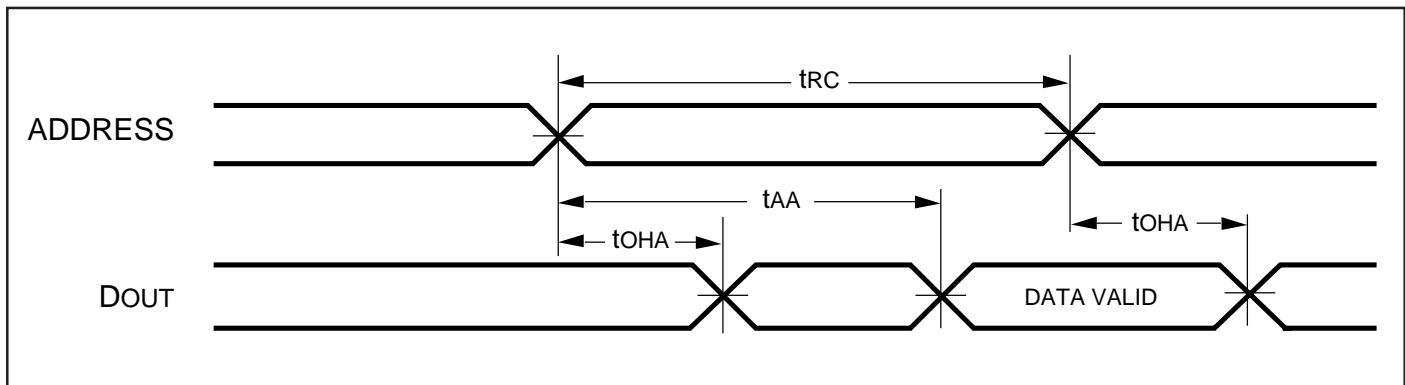
READ CYCLE NO. 2[1,3]

Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V$_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2,3] (Over Operating Range)

Symbol	Parameter	-45 ns Min.	-45 ns Max.	-70 ns Min.	-70 ns Max.	Unit
t_{WC}	Write Cycle Time	45	—	70	—	ns
t_{SCE}	$\overline{CE}$ to Write End	35	—	60	—	ns
t_{AW}	Address Setup Time to Write End	25	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	25	—	55	—	ns
t_{SD}	Data Setup to Write End	20	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with $\overline{OE}$ HIGH.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]
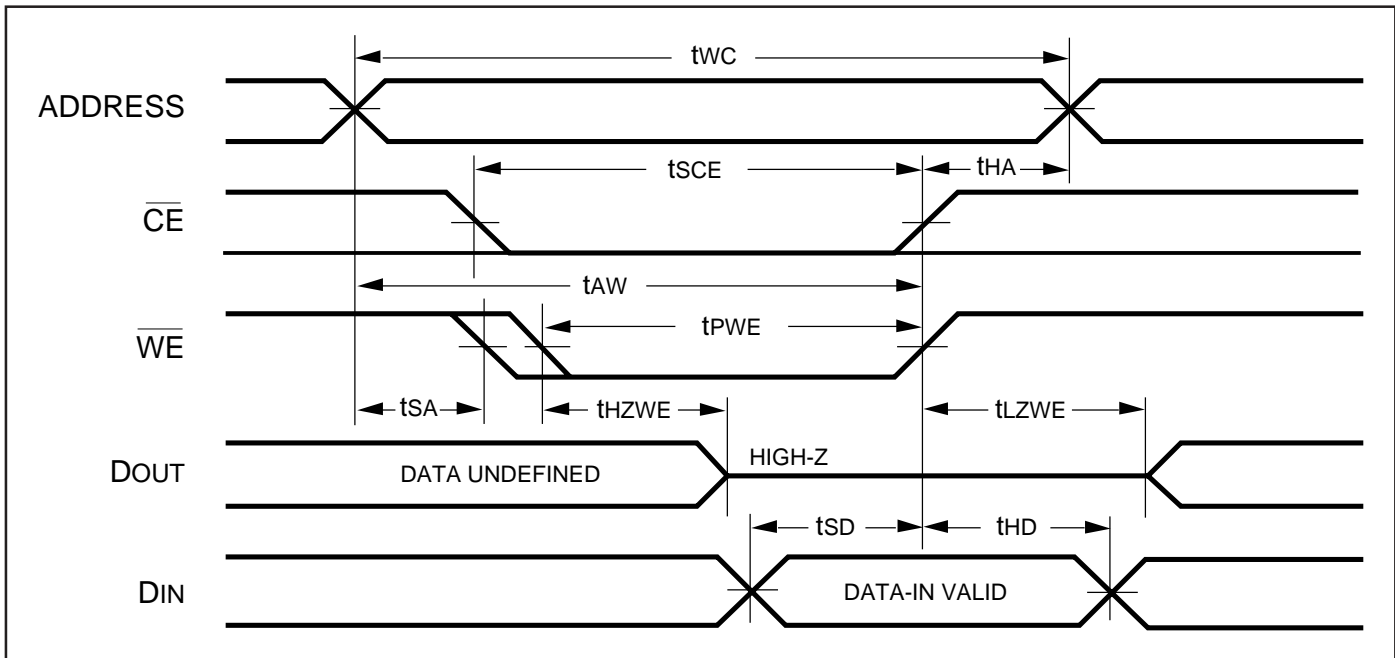
WRITE CYCLE NO. 2 ($\overline{CE}$ Controlled)[1,2]
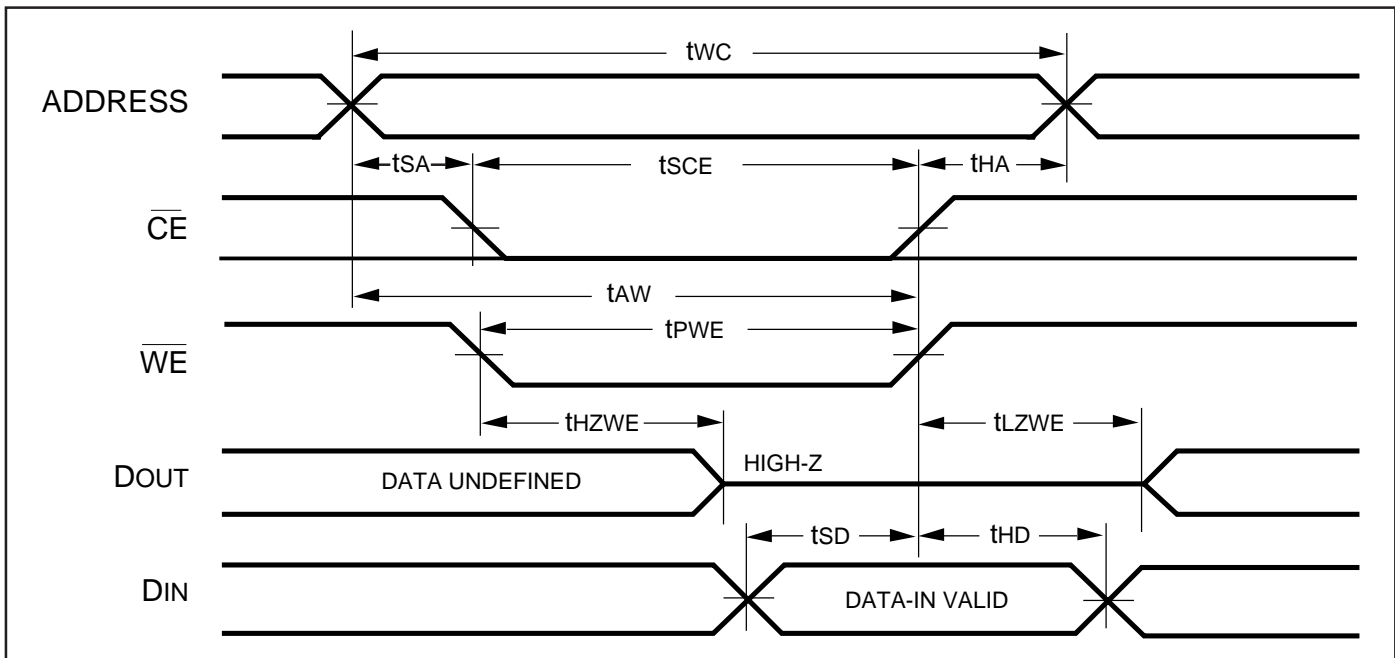
Notes:
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \cdot V_{IH}$.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
45	IS62LV256-45J	300-mil Plastic SOJ
45	IS62LV256-45U	330-mil SOP
45	IS62LV256-45T	TSOP (Type I normal bent)
70	IS62LV256-70U	330-mil SOP
70	IS62LV256-70T	TSOP (Type I normal bent)
70	IS62LV256-70RT	TSOP (Type I reverse Bent)

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62LV256-45JI	300-mil Plastic SOJ
45	IS62LV256-45UI	330-mil SOP
45	IS62LV256-45TI	TSOP (Type I normal bent)
70	IS62LV256-70UI	330-mil SOP
70	IS62LV256-70TI	TSOP (Type I normal bent)
70	IS62LV256-70RTI	TSOP (Type I reverse Bent)