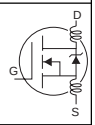
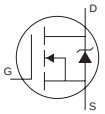
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.185	Ω	V_{GS} = 10V, I_D = 6.0A ④
		—	—	0.225		V_{GS} = 5.0V, I_D = 6.0A ④
		—	—	0.265		V_{GS} = 4.0V, I_D = 5.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	3.1	—	—	S	V_{DS} = 25V, I_D = 6.0A⑥
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -16V
Q_g	Total Gate Charge	—	—	20	nC	I_D = 6.0A
Q_{gs}	Gate-to-Source Charge	—	—	4.6		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	10		V_{GS} = 5.0V, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	4.0	—	ns	V_{DD} = 50V
t_r	Rise Time	—	35	—		I_D = 6.0A
$t_{d(off)}$	Turn-Off Delay Time	—	23	—		R_G = 11Ω, V_{GS} = 5.0V
t_f	Fall Time		22			R_D = 8.2Ω, See Fig. 10 ④⑥
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact⑤
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	440	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	97	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	50	—		f = 1.0MHz, See Fig. 5⑥



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	10	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	35		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 6.0A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	110	160	ns	T_J = 25°C, I_F =6.0A
Q_{rr}	Reverse RecoveryCharge	—	410	620	nC	di/dt = 100A/µs ④⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 4.7mH R_G = 25Ω, I_{AS} = 6.0A. (See Figure 12)

③ I_{SD} ≤ 6.0A, di/dt ≤ 340A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact

⑥ Uses IRL520N data and test conditions.

** When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

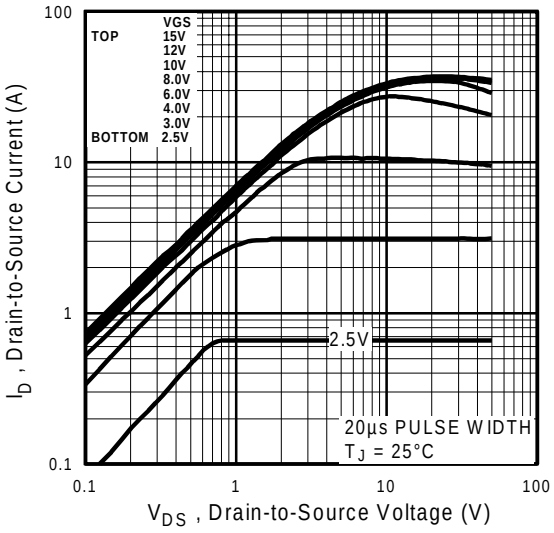


Fig 1. Typical Output Characteristics

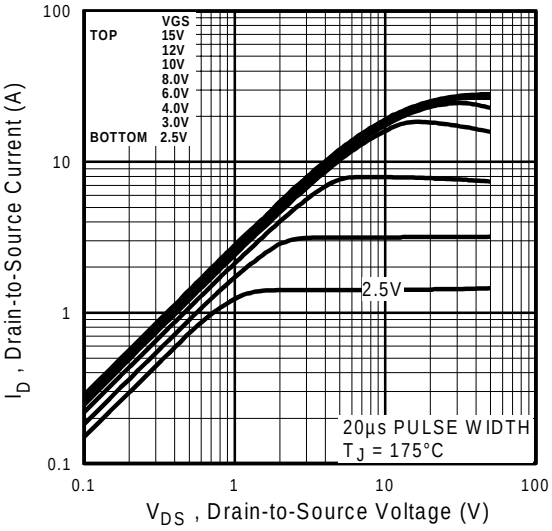


Fig 2. Typical Output Characteristics

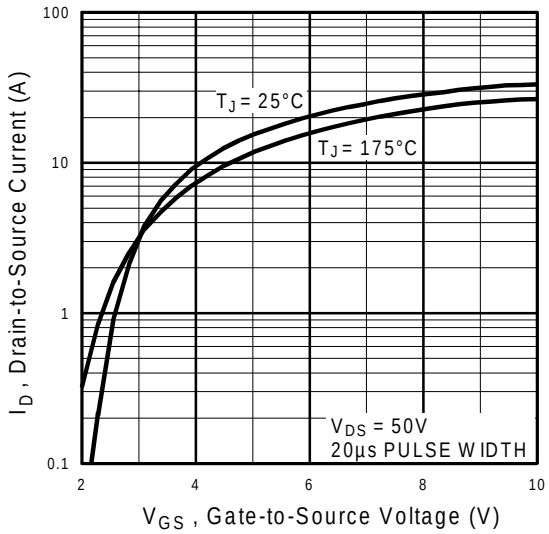


Fig 3. Typical Transfer Characteristics

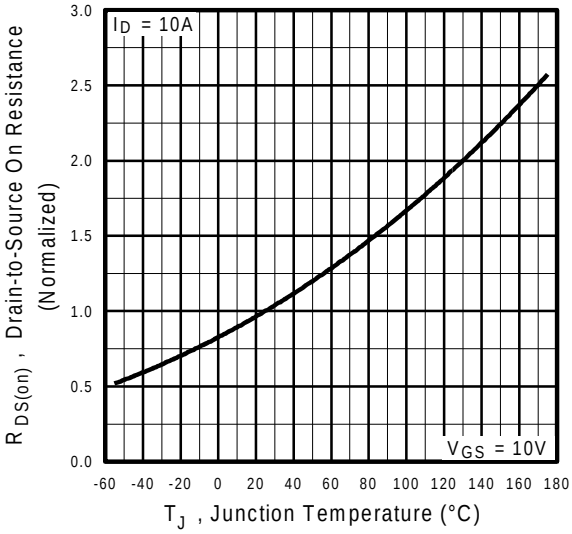


Fig 4. Normalized On-Resistance Vs. Temperature

and

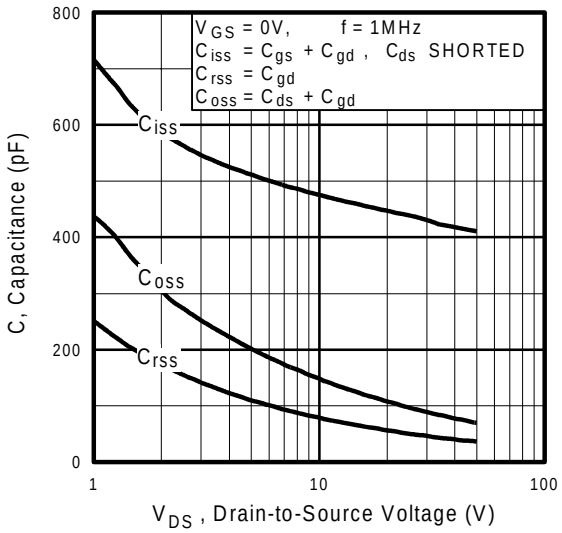


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

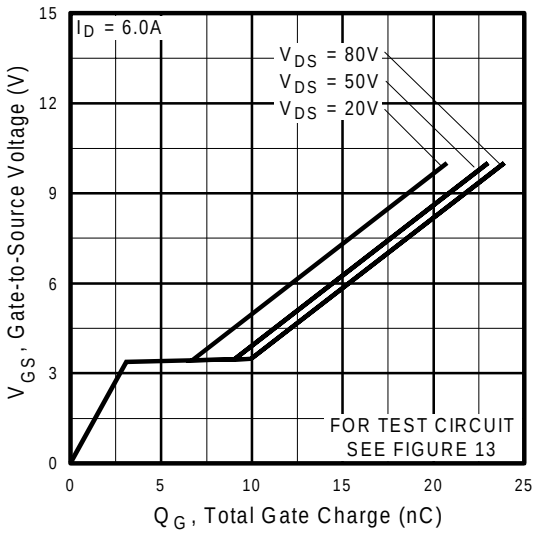


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

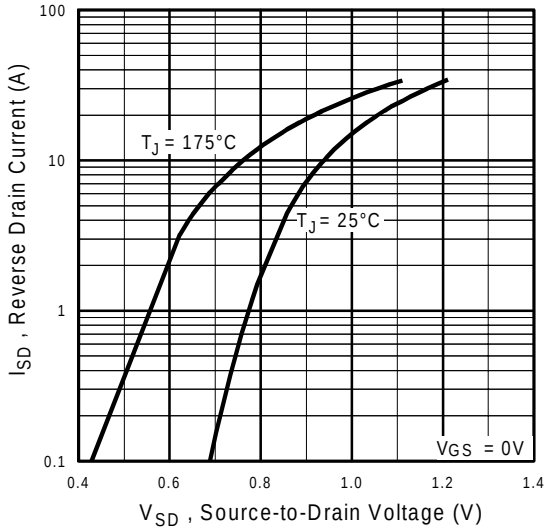


Fig 7. Typical Source-Drain Diode Forward Voltage

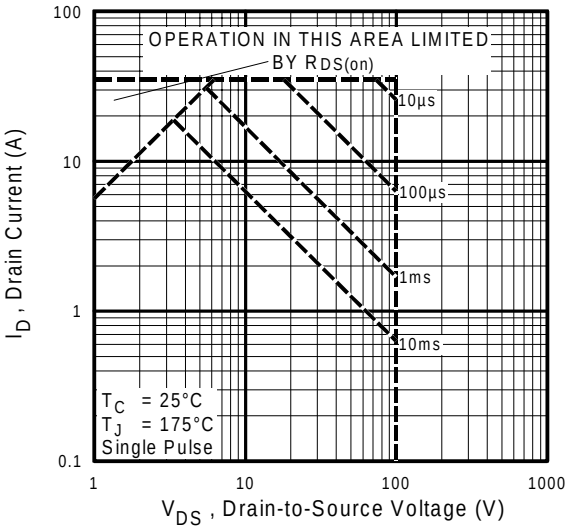


Fig 8. Maximum Safe Operating Area

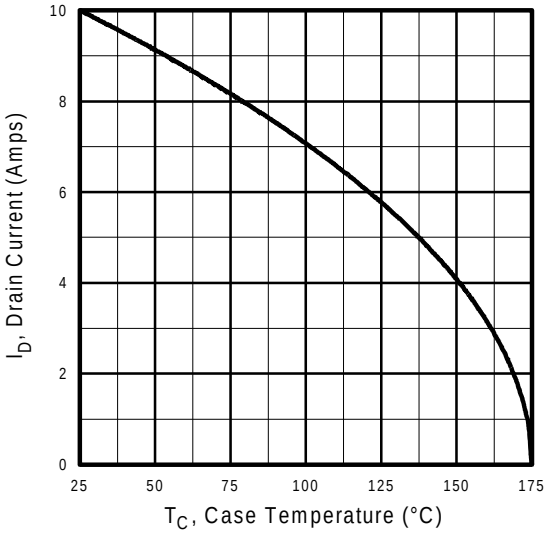


Fig 9. Maximum Drain Current Vs. Case Temperature

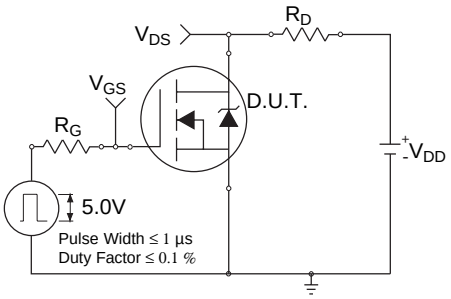


Fig 10a. Switching Time Test Circuit

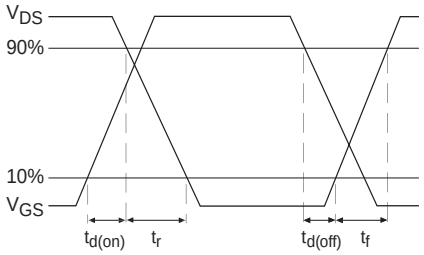


Fig 10b. Switching Time Waveforms

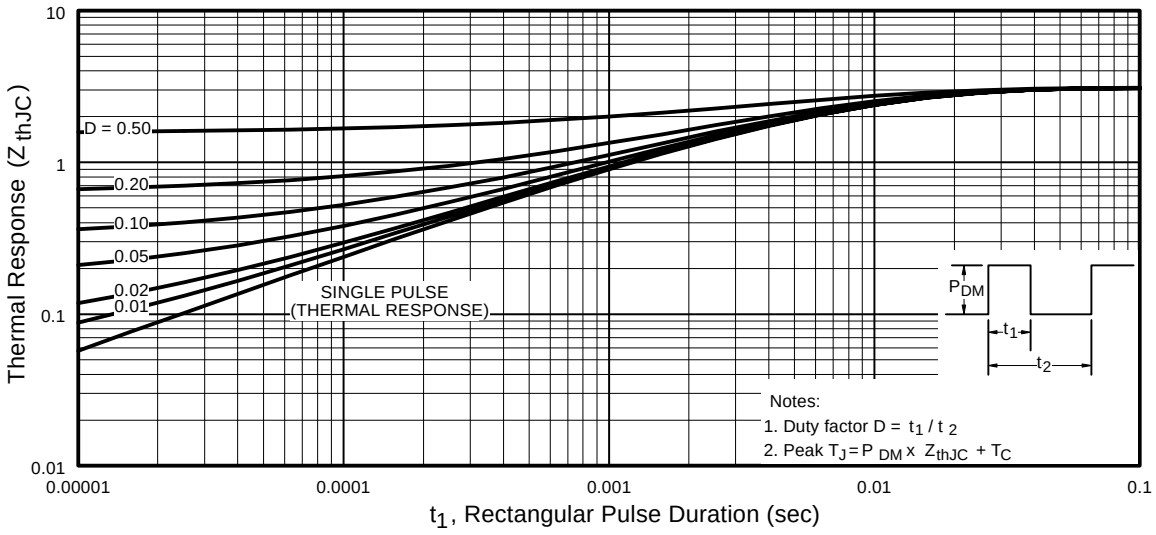


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

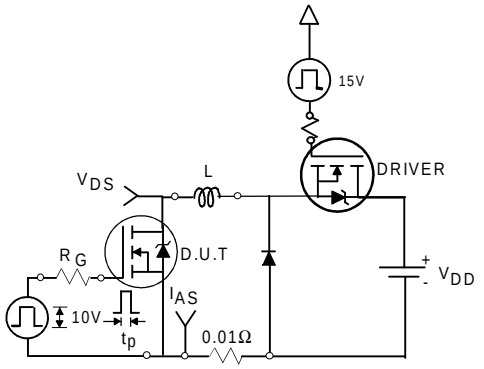


Fig 12a. Unclamped Inductive Test Circuit

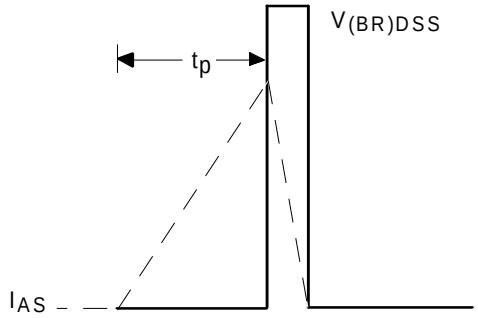


Fig 12b. Unclamped Inductive Waveforms

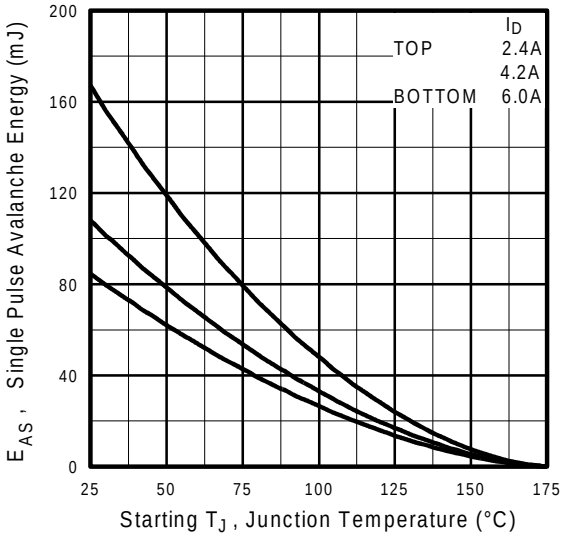


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

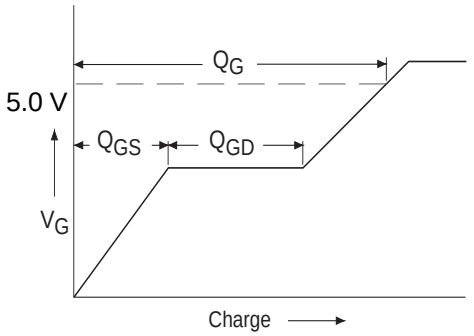


Fig 13a. Basic Gate Charge Waveform

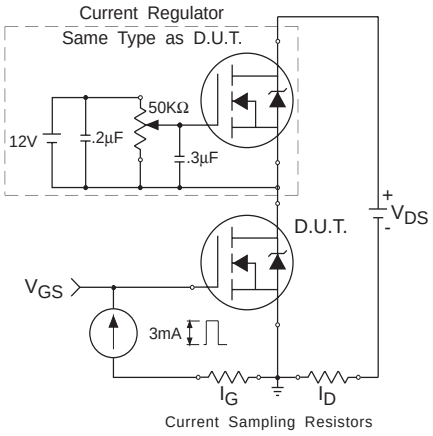
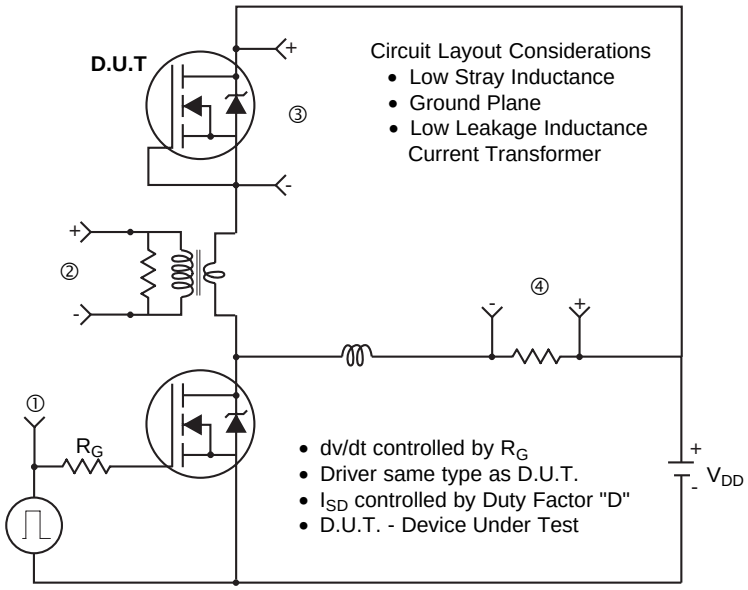
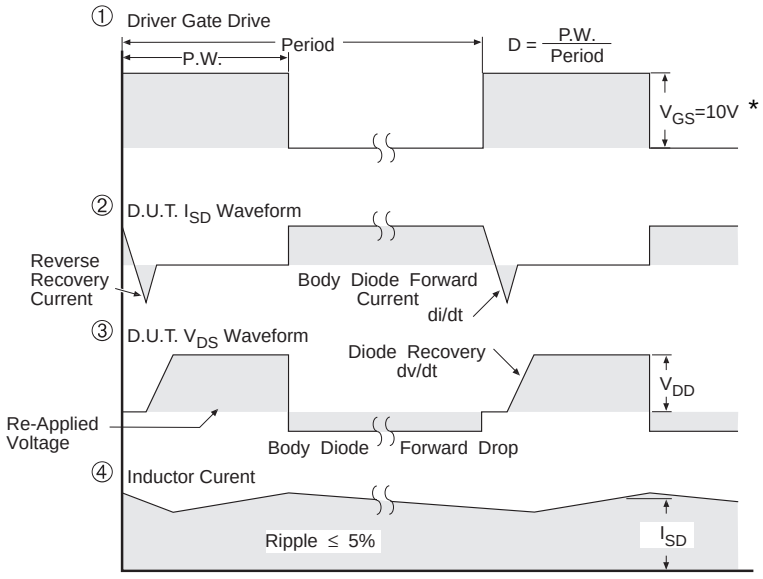


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



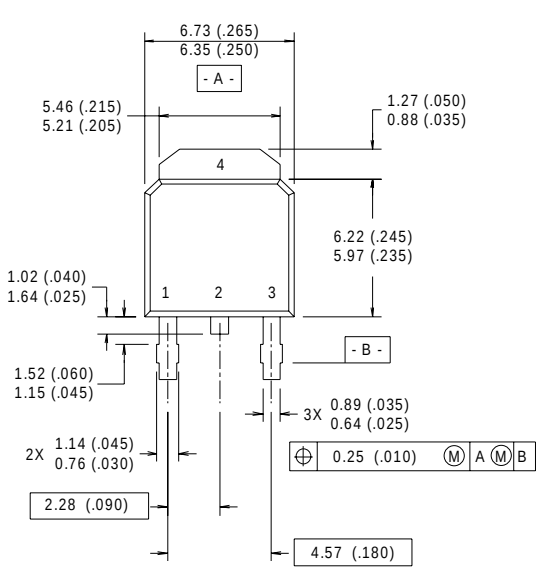


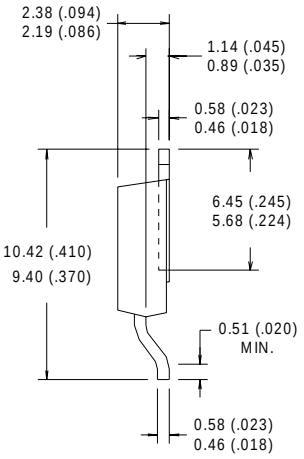
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-252AA Outline
Dimensions are shown in millimeters (inches)





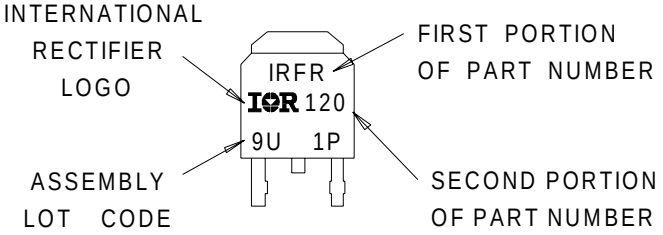
LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Part Marking Information

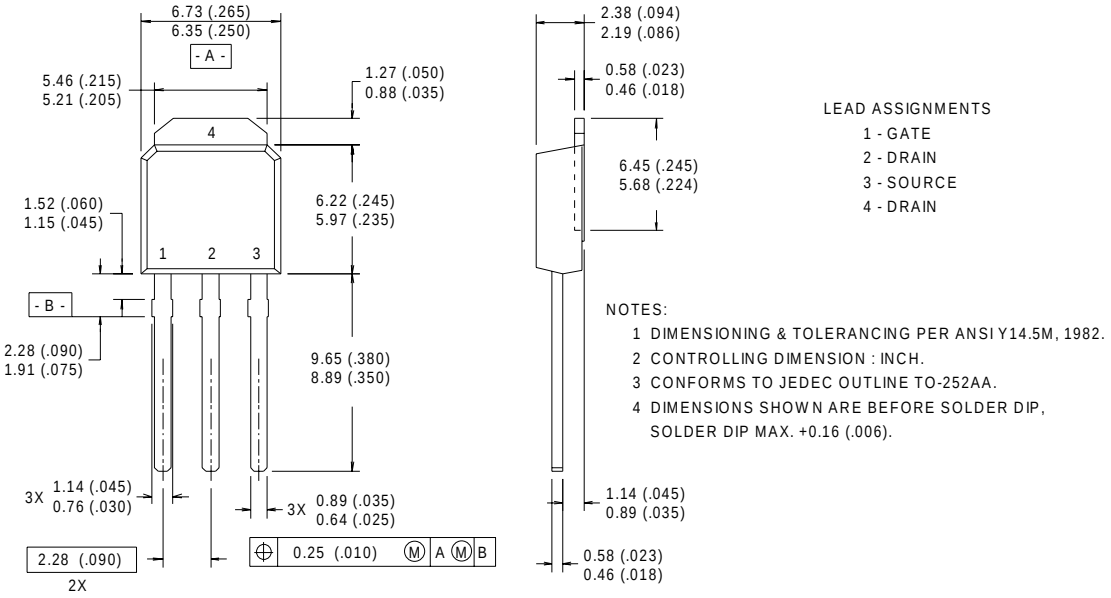
TO-252AA (D-PARK)

EXAMPLE : THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



Package Outline

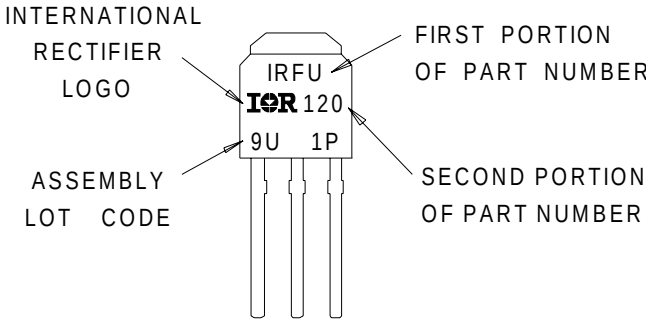
TO-251AA Outline
Dimensions are shown in millimeters (inches)



Part Marking Information

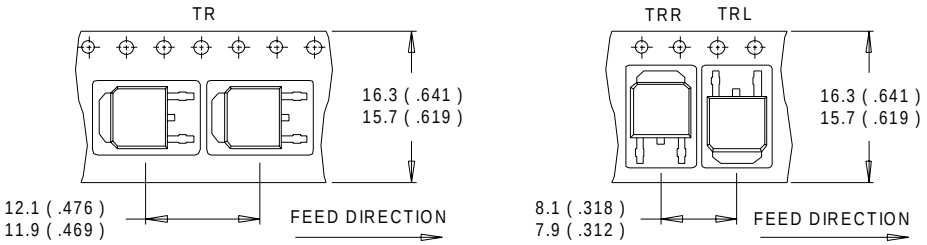
TO-251AA (I-PARK)

EXAMPLE : THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 9U1P

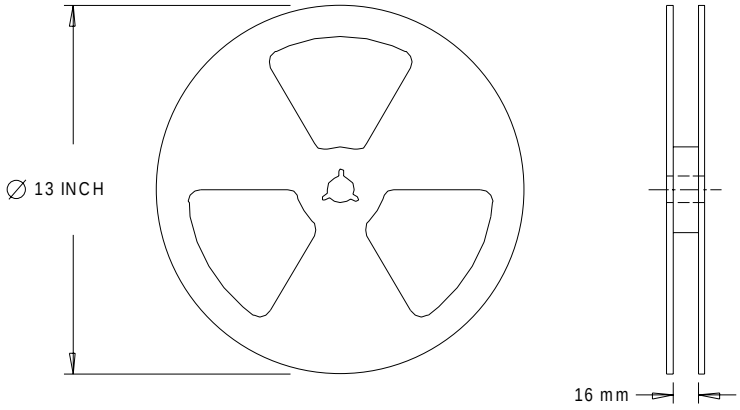


Tape & Reel Information

TO-252AA



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T 3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: 171 (K&H Bldg.) 30-4 Nishi-ikebukuro 3-chome, Toshima-ku, Tokyo Japan Tel: 81 33 983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 16907 Tel: 65 221 8371

Data and specifications subject to change without notice. *5/98*

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/