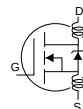


Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.052	—	$V/^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	—	0.040	Ω	$V_{GS} = 10V, I_D = 16A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	6.5	—	—	S	$V_{DS} = 25V, I_D = 16A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	34	nC	$I_D = 16A$
Q_{gs}	Gate-to-Source Charge	—	—	6.8		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	14		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	7.0	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	49	—		$I_D = 16A$
$t_{d(off)}$	Turn-Off Delay Time	—	31	—		$R_G = 18\Omega$
t_f	Fall Time	—	40	—		$R_D = 1.8\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	700	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	240	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	100	—		$f = 1.0MHz$, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	29	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	100		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	$T_J = 25^\circ\text{C}$, $I_S = 16A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	57	86	ns	$T_J = 25^\circ\text{C}$, $I_F = 16A$
Q_{rr}	Reverse Recovery Charge	—	130	200	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

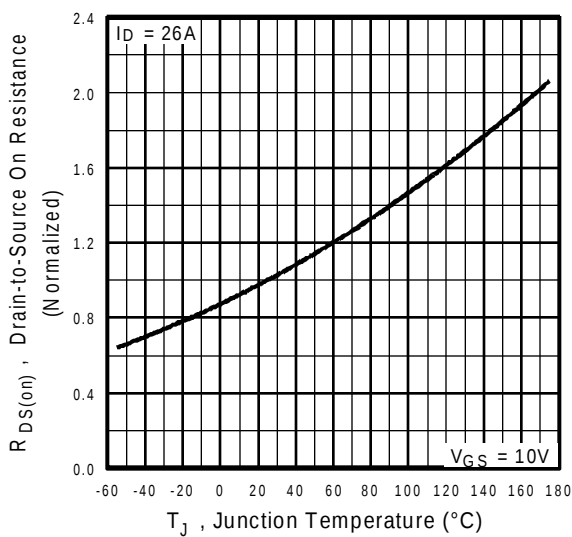
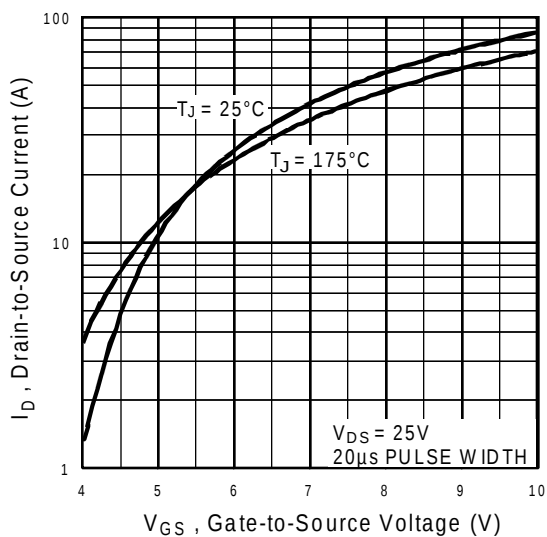
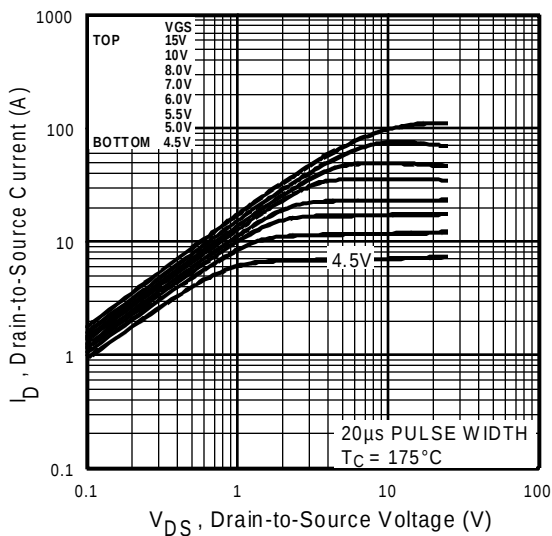
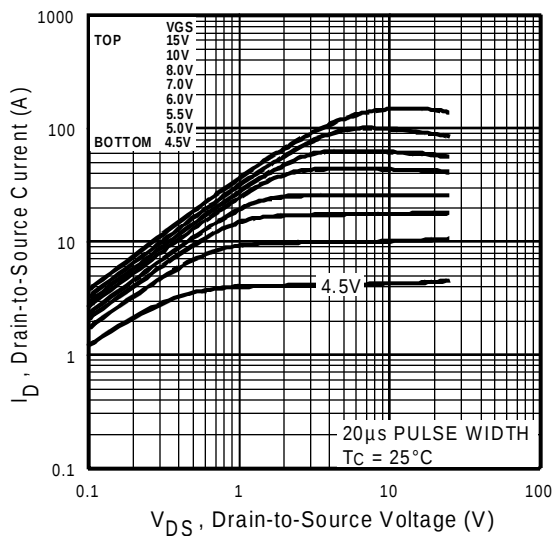
Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

③ $I_{SD} \leq 16 A$, $di/dt \leq 420A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 410\mu H$
 $R_G = 25\Omega$, $I_{AS} = 16A$. (See Figure 12)

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.



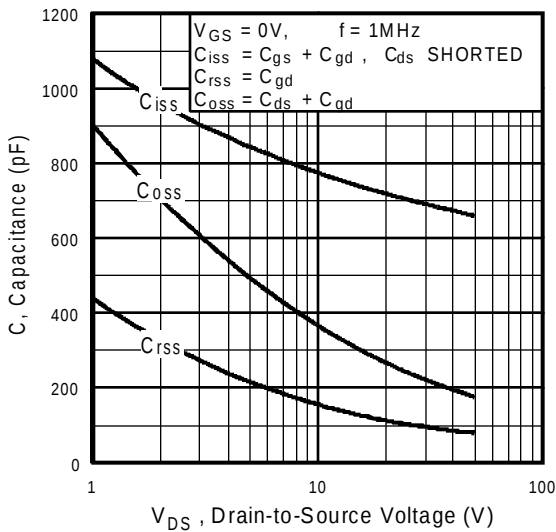


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

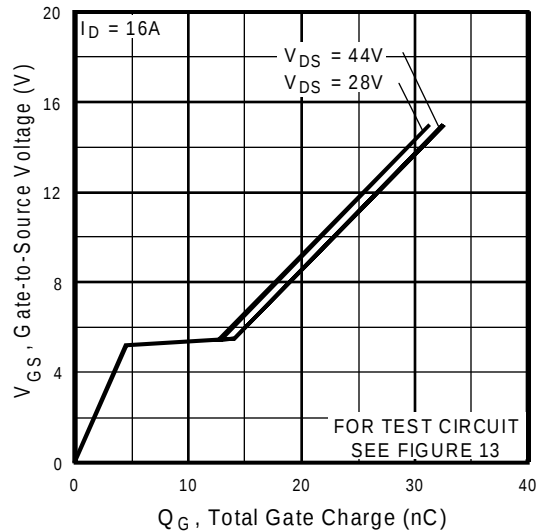


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

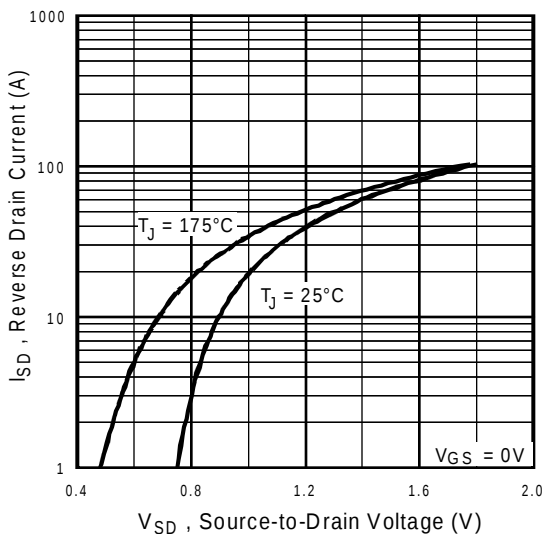


Fig 7. Typical Source-Drain Diode Forward Voltage

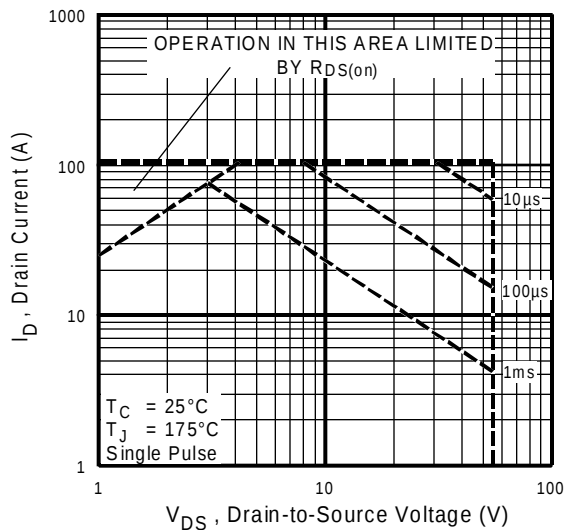


Fig 8. Maximum Safe Operating Area

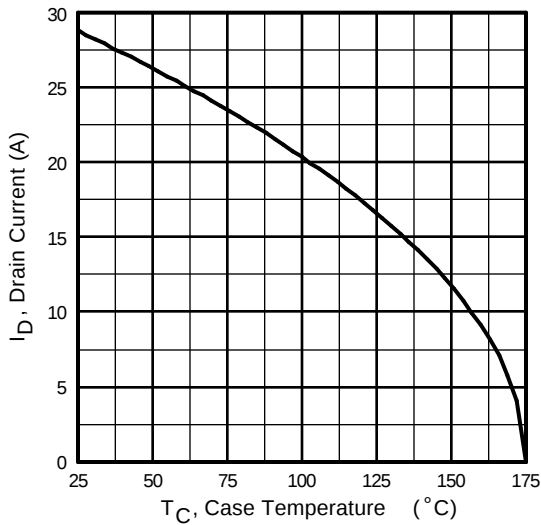


Fig 9. Maximum Drain Current Vs. Case Temperature

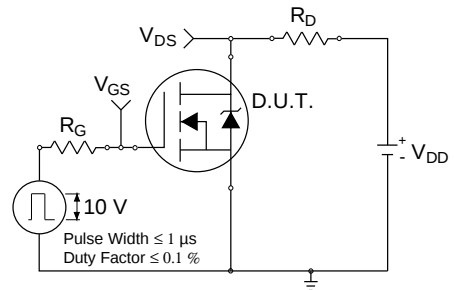


Fig 10a. Switching Time Test Circuit

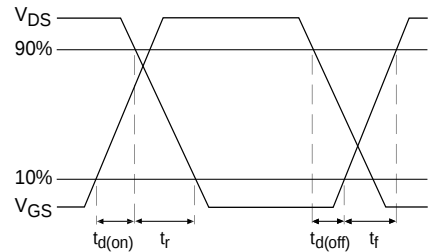


Fig 10b. Switching Time Waveforms

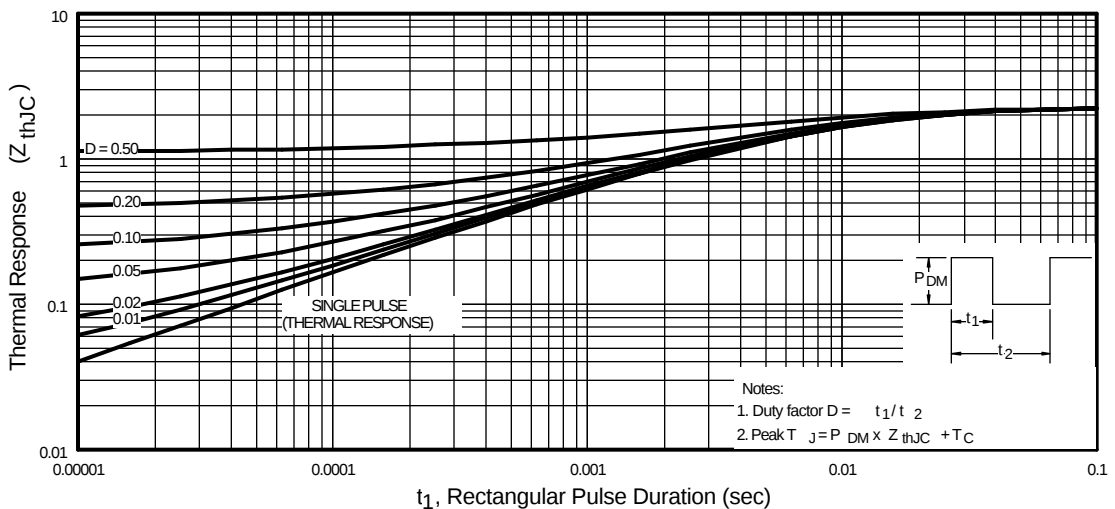


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

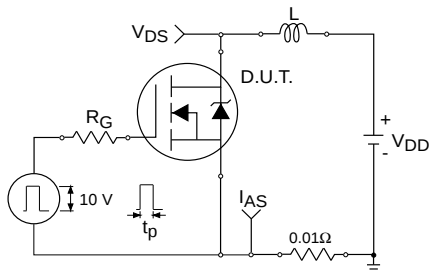


Fig 12a. Unclamped Inductive Test Circuit

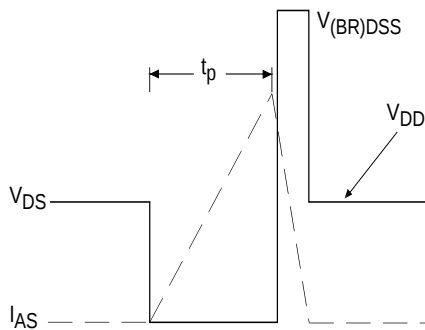


Fig 12b. Unclamped Inductive Waveforms

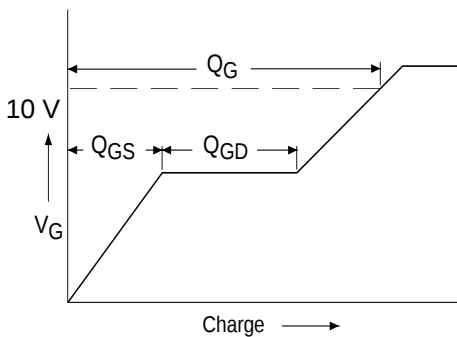


Fig 13a. Basic Gate Charge Waveform

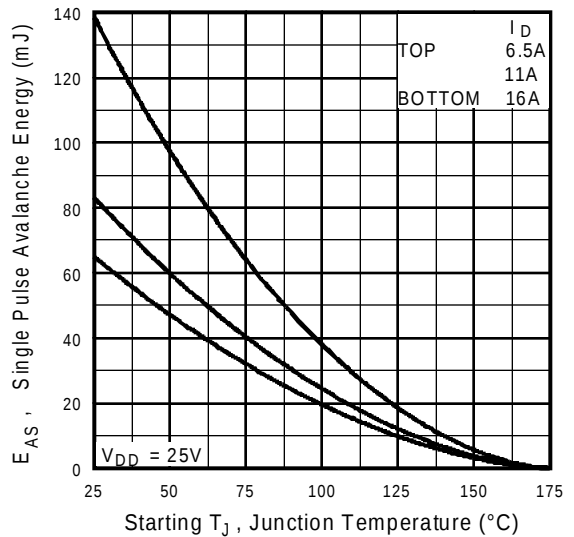


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

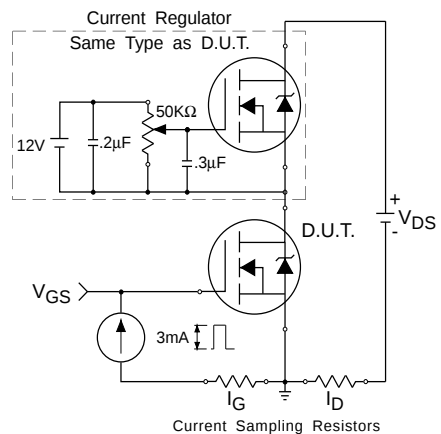
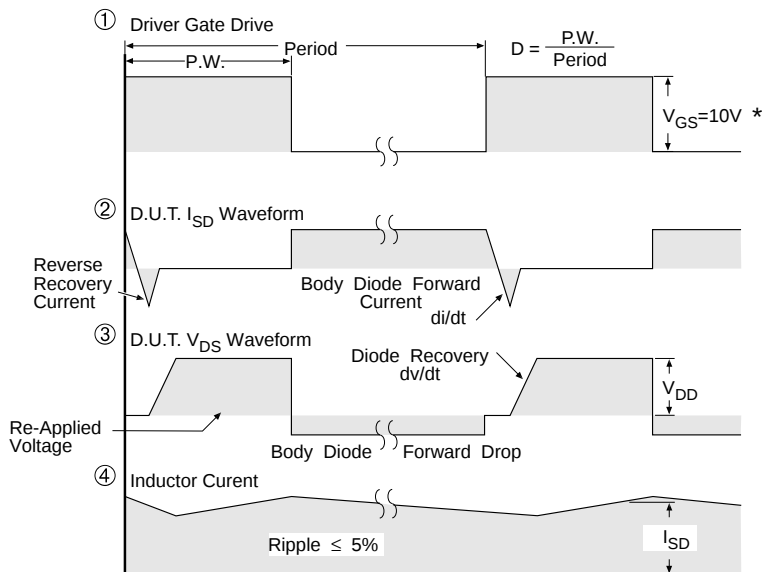
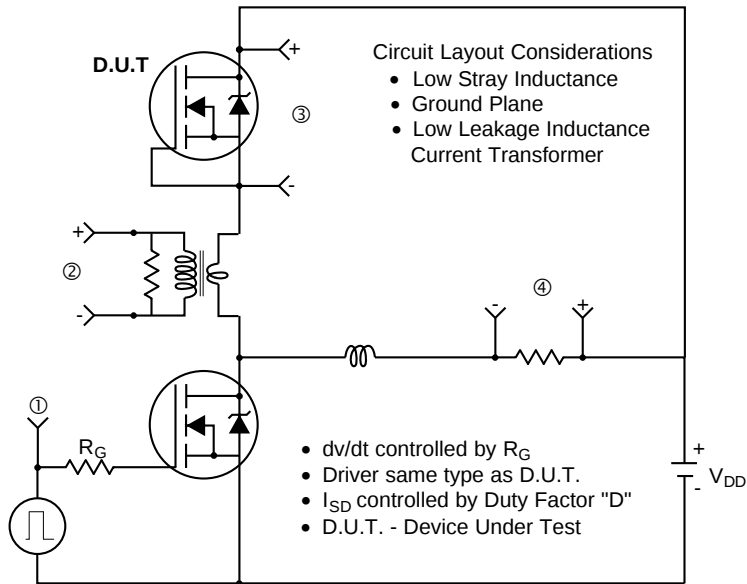


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



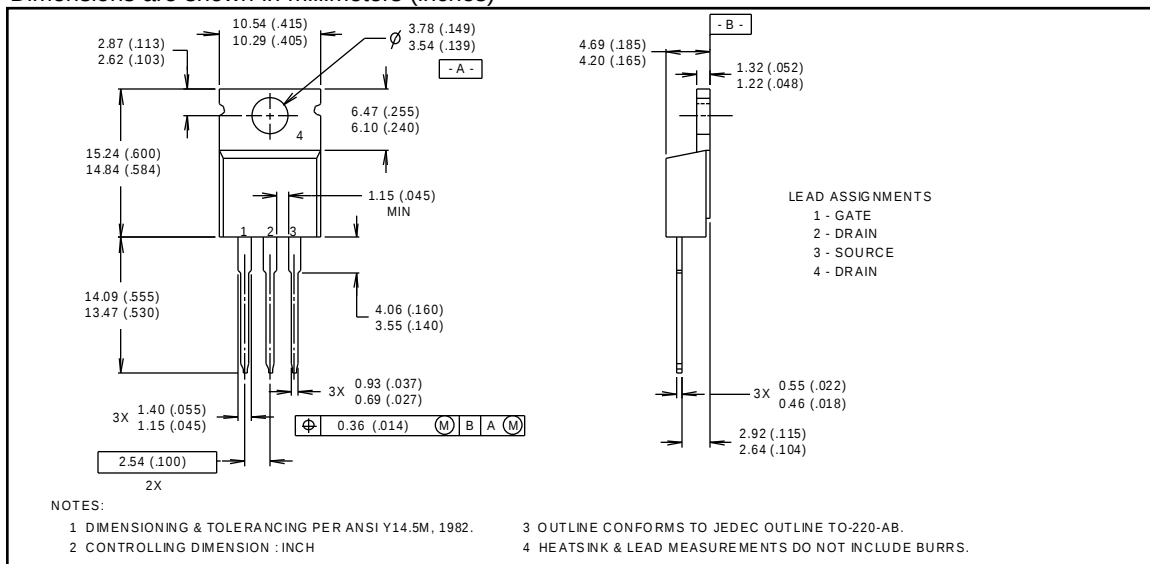
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-220AB Outline

Dimensions are shown in millimeters (inches)



Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M

