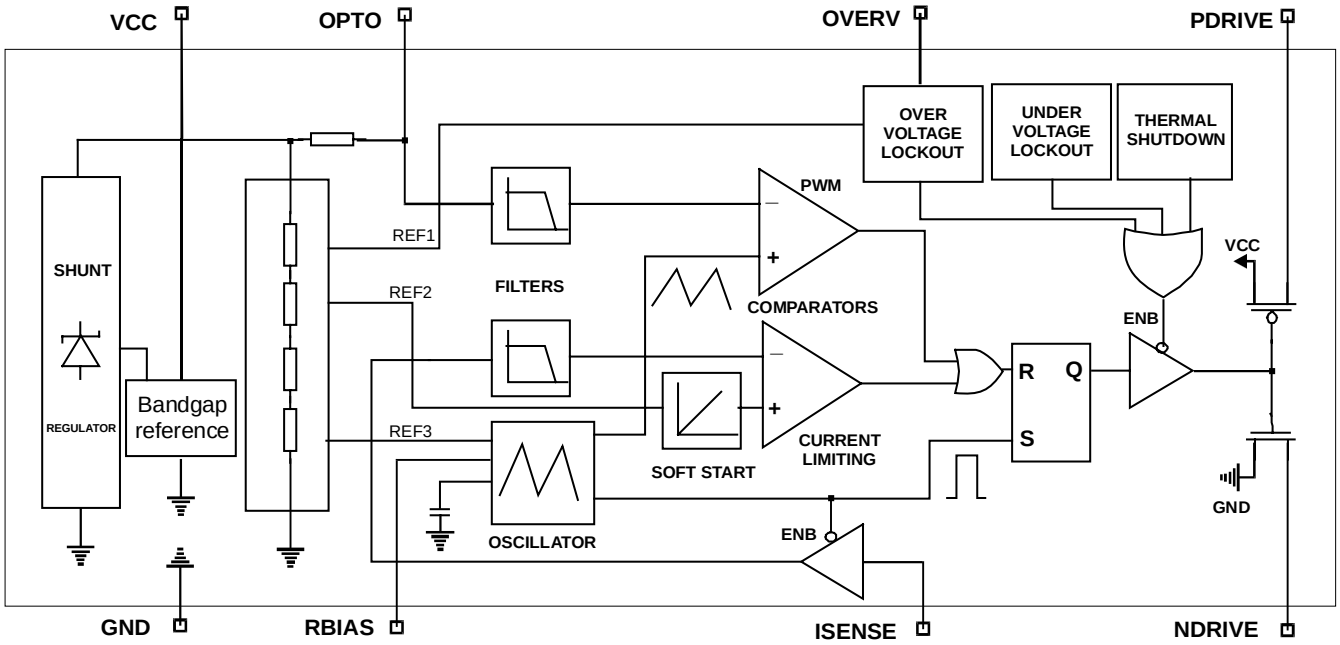
FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION SCHEMATIC: AC IN 110V, 5W OUTPUT, zener regulation (EMC components not shown).

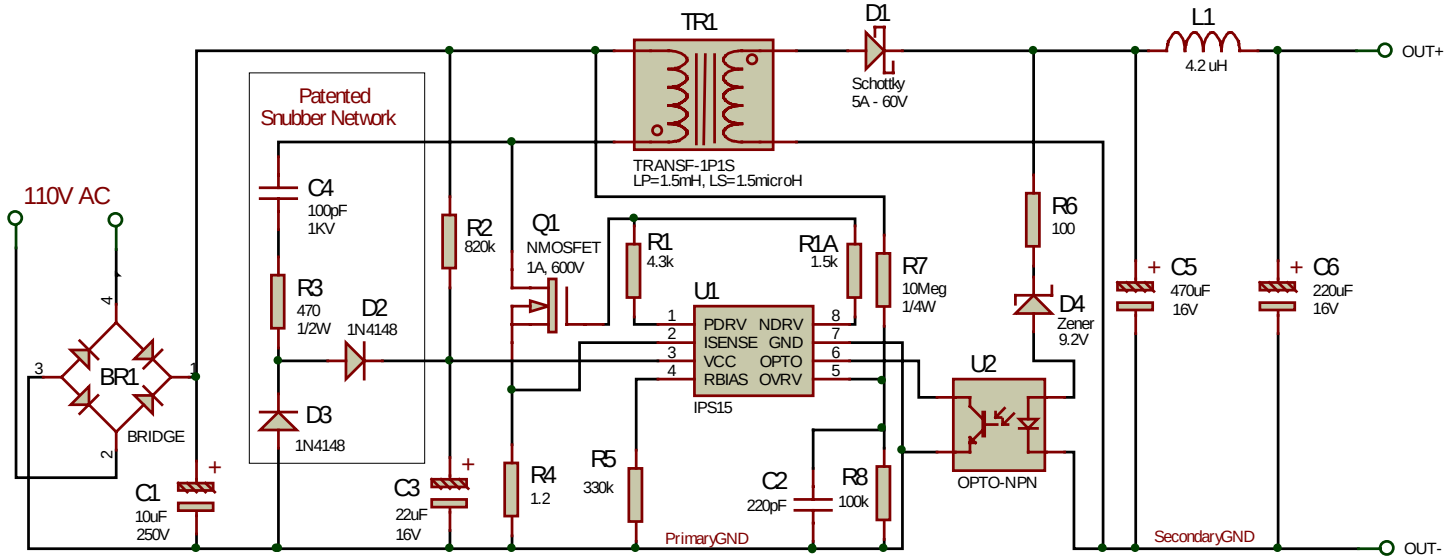


Figure 1

PIN DESCRIPTION

Number	Name	Description
1	PDRIVE	Internal P drive terminal to be connected to the gate of the outside power MOSFET. (The rising edge can be adjusted with an external resistor)
2	I_{SENSE}	MOSFET current sensing. Any voltage over 700 mv @ 25°C on this pin will stop gate pulses.
3	V_{CC}	IC positive supply. The chip behaves like a 9.5 volts zener diode.
4	R_{BIAS}	External R_{BIAS} connection to set the operating frequency.
5	OVERV	Over-voltage lock-out pin. @ 25°C a voltage over 4V on this pin will pull the MOSFET gate to GND.
6	OPTO	Feedback input
7	GND	Ground
8	NDRIVE	Internal N drive terminal to be connected to the gate of the outside power MOSFET. (The falling edge can be adjusted with an external resistor)

IN-PLUG® IPS15 SERIES FUNCTIONAL DESCRIPTION

The **IPS15** is a PWM controller for fly-back switching power supply applications. It has been optimized to reduce the external component count. The principal features are:

- Low start Current.
- Shunt regulator to allow the maximum flexibility to power the chip.
- Protections against overheating, under-voltage and over-voltage.
- Precise oscillator with externally adjustable frequency.
- On-chip filters for the loop compensation and the over-current sensing.
- Soft start and over-voltage shut-down to protect the MOSFET.
- Separate MOSFET P and N drivers to adjust rising and falling edge independently.

The shunt regulator operates like a zener diode, keeping the chip supply voltage around 9.5 volts. At start-up the chip stays in stand-by mode until the voltage of VCC reaches about 9.5 volts. During this phase, the consumption is of the order of 120 µA. When the 9.5 volts are reached, the driver starts providing gate pulses. The chip will go back to the stand-by mode if the supply voltage decreases down to ~8 volts. The overall chip consumption in normal operation is about 600 µA, not counting the current required to drive the MOSFET gate.

For domestic application, the chip can be supplied from the rectified line voltage through a resistor. In such case, the resistor has to be sized to drive enough current to the chip.

For international applications, the IC gets the start current from a resistor connected to the rectified line voltage (~150 µA) then, after the first gate pulse, the patented modified snubber network (*) provides the additional current to keep the chip running.

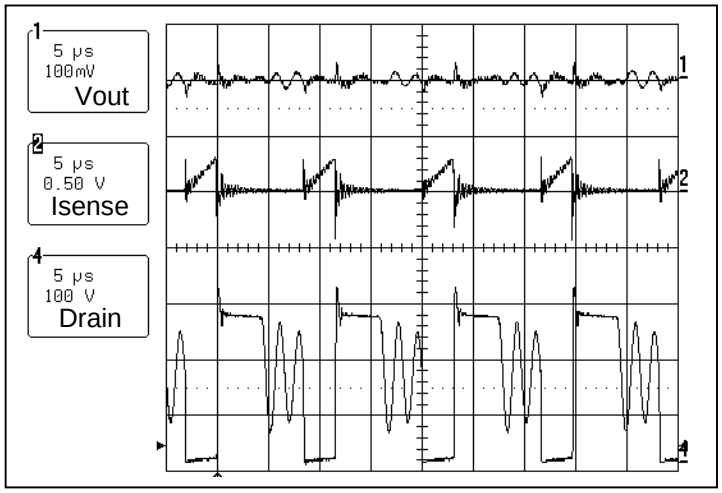
The opto pin is pulled to VCC through an internal resistor, allowing a maximal duty cycle of 60 %. During start-up, the duty cycle is controlled by the internal soft start unit which smoothly increases the MOSFET current up to its maximum, corresponding to 700mV developped across the sense resistor.

When the expected output voltage is reached, the optocoupler's led is driven, and the opto pin voltage decreases, reducing the duty cycle to a controlled value. The current limiting protection operates by turning-off the MOSFET when the ISENSE pin voltage exceeds ~700 mv. This ensures a cycle to cycle protection of the MOSFET and provides a mean of operating the power supply in constant-power mode.

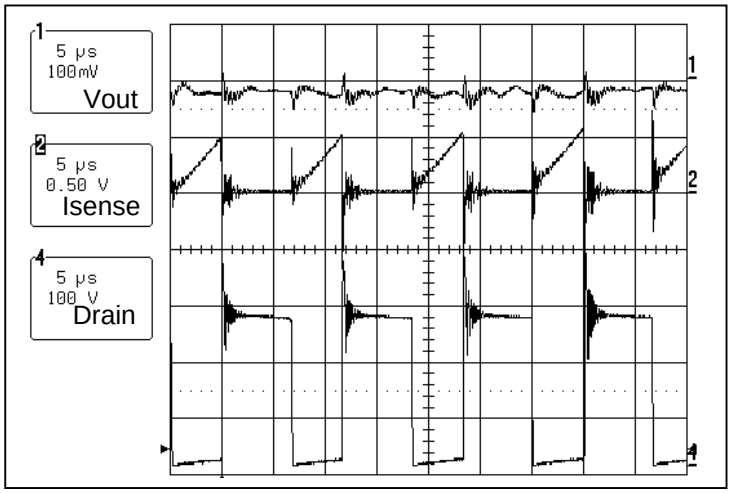
The voltage limiting protection operates by turning-off the MOSFET when the OVERV pin voltage exceeds 4V.

(*) *US Patent # 6,233,165* - ***Royalty free licence for IN-PLUG® Customers.***

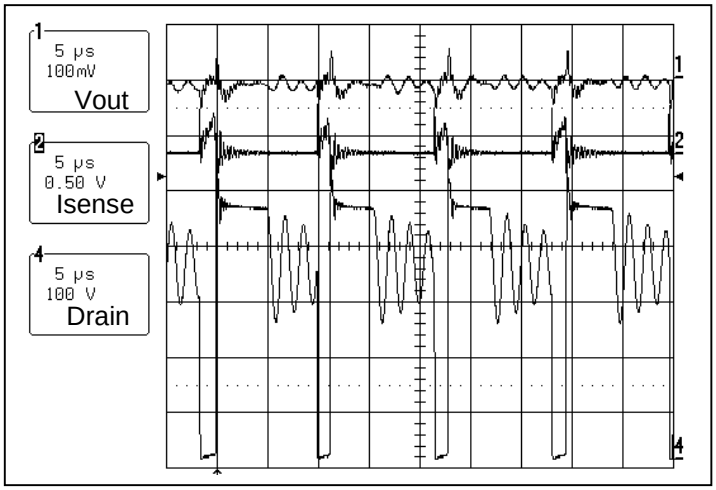
AC 110V- IPS15 operations at medium load (5W)*



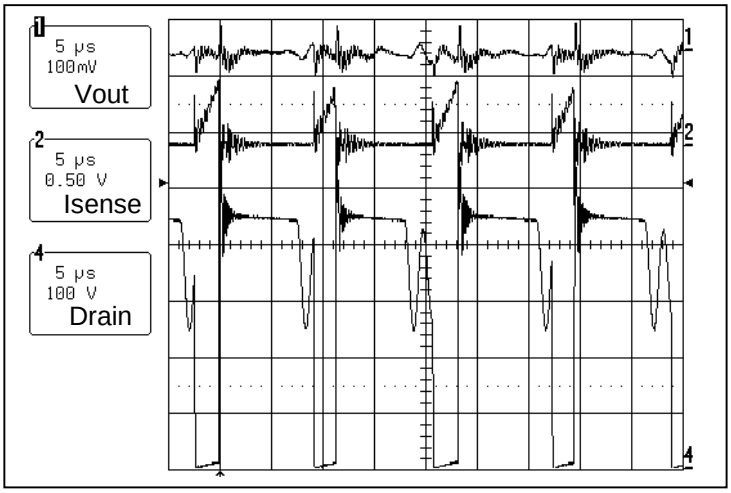
IPS15 operations at heavy load (15W)*



AC 250V - IPS15 operations at medium load (5W)*



IPS15 operations at heavy load (15W)*



***** Together with a 1A, 600V MOSFET.

OUTPUT POWER CAPABILITY			
Part Number	**Package**	**230V AC or 115V AC w/ Doubler**	**85 – 285V AC**
IPS15	**DIP-8 / SOIC-8**	**Up to 70W (1)**	**Up to 30W (1)**

Note (1): Governed by size and package of external MOSFET

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING		
Characteristics	**Value**	**UNITS**
Shunt regulator max I_{CC} (pin 3) - see fig 4-	50	mA
All analog inputs (pin 2, 4, 5, 6)	Min= -0.3, Max= +6.3V	V
Peak drive output current (pin1)	Source=100, Sink=170	mA
Junction to case thermal resistance $R_{\theta J-C}$	PDIL = 42, SOIC = 45	°C / W
Junction to PCB thermal resistance $R_{\theta J-A}$	PDIL = 125, SOIC =155	
Power dissipation for T_A <= 70°C	PDIL = 640, SOIC = 500	mW
Operating junction temperature	- 40 to 150	°C
Storage temperature range	- 55 to 150	
Lead temperature (3 mm from case for 5 sec.)	260	

PARAMETER	TEST CONDITIONS	PARAMETERS			UNITS
	@ 25°C unless specified	MIN.	TYP.	MAX.	
Supply, bias & circuit protection					
Shunt regulator voltage	ICC = 1 to 30 mA	9.2	9.7	10.5	V
Shunt regulator dynamic resistance (see Fig. 4)	1 to 30 mA	2	3	5	Ω
Shunt regulator max peak repetitive current		-	35	-	mA
Min I_{CC} to start oscillator		-	-	140	µA
Under voltage lock-out		V_{CC} – 2.2	V_{CC} - 1.5	V_{CC} - 1.4	V
Min I_{CC} to ensure continuous operation	1A, 600V, 5 nC MOSFET	1.1 @ 20KHz	3.2 @ 80KHz	4.9 @ 150KHz	mA
Current limiting sensing voltage		655	700	745	mV
Temperature coefficient of current limiting		-	-	50	µV/°C
Overvoltage sensing voltage		3.85	4	4.15	V
Soft/start duration	0 to 700mV	-	20	-	clock cycles
Leading edge blanking		200	-	450	ns
Thermal shutdown trip temperature		-	150	-	°C
Oscillator & PWM					
Range of operating frequencies		30	80	150	KHz
RBIAS values for above frequencies (see figure 2)		550	170	80	KΩ
Oscillator stability with supply & temperature (see figure 3 for average)	I_{CC} = 5 mA Temp = 0 to 70°C	-1.5	-	1.5	%
Maximum duty cycle		-	66	-	%
Minimum duty cycle		-	0	-	%

ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETER	TEST CONDITIONS	PARAMETERS			UNITS
	@ 25°C unless specified	MIN.	TYP.	MAX.	
Error amplifier					
Sensitivity in mV / % of PWM		-	54	95	mV
Voltage for max duty cycle	OPTO pin	-	4	-	V
Voltage for min duty cycle	OPTO pin	-	0.5	-	V
Input impedance	OPTO pin	-	60	-	KΩ
P & N Outputs to MOSFET gate					
P gate driver saturation	10 mA (source)	-	-	1	V
N gate driver saturation	10 mA (sink)	-	-	0.6	V
Gate pull-down resistor	(internal)	280	400	520	KΩ
PDRIVE Rise time (10% to 90%)	240 pF load	-	250	-	ns
NDRIVE Fall time (10% to 90%)	240 pF load	-	100	-	ns
Max recommanded total external MOSFET charge	@ 20 KHz	-	-	100	nC
"	@ 80 KHz	-	-	50	nC
"	@ 150 KHz	-	-	15	nC

Note: Electrical parameters, although guaranted, are not all 100% tested in production.

Figure 2: Frequency vs Rbias

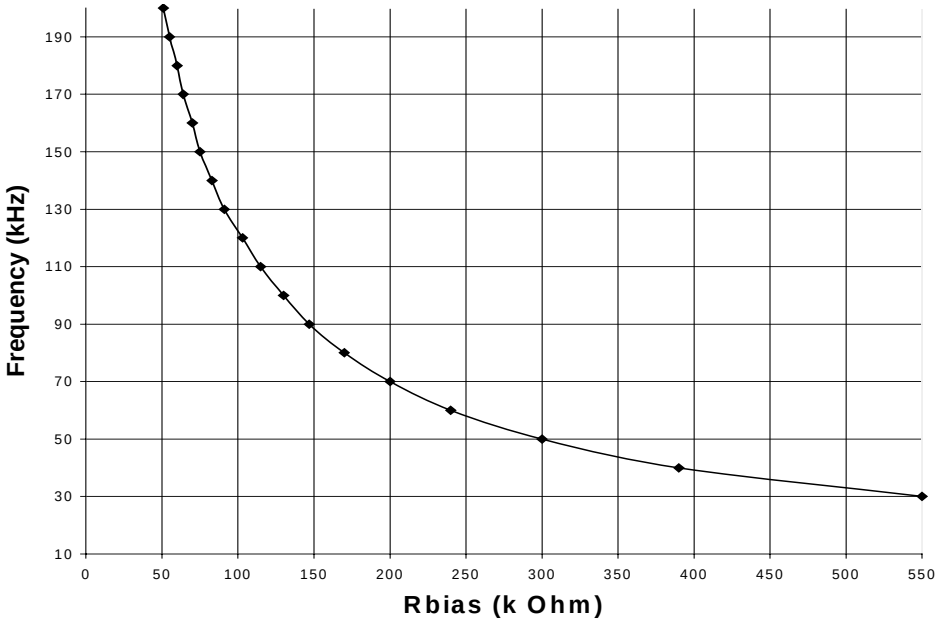


Figure 3 Frequency drift vs temperature

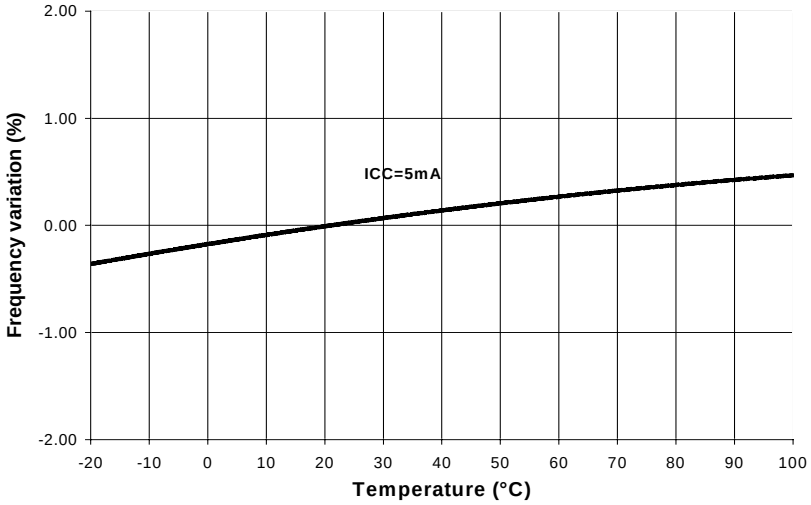
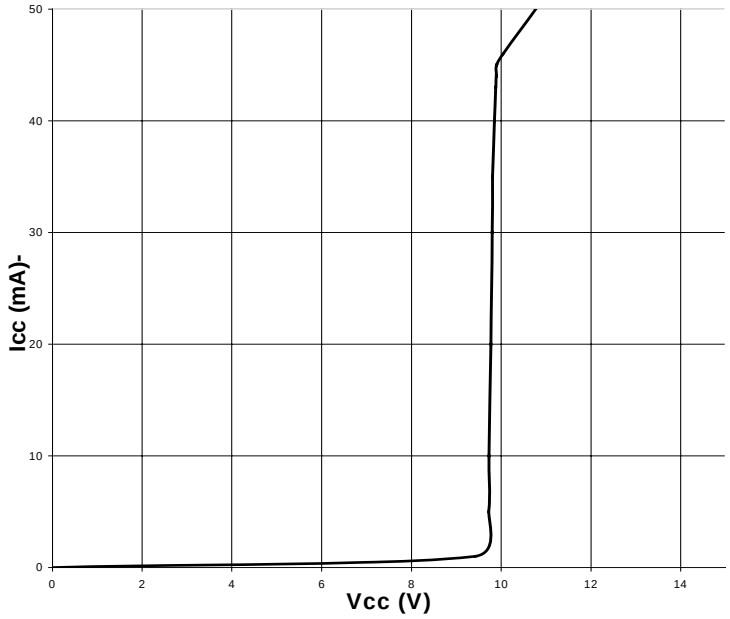


Figure 4 Shunt regulator Icc current



ORDERING INFORMATION

Part No.	ROHS / Pb-Free	Package	Temperature Range	
IPS15C-D	-G-LF	8-Pin PDIP	0°C to +70°C	Commercial
IPS15I-D	-G-LF	8-Pin PDIP	-40°C to +85°C	Industrial
IPS15C-SO	-G-LF	8-Pin SOIC	0°C to +70°C	Commercial
IPS15I-SO	-G-LF	8-Pin SOIC	-40°C to +85°C	Industrial

For detailed ordering information, see page 14

GOOD DESIGN PRACTICES

IPS15 and loop stability:

The IPS15 is intrinsically very fast and doesn't participate to the loop stability. It only involves a comparator that doesn't bring any gain and exhibits a negligible phase shift.
It has been designed on purpose to allow its utilization in a large range of applications:
(a) Operating at frequencies up to 200 kHz and even above,
(b) Involving very different types of loop stability from "cycle skipping" where the loop is not compensated at all (figure 1), to good stability achieved through the utilization of a TL431 (figure 5) and finally superior transient response when using the IPS25 feedback controller (figure 6).
The loop compensation is entirely achieved on the load side and the feedback is performed by an optocoupler which gain and dynamic response play an important role in the loop stability.

Precaution in selecting the optocoupler:

The optocoupler must be **using a Phototransistor** and **NOT** a Photodarlington. Most optocouplers of this type are offered in a wide range of coupling efficiency, also called transfer ratio. Even the cheapest ones have a guaranteed transfer ratio of the order of 100% meaning that 1mA of current in the IR LED creates approximately 1mA of current in the receiving phototransistor. The user should be able to design the loop to be stable even though the actual transfer ratio differs by more than a factor of 3 (example from 100% to 300% or 50% to 150%).
Unfortunately optocouplers were not designed for low-current applications and this results in very bad speed and saturation characteristics for the phototransistor which could become incredibly slow and create severe loop stability problems should it be allowed to saturate hard in the application (the optocoupler could cause the IPS15 to skip cycles due to the long time required by the opto transistor to go out of saturation).
In the example of figure 5, the output voltage is 10 volts as defined by R15 and R16 and 2.5V at the Pin #1 of the TL431. The cathode of the TL431 can go to a voltage as low as 2 Volts. The IR LED requires approximately 1 Volt which means that the voltage drop across R14 could be up to 6 volts resulting in a maximum current of 700uA. This value is plentiful for the utilization of a broad range of optocouplers and yet small enough to avoid hard saturation.

Loop stability with the TL431:

The TL431 has an enormous DC gain and will not ensure stability unless specific loop-compensation components such as a RC network are added as indicated below.

The RC network should have a cut-off frequency at 100Hz to roll-off the gain at low frequencies but **reach a plateau around 100Hz** and have enough AC gain at twice the line frequency and achieve a good line ripple rejection.
This is achieved by the loop compensation network **C7, R17** of figure 5. The gain rolls off until the impedance of C7 reaches the value of R7. At much higher frequencies, the gain continue to roll-off due to the natural frequency response of the TL431.
The goal is to reach a very low gain at the switching frequency.

If the addition of C7 & R17 with values as shown results in gain is too low, the values of R15 & R16 should be reduced in proportion to lower the impedance at Pin #1 of TL 431. Alternately, if the gain is too high the values of R17 should be reduced and C7 re-adjusted accordingly to maintain the required cut-off frequency.
Criteria to calculate the network :
1) R17 must be much higher than the input resistance of TL431 constituted by R16//R15=5K → 68Kohm OK.
2) F=100Hz=1/(2 x 3.14 x R17 x C7) gives approximately 22,000 pF for C7.

Discontinuous operation:

Check discontinuous mode of operation of the transformer (see application note AN-IPS02 page 2 for details)
to ensure that the Flyback SMPS is indeed operating in discontinuous mode in the entire range of Input Voltages and Output Current. The response of the SMPS drastically changes in continuous mode, it gets considerably slower which requires a totally different loop compensation technique. Remember that it is very difficult to ensure loop

stability with a simple schematic when the SMPS is allowed to transition between Discontinuous and Continuous modes.

MOSFET driver protection:

The MOSFET driver has been sized to be capable of driving power MOSFETs featuring a total gate charge up to 100nC.

The MOSFET should be turned-on relatively slowly and turned-off much faster. As shown below, these 2 parameters can be independently adjusted through the external resistors R10 (pin1) and R10A (pin8).

The minimum value of these resistors should be 50Ω in order to reduce EMI and minimize the noise injection which could result from Miller-capacitance kick-back during transient conditions.

See application note AN-IPS-02 for EMI reduction techniques.

APPLICATION 2: AC IN 85-260V, 5 – 10W OUTPUT, voltage regulation with TL431.

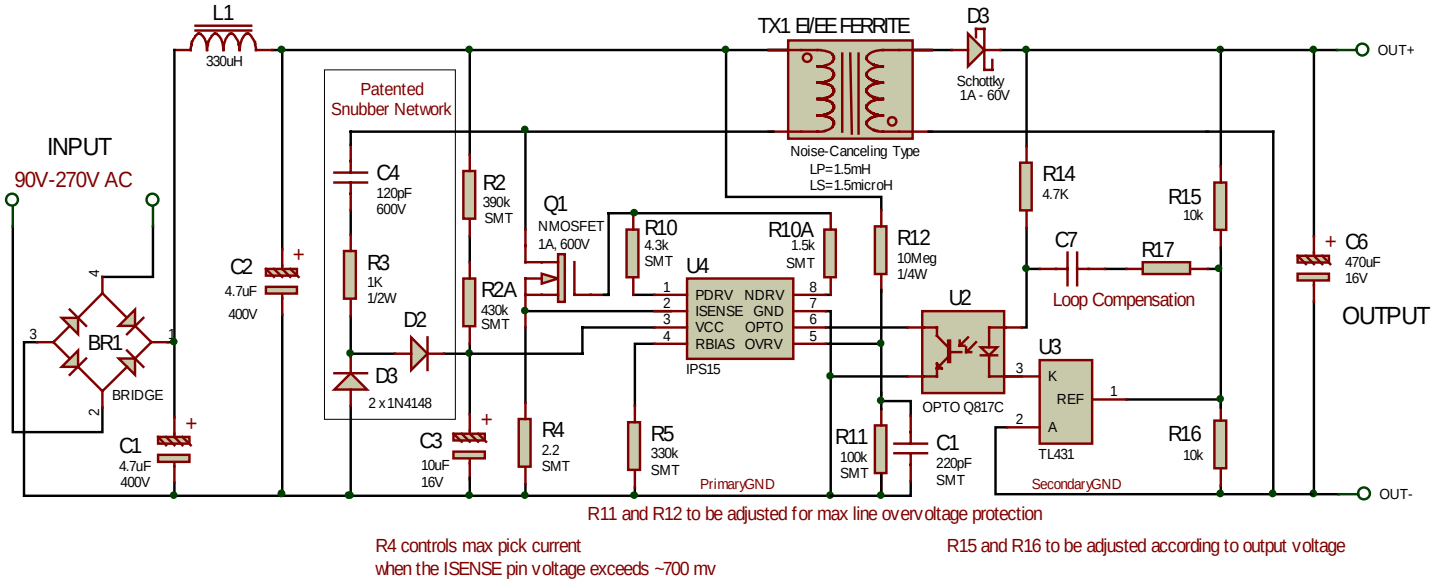


Figure 5

APPLICATION 2: AC IN 85-260V, 0 – 5W OUTPUT, current & voltage regulation with IPS25.

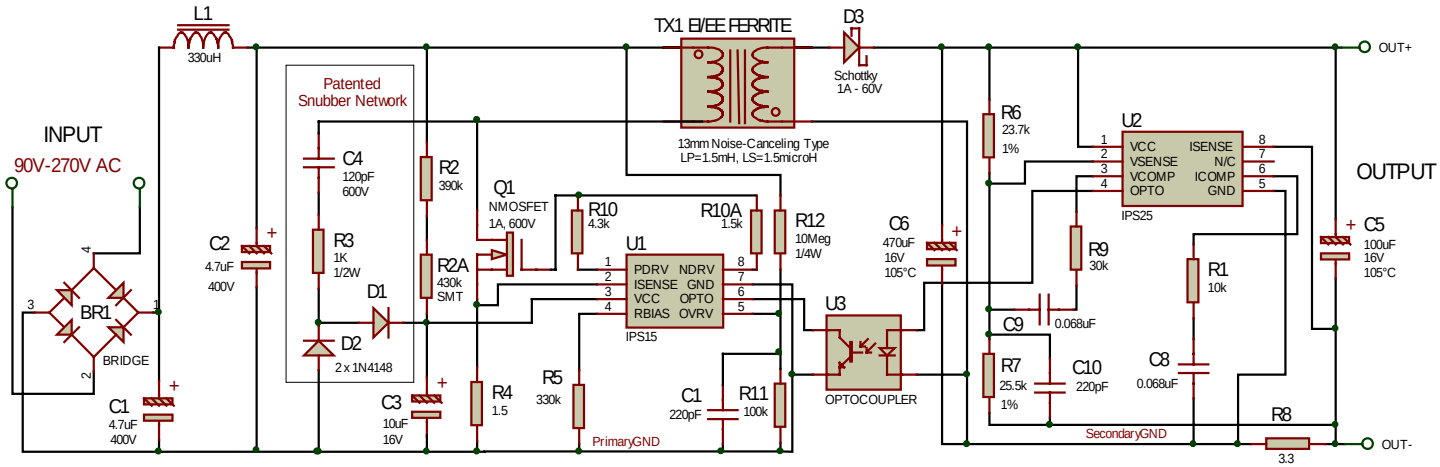


Figure 6

OUTPUT CORD SERIAL RESISTANCE COMPENSATION WITH THE IPS25 FEEDBACK CONTROLLER

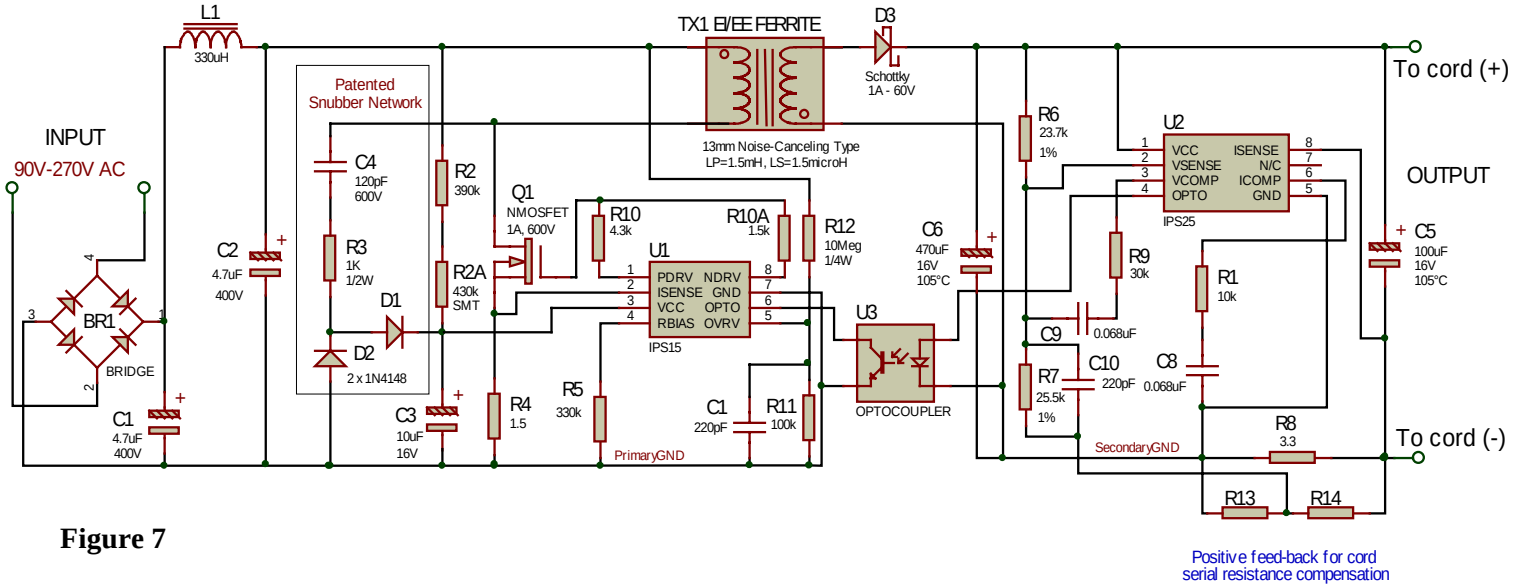


Figure 7

The voltage drop due to the output serial resistance of the cord can be compensated by adding a voltage positive feedback to the IPS25 input pin VSENSE, proportional to Vdrop. This can be achieved either by splitting R8 (output current sensing resistor) in two or by inserting 2 serial resistors R13 and R14 in parallel to R8 and connect the positive feedback to the intermediate node.

R13 and R14 should be calculated, based on the following conditions:

- (R13 + R14) ≥ 20 x R8 (but should remain low impedance in regards to R7),
- Vint ~ Vdrop, where Vint is the intermediate voltage measured on the common node of R13 and R14, and Vdrop is the voltage drop across the cord serial resistor.

SMPS with output cord

ADDITIONAL RECOMMENDATIONS:

For best results in low power off-line SMPSs with the **IPS15**, the following MOSFET features are recommended:
- Low gate charge (max 50 nC).
- 400 V breakdown voltage for domestic use (USA / Japan).
- 600V breakdown voltage for European use (800V when transformer leakage inductance is very small).
- 1, 2 or 3A depending on the maximum output power.

Examples of suitable MOSFETS:
- **IXYS PolarHT™ and Polar HV™** MOSFET series: IXTY1R4N60P, IXTY2N60P, IXTY3N60P
- **Fairchild** MOSFET series: FQPF1N60, FQPF 2N60, FQPF 3N60.
- **Infineon COOLMOS™** series: SPD01N60S5, SPD02N60S5, SPD03N60S5.
- **Motorola** MOSFET series: MTP1N60, MTP2N60, MTP3N60.
- **SGS-Thomson** MOSFET series: STD1NB60, STD2NB60, STD3NB60.
- **Etc…**

Notes:
- Due to the rapid evolution of MOSFET technologies, please check for current models when designing a new SMPS.
- **PolarHT™ and Polar HV™** are trademarks of IXYS corporation
- **COOLMOS™** is a trademark of Infineon.

TRANSFORMER CHARACTERISTICS:

(a) Transformer design:
E-core with suitable gap to prevent saturation or distributed-gap toroid. Primary inductance of 1.5 mH is very typical.
Turn ratio = 9 for 220V input or universal 85V – 265V.
Turn ratio = 7 for 100-120V AC input (Japan and USA)

(b) Transformer phasing:
Check the phase as indicated in figure 1 , 5 and 6. Also refer to application notes AN-IPS-01 and AN-IPS-02.

SNUBBER NETWORK:

With reference to figure 1, R2 provide the start-up current for the chip. C3 is being charged through R2. Once the chip supply voltage is high enough, the gate drive starts and the chip is then powered by the modified snubber network patented by our company.
The snubber values may have to be optimized for different specific operating conditions:
- R3 could be reduced to 100 ohms and sometimes eliminated.
- C4 could be increased to 200pF and sometimes more.

Depending on the characteristics of the transformer, essentially leakage inductance and distributed capacitance, the snubber network shown in figure 1, may not be efficient enough to reduce the voltage spikes when operating at 20W or above. Please refer to applications notes AN-IPS-01 and AN-IPS-02 design tips or EMI reduction techniques, or feel free to contact our technical support for assistance.

POWER SHUT-DOWN SOLUTIONS for STAND-BY REQUIREMENTS:

For low-power stand-by requirements, the primary circuitry can be shut-down by pulling the IPS15 VCC pin "LOW" through a 100Ω resistor.
This can be easily done using a:

- Simple switch
- PNP transistor
- NPN transistor

SHUT-DOWN SOLUTIONS

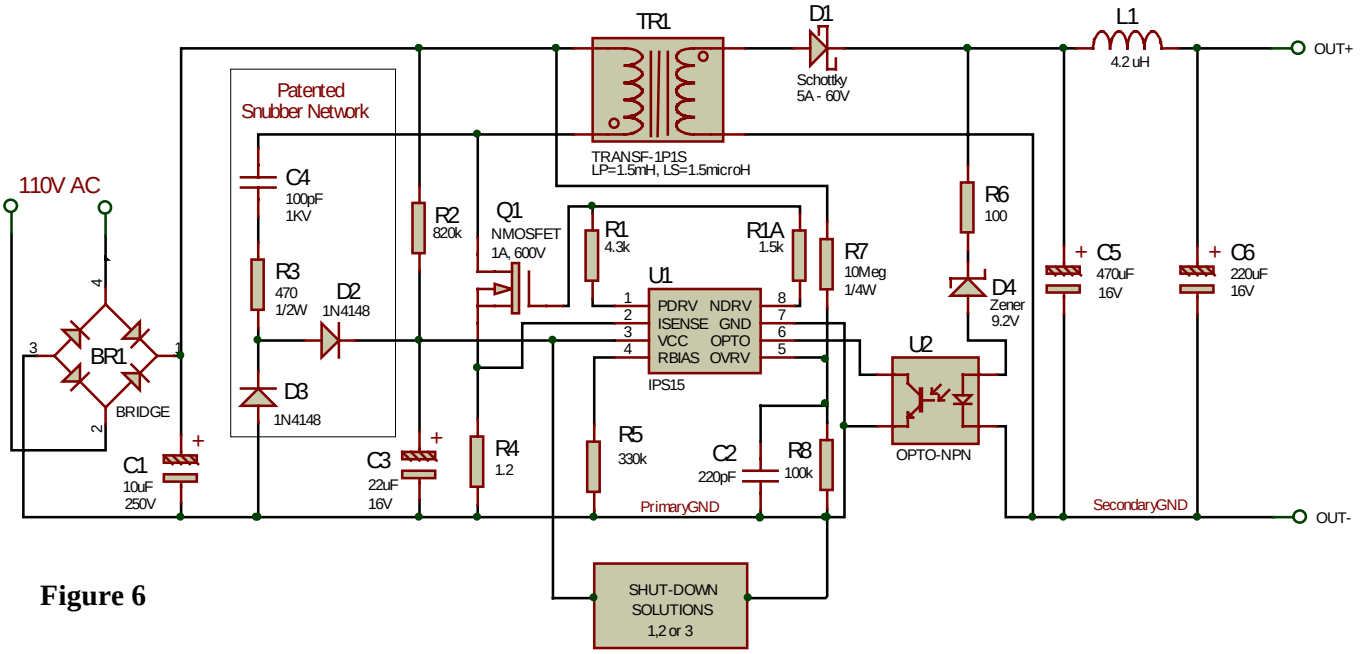
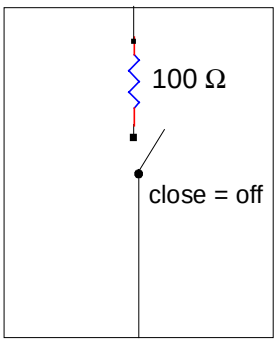
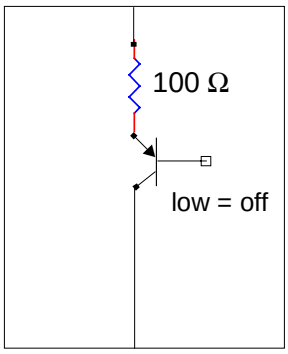


Figure 6

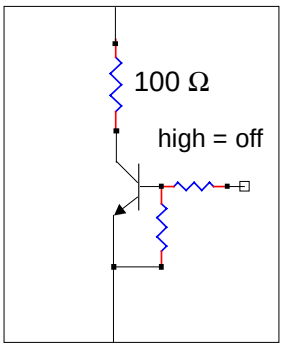
Solution 1:
simple switch, close = off
100Ω resistor
mandatory



Solution 2:
PNP transistor, low = off
(low = less than 4V)
100Ω resistor
optional



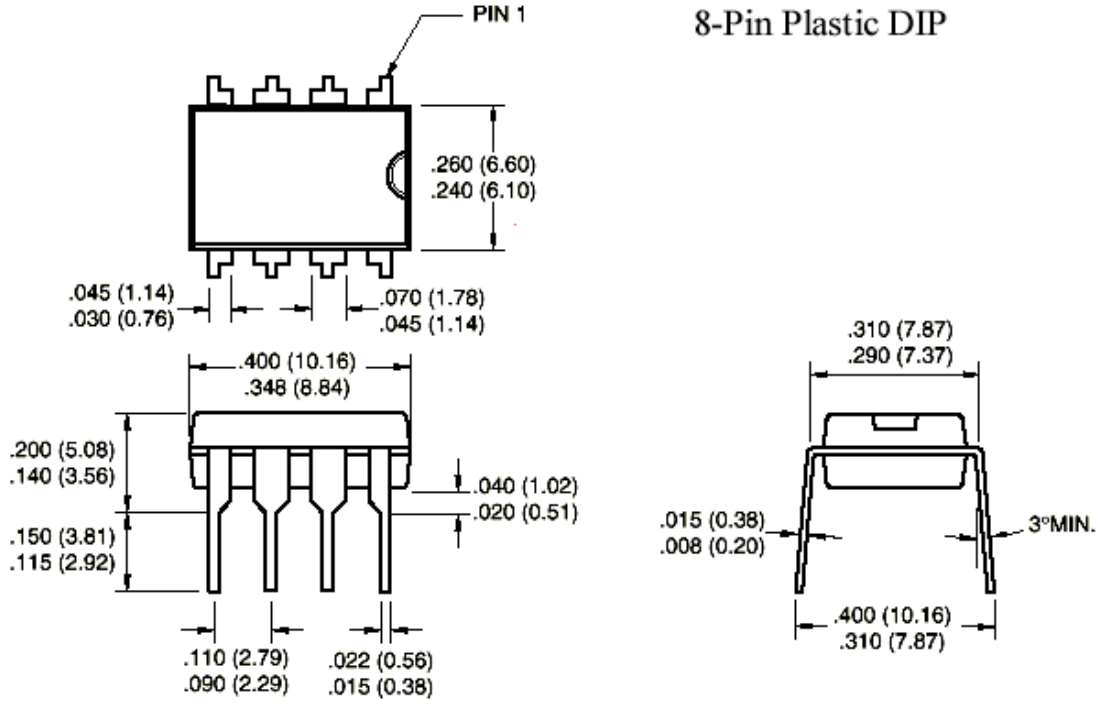
Solution 3:
NPN transistor, high = off
100Ω resistor
optional



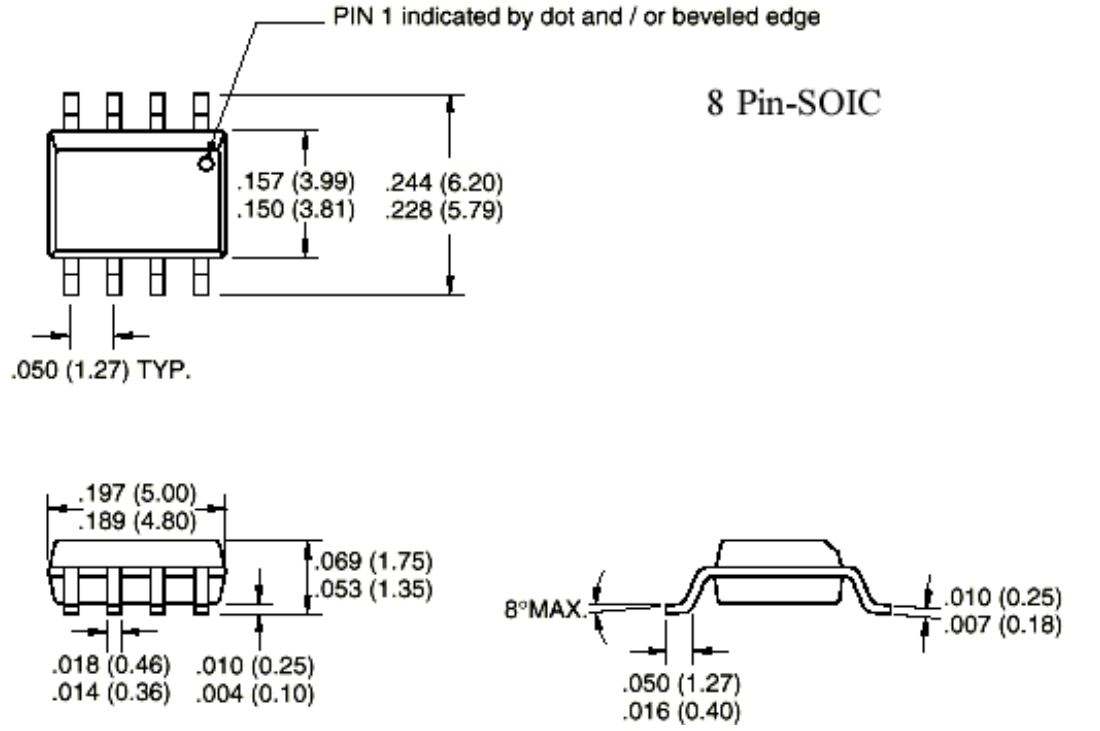
When the "LOW" state is released, the VCC is naturally re-established, re-activating the IPS15.

PACKAGE DIMENSIONS

PLASTIC DIP-8



PLASTIC SOIC-8



ORDERING INFORMATION

Part-Number

IPS XXXH C – YY – G-LF - TR

IN-PLUG® Controller Series

Flyback
Feedback
PFC
Push-Pull
LED Driver

Controller Type

Flyback: 10 series
Feedback: 20 series
PFC: 100 series
Push-Pull: 200 series
LED Driver: 400 series

"H" with hiccup overload protection

Temperature Range

C : Commercial (0, +70°C)
I : Industrial (-40°C. +85°C)
Note : Default or not specified is <commercial>

Package Type

D : DIP8
SO : SOIC8
(For production with a new date code, after January 2006, the package type will not appear anymore on package marking)

ROHS + Pb-Free

Tape and Reel

TR : Tape & Reel
TU : Tube
Note1 : Default or not specified is « tube ».
Note2 : Does not appear on package marking.

Example of Marking

Non-Green Package

Green ROHS + Pb-Free Package

(Note : For production with a new date code, since January 2006, the package type does not appear anymore on package marking)

This ordering information is for commercial and industrial standard IN-PLUG® controllers ONLY. For custom controllers or for automotive and military temperature ranges, call AAI's sales representative.

The following is a brief overview of certain terms and conditions of sale of product. For a full and complete copy of all the General Terms and Conditions of Sale, visit our webpage http://www.asicadvantage.com/terms.htm.

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The product is warranted that it will conform to the applicable specifications and be free of defects for one year. Buyer is responsible for selection of, use of and results obtained from use of the product. Buyer indemnifies and holds ASIC Advantage, Inc. harmless for claims arising out of the application of ASIC Advantage, Inc.'s products to Buyer's designs. Applications described herein or in any catalogs, advertisements or other documents are for illustrative purposes only.

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Products are not authorized for use in critical applications including aerospace and life support applications. Use of products in these applications is fully at the risk of the Buyer. Critical applications include any system or device whose failure to perform can result in significant injury to the user.

LETHAL VOLTAGES

Lethal voltages could be present in the applications. Please comply with all applicable safety regulations.

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TRADEMARKS AND PATENTS

- IN-PLUG® is a registered trademark of ASIC Advantage, Inc.
- AAI's modified snubber network is patented under the US Patent # 6,233,165. IN-PLUG® Customers are granted a royalty-free licence for its utilization, provision the parts are purchased factory direct or from an authorized agent.

PROTECTION FOR CUSTOM IN-PLUG® SOLUTIONS

When AAI accepts to design and manufacture IN-PLUG® products to Buyer's designs or specifications, buyer has certain obligations to provide defense in a suit or proceeding claiming infringement of a patent, copyright or trademark or for misappropriation of use of any trade secrets or for unfair competition.

COMPLIANCE WITH LAWS

Buyer agrees that at all times it will comply with all applicable federal, state, municipal, and local laws, orders and regulations. Buyer agrees to comply with all applicable restrictions on exports and re-exports including obtaining any required U.S. Government license, authorization, or approval. Buyer shall pay any duties, levies, taxes, brokerage fees, or customs fees imposed on the products.

TITLE AND DELIVERY

All shipments of goods shall be delivered ExWorks, Sunnyvale, CA, U.S.A. Title in the goods shall not pass to Buyer until ASIC Advantage, Inc. has received in full all amounts owed by Buyer.

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To access AAI's list of worldwide representatives , visit our web page http://www.in-plug.com/representatives.htm

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