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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	13 8	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	49	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	57	mJ	$I_D=5.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.29	mJ	$I_D=5.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	5.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	72	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current	I_S	-	-	13	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	49	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	1	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	55	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$.

³⁾ Identical low side and high side switch with identical R_G .

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.73	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at $T_j=25^{\circ}\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0\text{V}$, $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$, $I_D=0.29\text{mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=650$, $V_{GS}=0\text{V}$, $T_j=25^{\circ}\text{C}$ $V_{DS}=650$, $V_{GS}=0\text{V}$, $T_j=150^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.168 0.404	0.190 -	Ω	$V_{GS}=10\text{V}$, $I_D=5.7\text{A}$, $T_j=25^{\circ}\text{C}$ $V_{GS}=10\text{V}$, $I_D=5.7\text{A}$, $T_j=150^{\circ}\text{C}$
Gate resistance	R_G	-	1.1	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1150	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=400\text{V}$, $f=250\text{kHz}$
Output capacitance	C_{oss}	-	17	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=400\text{V}$, $f=250\text{kHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	34	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=0\ldots400\text{V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	374	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{V}$, $V_{DS}=0\ldots400\text{V}$
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=5.7\text{A}$, $R_G=10\Omega$; see table 9
Rise time	t_r	-	11	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=5.7\text{A}$, $R_G=10\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	54	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=5.7\text{A}$, $R_G=10\Omega$; see table 9
Fall time	t_f	-	9	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=5.7\text{A}$, $R_G=10\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	6	-	nC	$V_{DD}=400\text{V}$, $I_D=5.7\text{A}$, $V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	7	-	nC	$V_{DD}=400\text{V}$, $I_D=5.7\text{A}$, $V_{GS}=0$ to 10V
Gate charge total	Q_g	-	23	-	nC	$V_{DD}=400\text{V}$, $I_D=5.7\text{A}$, $V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=400\text{V}$, $I_D=5.7\text{A}$, $V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V$, $I_F=5.7A$, $T_J=25^{\circ}C$
Reverse recovery time	t_{rr}	-	830	-	ns	$V_R=400V$, $I_F=13A$, $di_F/dt=55A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	6.5	-	μC	$V_R=400V$, $I_F=13A$, $di_F/dt=55A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	18	-	A	$V_R=400V$, $I_F=13A$, $di_F/dt=55A/\mu s$; see table 8

4 Electrical characteristics diagrams

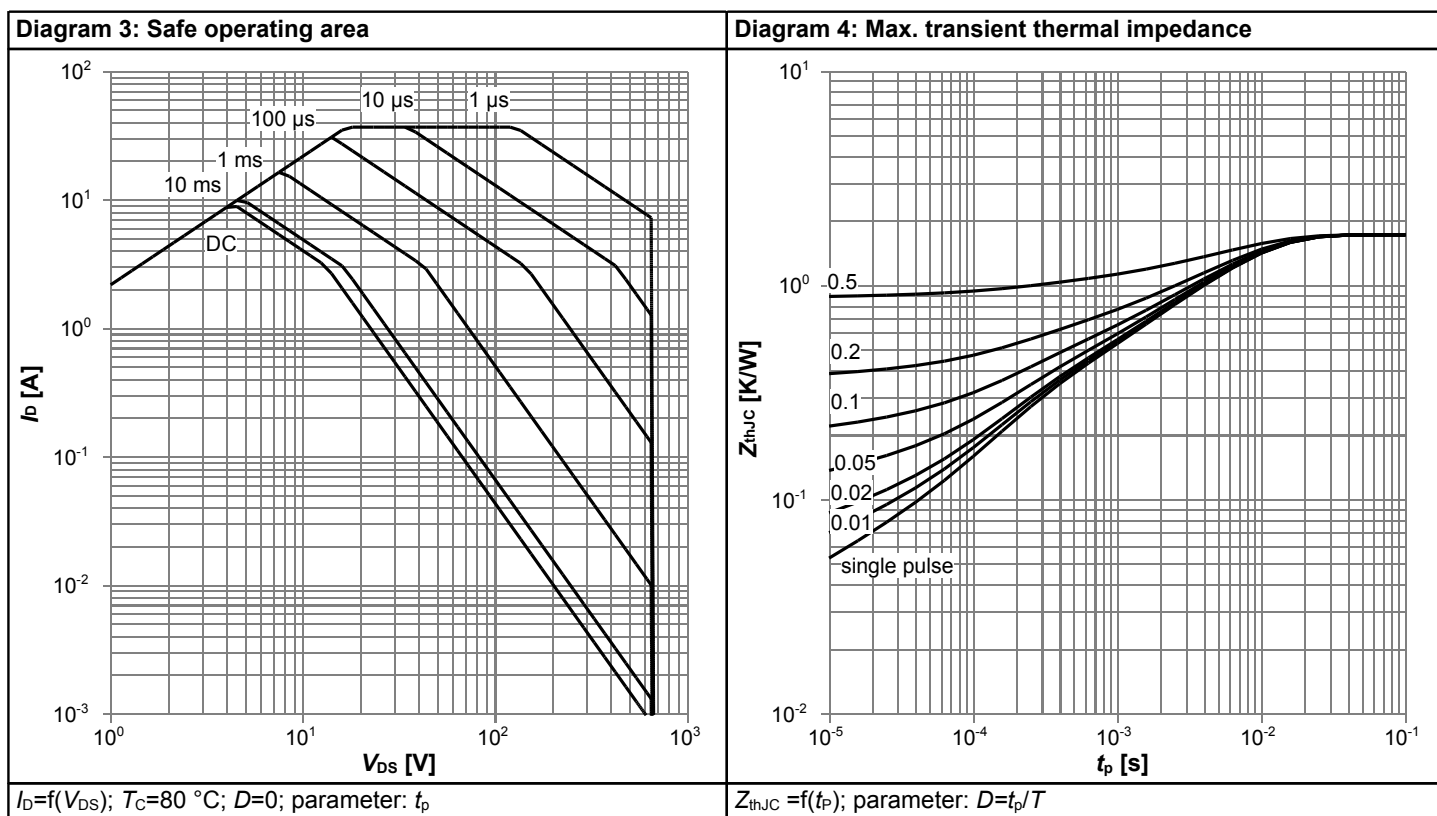
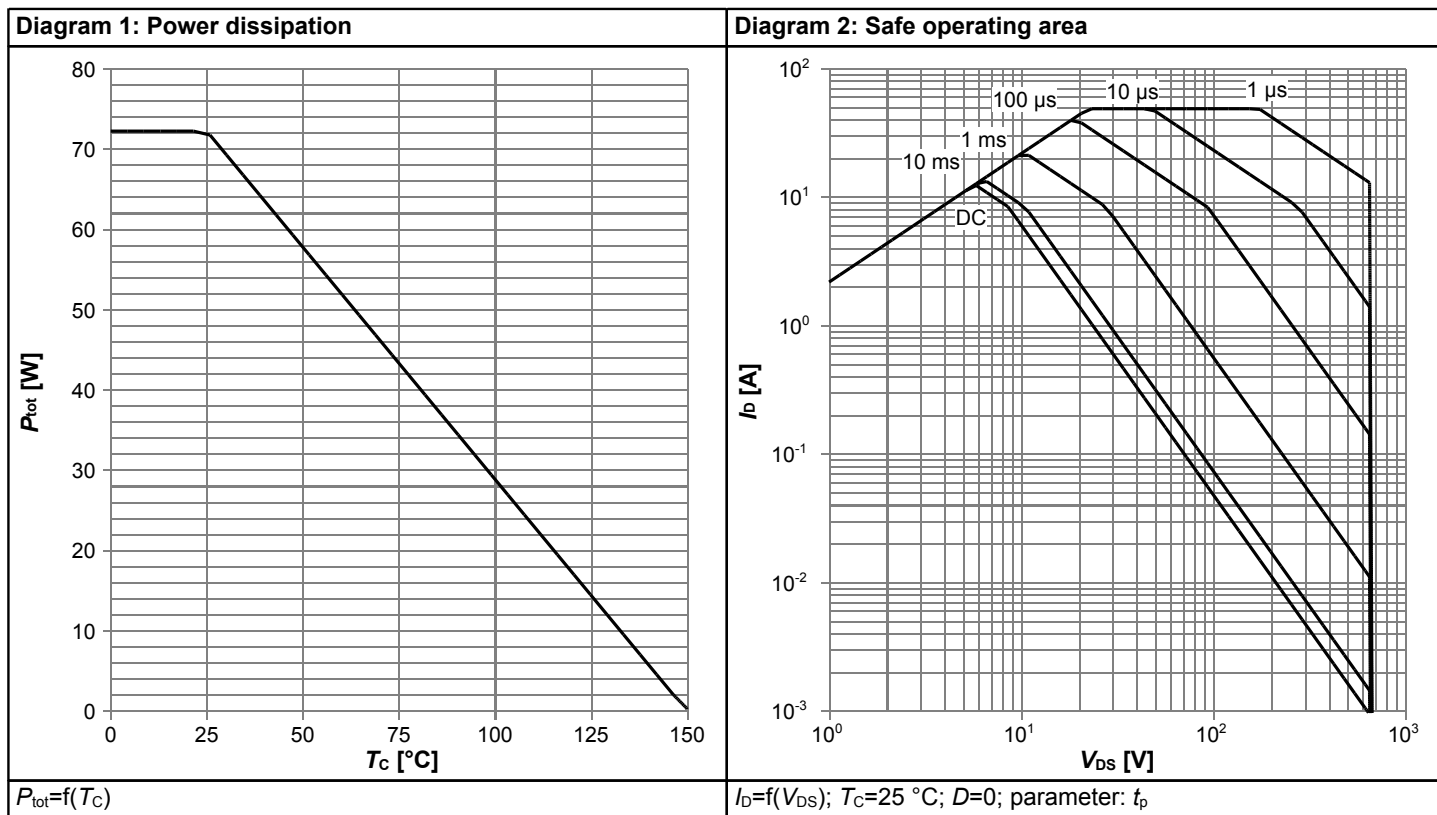
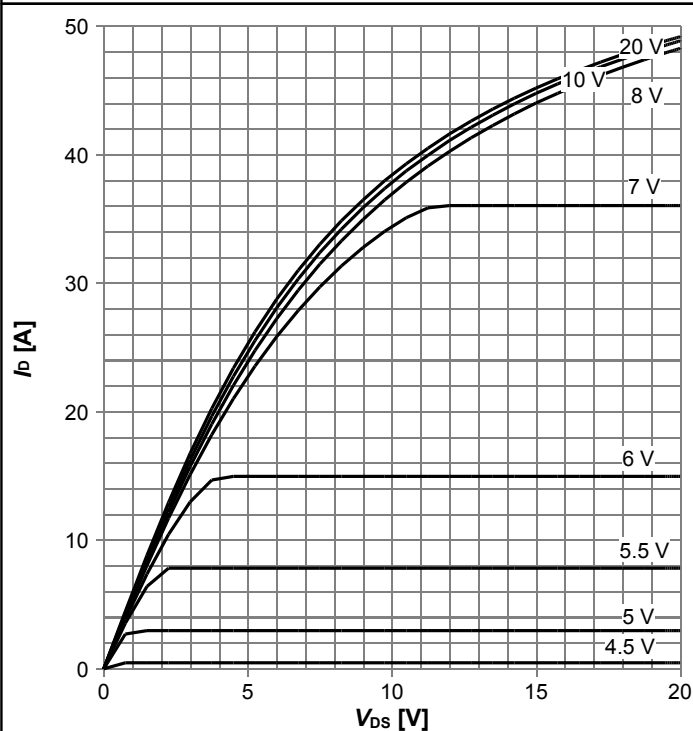
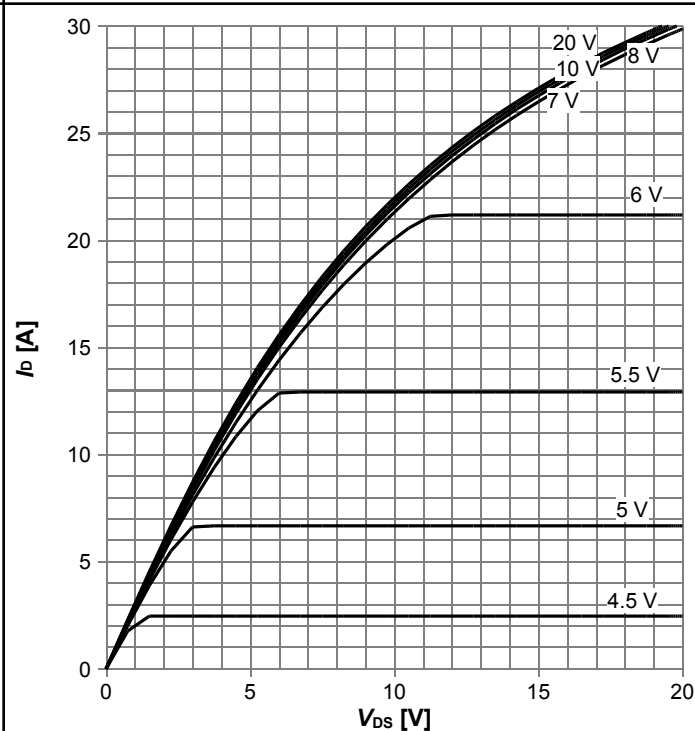


Diagram 5: Typ. output characteristics



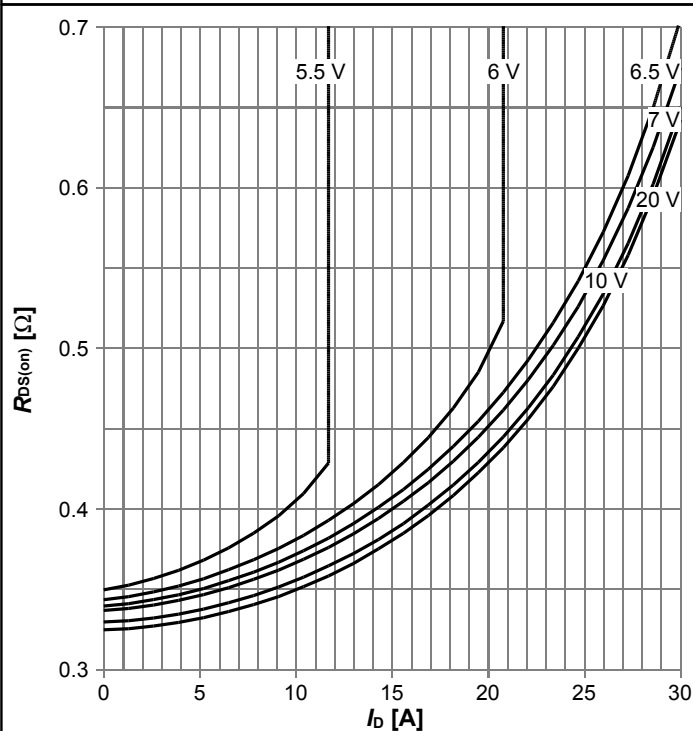
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



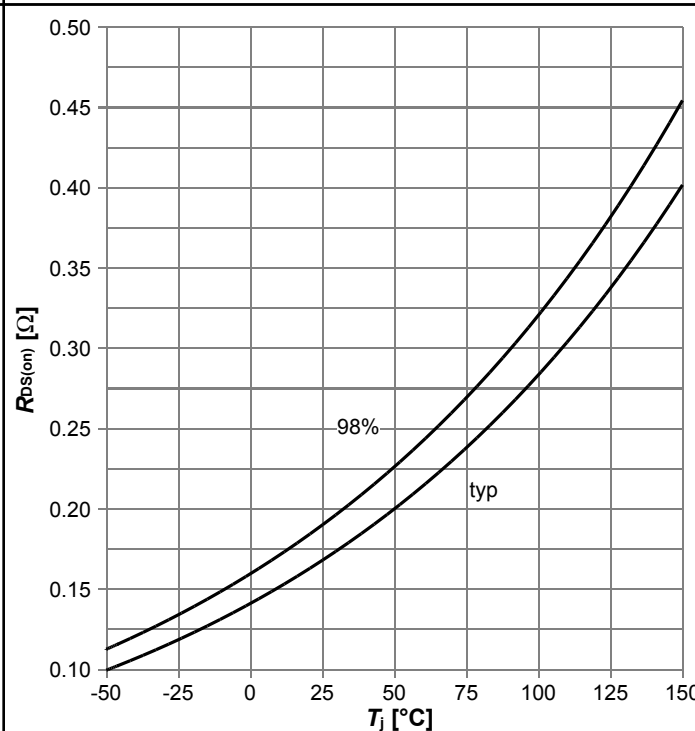
$I_D = f(V_{DS})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



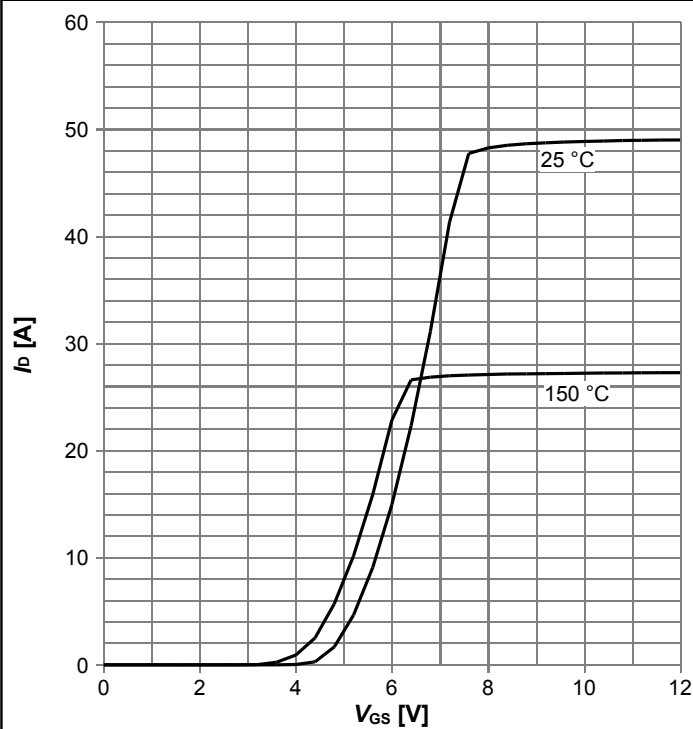
$R_{DS(on)} = f(I_D)$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



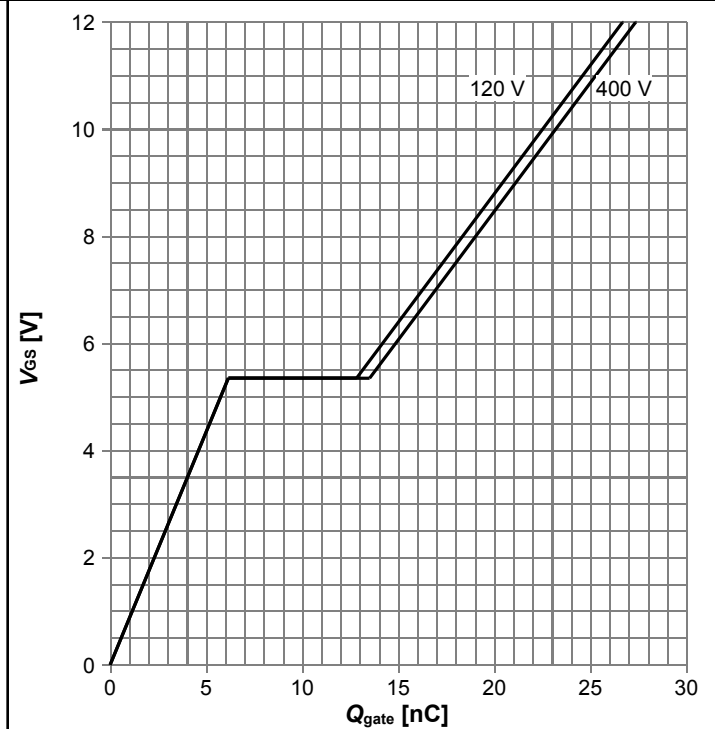
$R_{DS(on)} = f(T_j)$; $I_D = 5.7\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



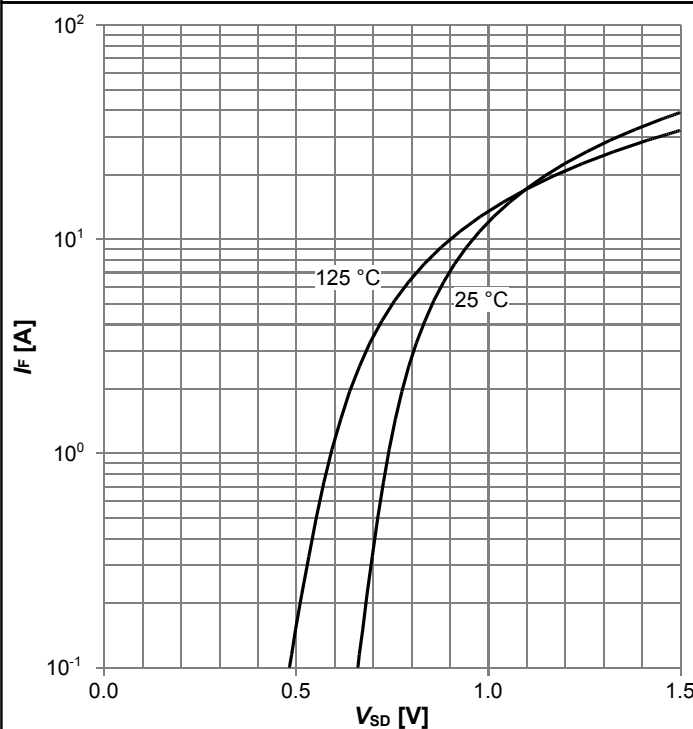
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



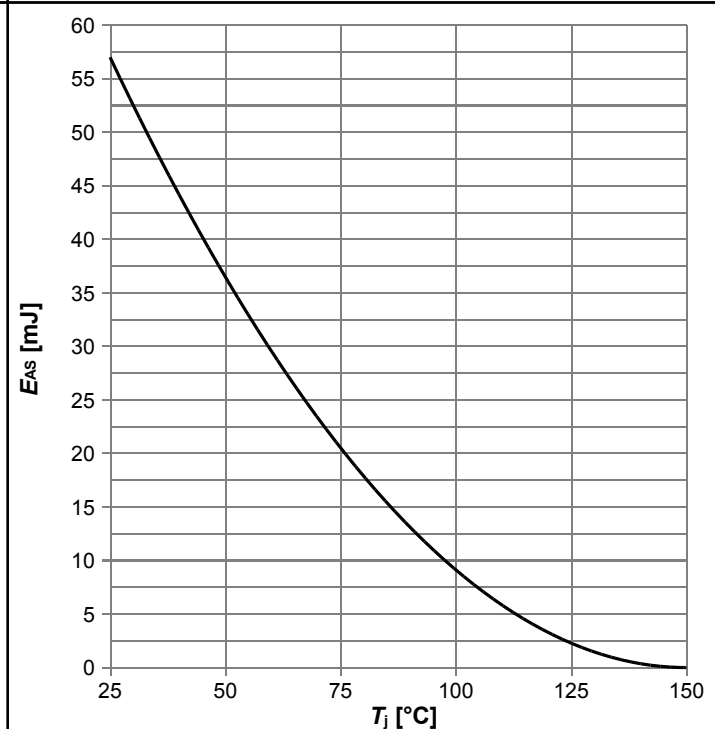
$V_{GS} = f(Q_{gate})$; $I_D = 5.7A$ pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



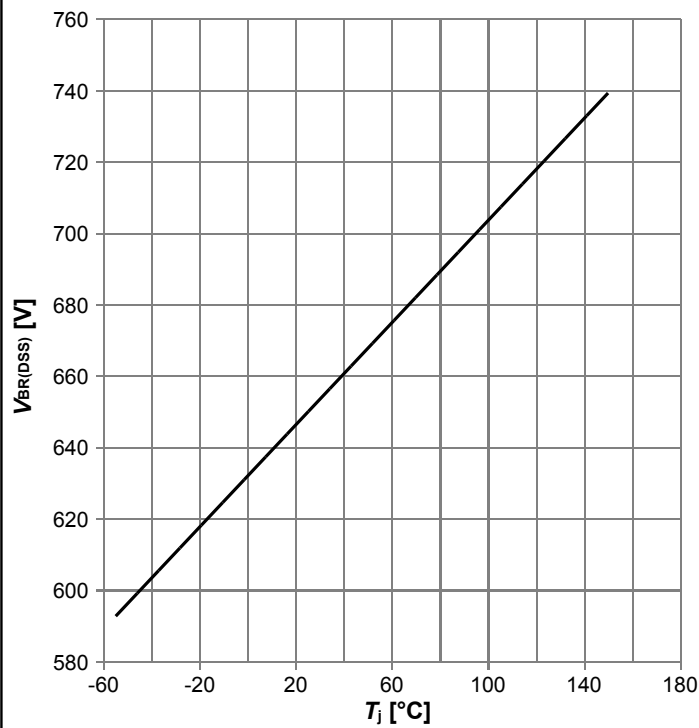
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



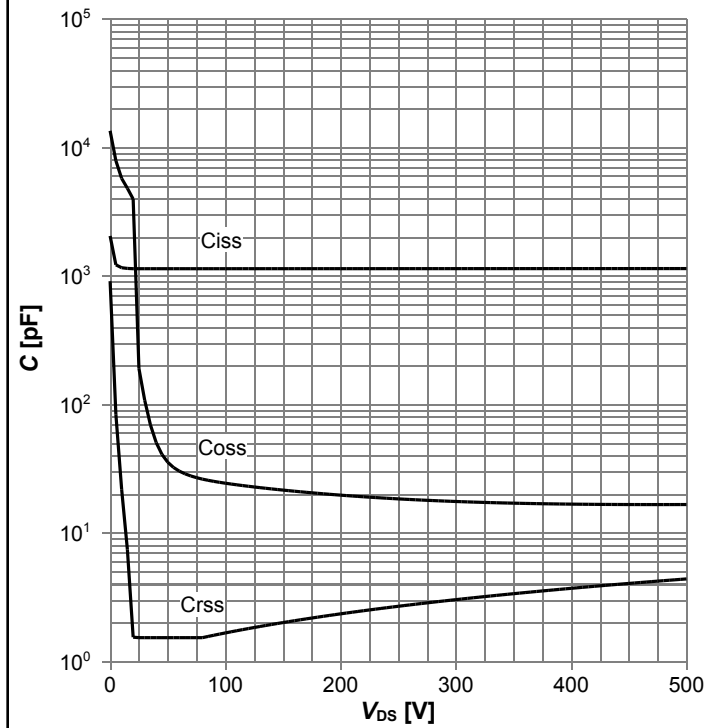
$E_{AS} = f(T_j)$; $I_D = 5.4 A$; $V_{DD} = 50 V$

Diagram 13: Drain-source breakdown voltage



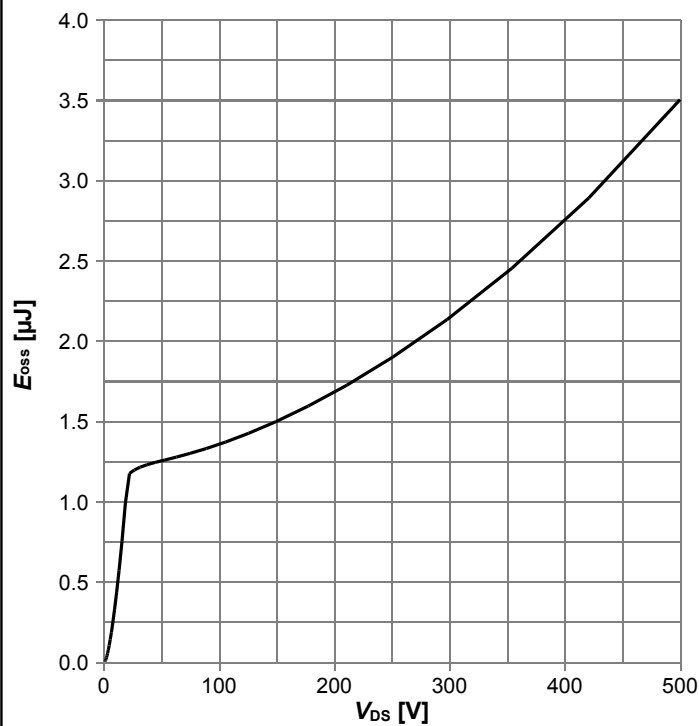
$V_{BR(DSS)} = f(T_J); I_D = 1 \text{ mA}$

Diagram 14: Typ. capacitances



$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss} = f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

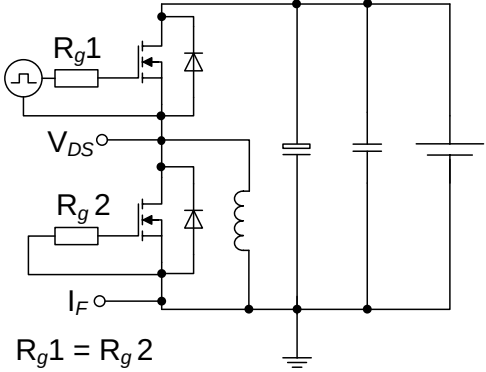
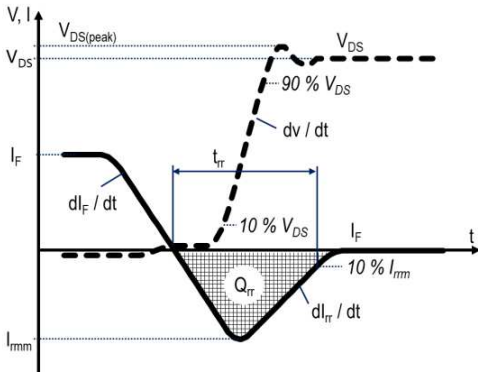
Test circuit for diode characteristics	Diode recovery waveform
 $R_{g1} = R_{g2}$	

Table 9 Switching times

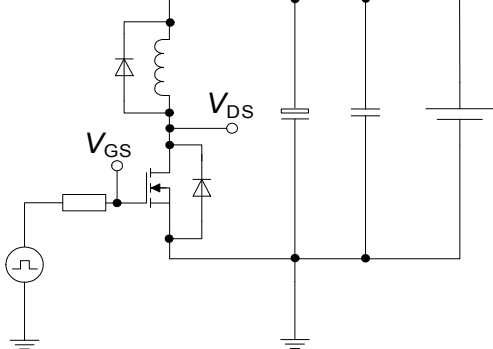
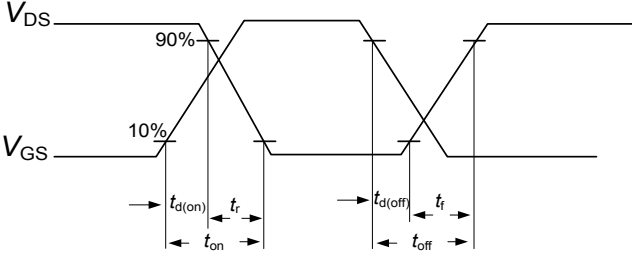
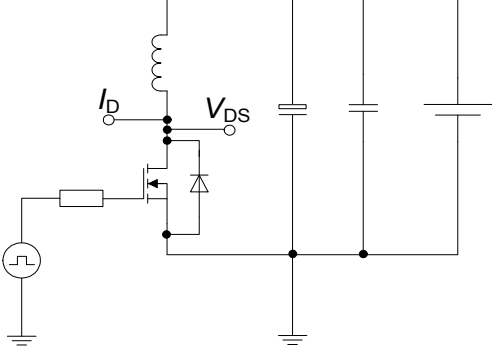
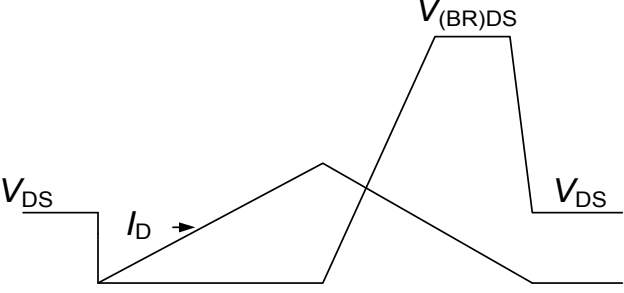
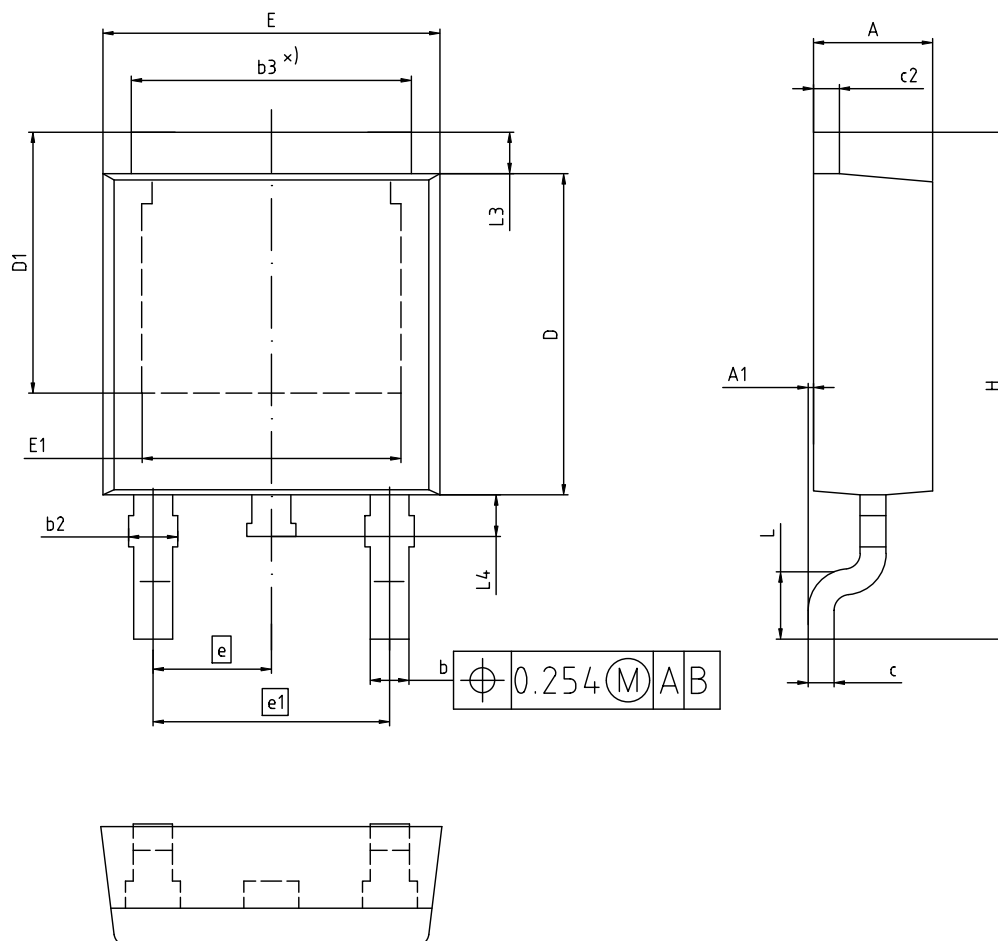
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines

PG-TO252-3 (DPAK)



ALL DIMENSIONS REFER TO JEDEC
STANDARD TO-252 AND DO NOT INCLUDE MOLD
FLASH OR PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b2	0.65	1.15
b3	4.95	5.50
c	0.46	0.61
c2	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L3	0.89	1.27
L4	0.51	1.02

DOCUMENT NO. Z8B00003328
REVISION 07
SCALE: 10:1 0 1 2mm
EUROPEAN PROJECTION
ISSUE DATE 01.04.2020

Figure 1 Outline PG-TO252-3, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ C7 Webpage: www.infineon.com
- IFX CoolMOS™ C7 application note: www.infineon.com
- IFX CoolMOS™ C7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPD65R190C7

Revision: 2020-05-26, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-10-10	Release of final version
2.1	2013-10-17	-
2.2	2020-05-26	Updated package/symbol drawing, and product validation

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