Electrical Specifications, (continued)

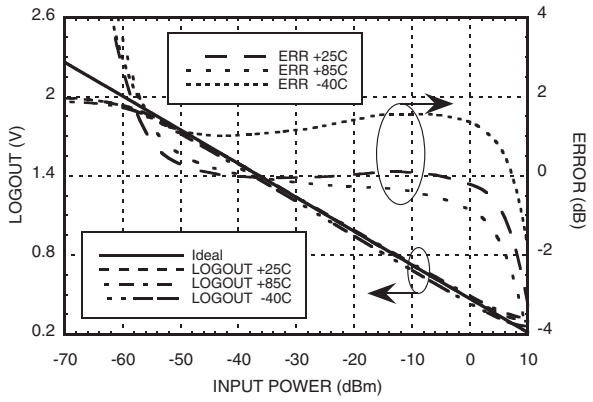
Parameter	Conditions	Min.	Typ.	Max.	Units
Open Loop Corner Frequency			700		kHz
Power Down (EN) Interface					
Voltage Range for Normal Mode		0.8 x Vcc [4]		Vcc [4]	V
Voltage Range for Powerdown Mode		0		0.2 x Vcc [4]	V
Threshold Voltage			Vcc [4]/2		V
Power Supply (Vcc1, Vcc2, Vcc3)					
Operating Voltage Range		4.5		5.5	V
Supply Current in Normal Mode			113		mA
Supply Current in Power Down Mode			1		mA

[4] Vcc= Vcc1= Vcc2= Vcc3= +5V

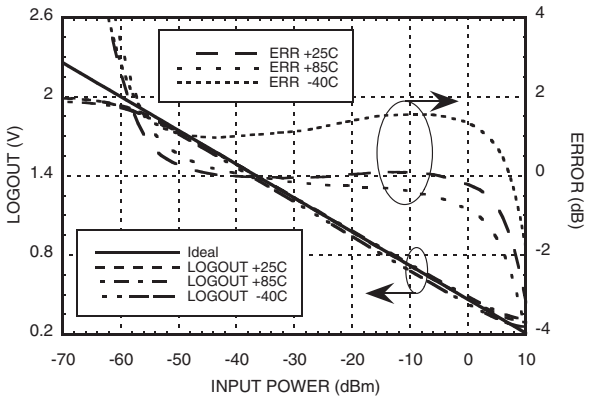
Test Conditions

Parameter	Condition
Vcc1, Vcc2, Vcc3	+5V
Input Zo	50Ω
T_A	+25C
Fin	900 MHz

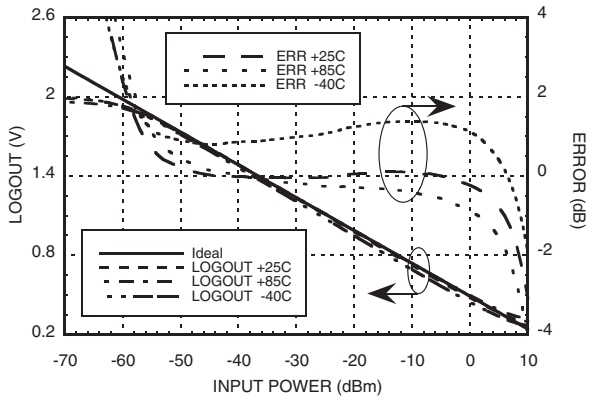
LOGOUT Voltage & Error vs. Input Power, Fin = 50 MHz



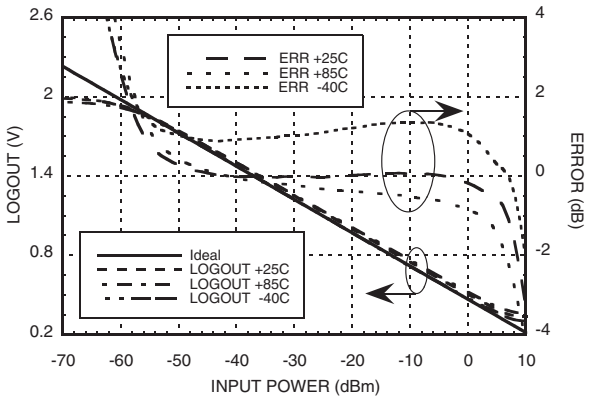
LOGOUT Voltage & Error vs. Input Power, Fin = 100 MHz



LOGOUT Voltage & Error vs. Input Power, Fin = 900 MHz



LOGOUT Voltage & Error vs. Input Power, Fin = 1900 MHz



Unless otherwise noted: Vcc1, Vcc2, Vcc3 = +5V, T_A = +25C

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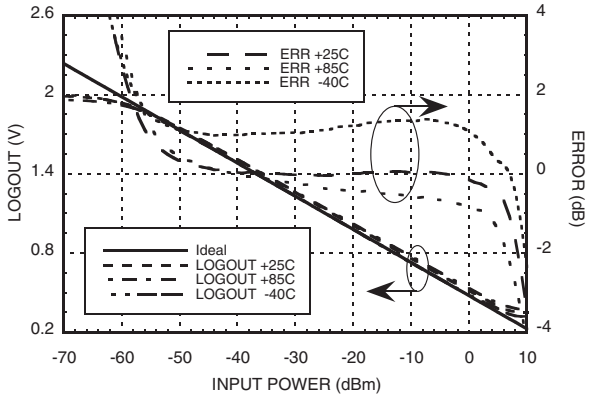
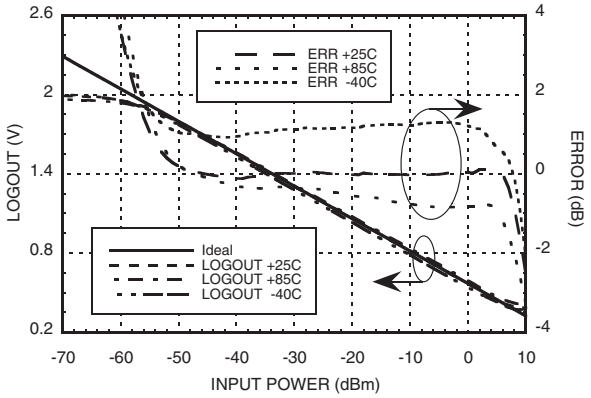
70 dB, LOGARITHMIC DETECTOR / CONTROLLER, 1 - 8000 MHz

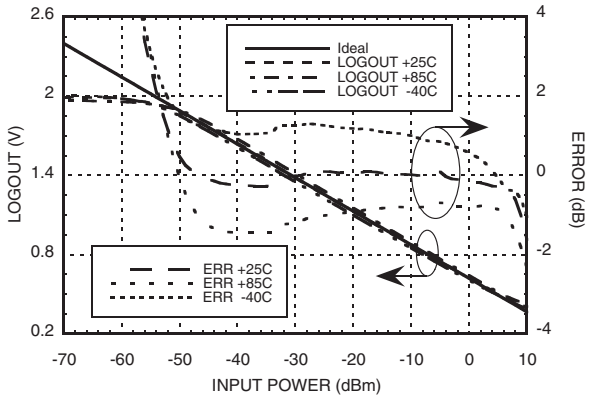
LOGOUT Voltage & Error vs. Input Power, Fin = 2200 MHz



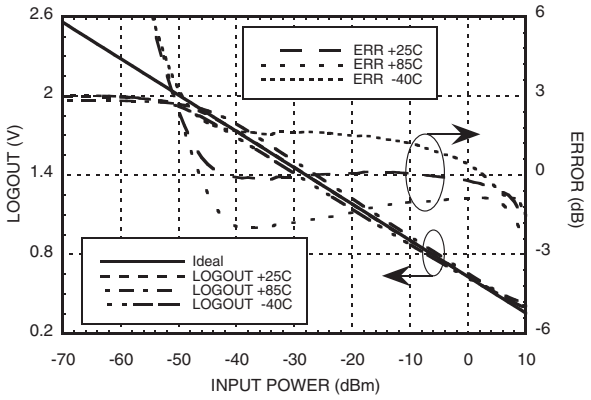
LOGOUT Voltage & Error vs. Input Power, Fin = 3600 MHz



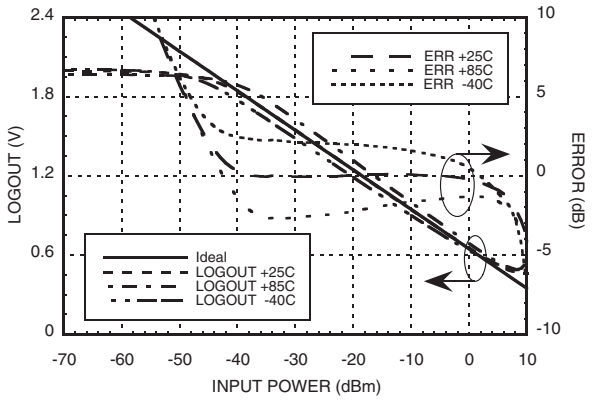
LOGOUT Voltage & Error vs. Input Power, Fin = 5800 MHz



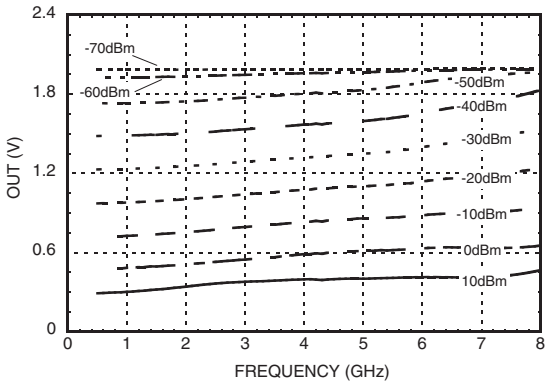
LOGOUT Voltage & Error vs. Input Power, Fin = 7000 MHz



LOGOUT Voltage & Error vs. Input Power, Fin = 8000 MHz



LOGOUT vs. Frequency Over Input Power



Unless otherwise noted: Vcc1, Vcc2, Vcc3 = +5V, T_A = +25C

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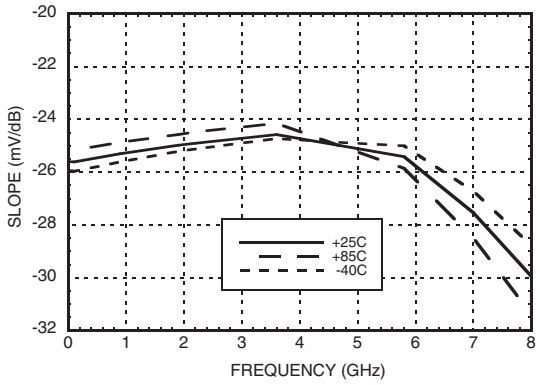
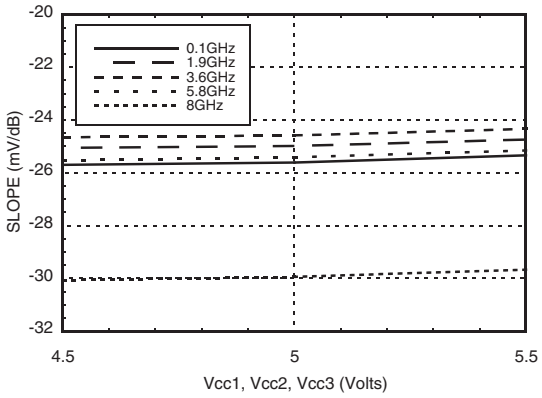
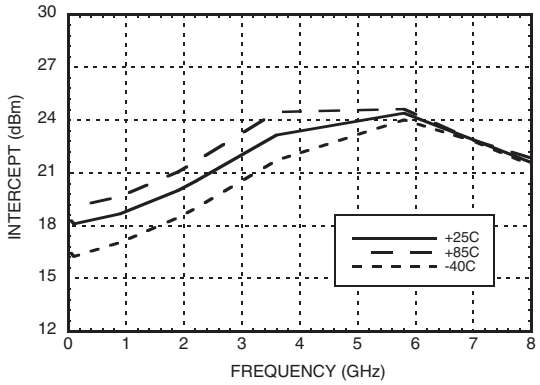
LOGOUT Slope vs. Frequency



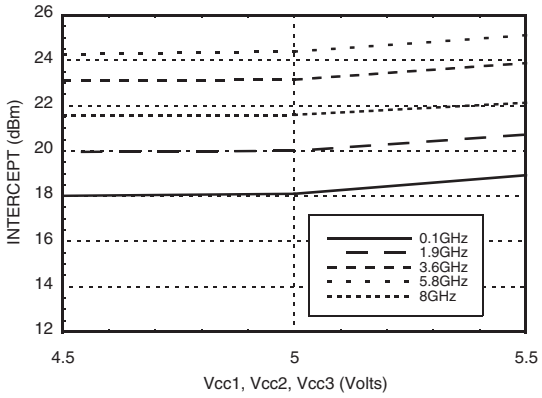
LOGOUT Slope vs. Supply Voltage



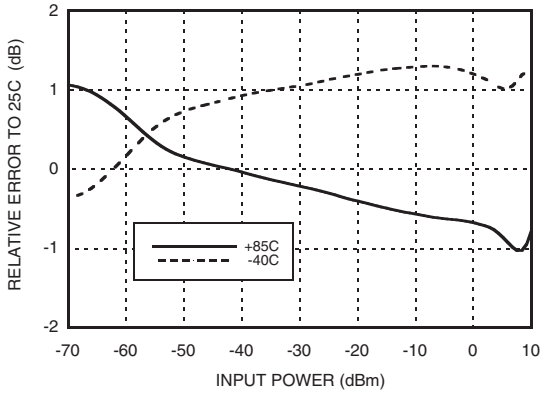
LOGOUT Intercept vs. Frequency



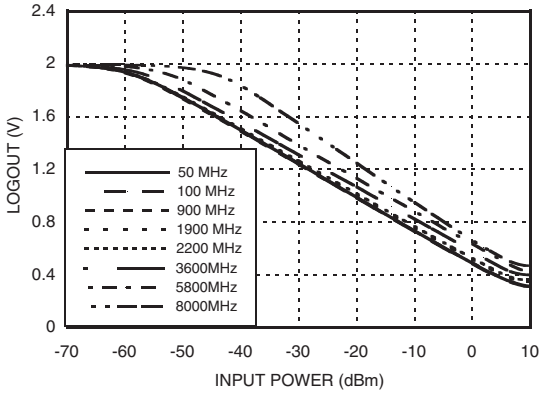
LOGOUT Intercept vs. Supply Voltage



LOGOUT Error vs. Input Power, Normalized [2], Fin= 1900 MHz



LOGOUT Voltage vs. Input Power & Frequency



[1] Unless otherwise noted: Vcc1, Vcc2, Vcc3 = +5V, T_A = +25C

[2] This data is relative to the room temperature performance of the HMC602LP4(E)

[3] Reference plane at J1 connector on Evaluation PCB

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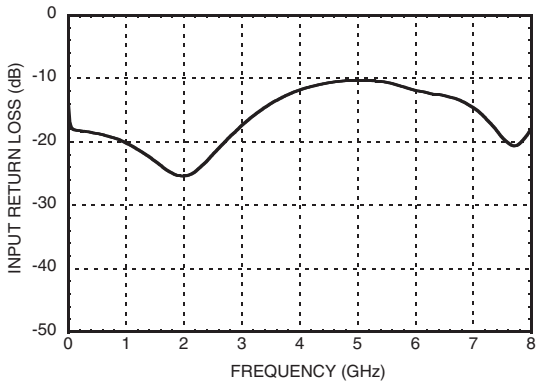
Input Return Loss vs Frequency [4]



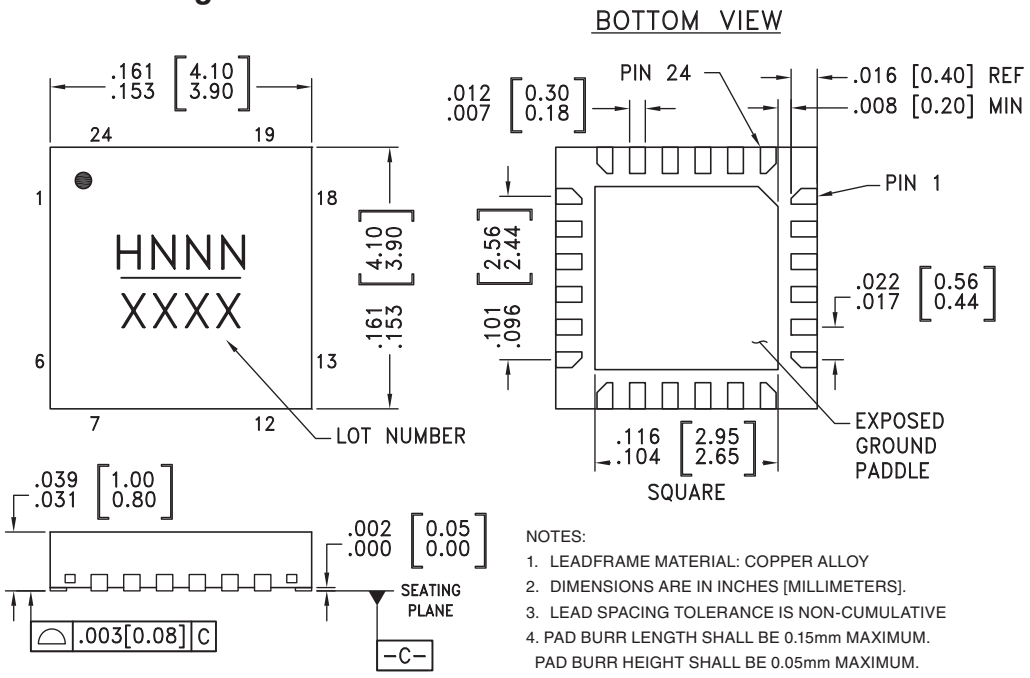
Absolute Maximum Ratings

Vcc1, Vcc2, Vcc3	+5.5V
EN	+5.5V
VSET Input Voltage	+5.5V
LOGOUT Output Current	3 mA
RF Input Power	+15 dBm
Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 7.95 mW/°C above 85°C)	1.55 Watts
Thermal Resistance (R_{th}) (junction to lead)	42 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

[4] Reference plane at J1 connector on Evaluation PCB

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC602LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H602 XXXX
HMC602LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H602 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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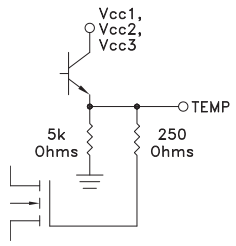
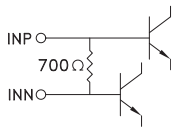
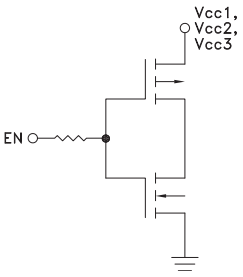
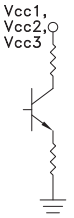
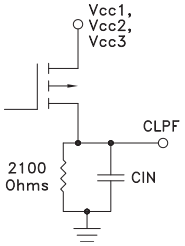
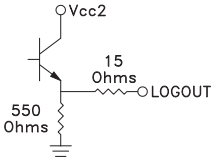
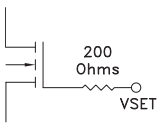
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 6, 7, 13, 17, 18	N/C	These pins are not connected internally.	
2	TEMP	Temperature sensor output pin.	
3, 4	INP, INN	RF Input pins. Connect RF to INP, and AC couple INN to ground for single-ended operation.	
5	EN	Enable pin, connect to Vcc1, Vcc2, Vcc3 for normal operation. Applying voltage <0.2 x (Vcc1, Vcc2, Vcc3) will initiate power saving mode.	
8 - 12, 19, 20, 23, 24	Vcc1, Vcc2, Vcc3	Bias supply. Connect supply voltage to these pins with appropriate filtering.	
14	CLPF	Loop filter capacitor for output ripple filtering.	
15	LOGOUT	Logarithmic output that converts the input power to a DC level in detector mode. Short this pin to VSET for detector mode.	
16	VSET	VSET input in controller mode. Short this pin to LOGOUT for detector mode.	

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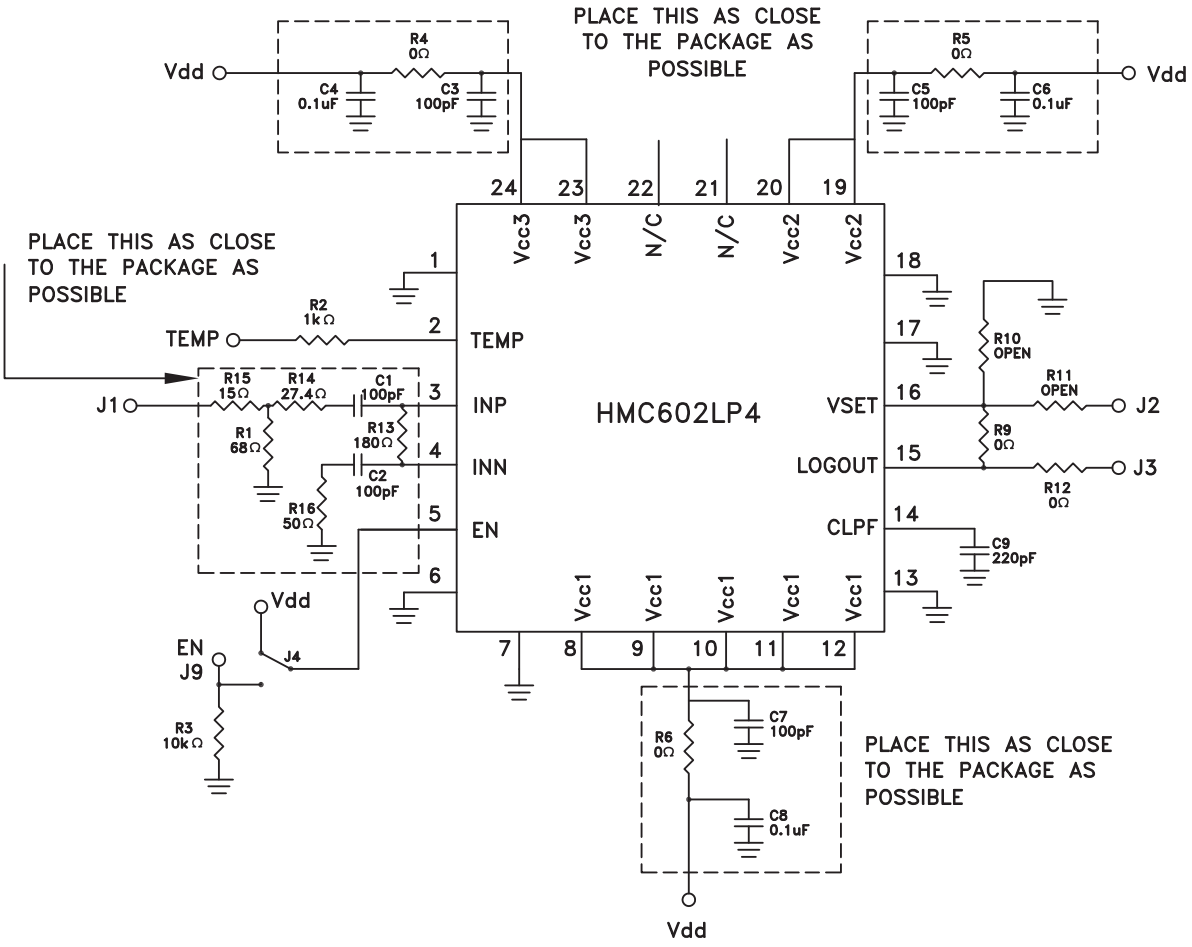
Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
21, 22	N/C	The user should not connect to these pins.	
Package Base	GND	Exposed paddle must be connected to RF and DC ground.	

Application & Evaluation PCB Schematic



Notes

Note 1: The HMC602LP4 & HMC602LP4E evaluation boards are pre-assembled for single-ended input, and detector/RSSI mode.

Note 2: For detector mode, connect high impedance volt meter to the LOGOUT port, and make no connection to VSET. LOGOUT is shorted to VSET by R9, as required for detector mode.

Note 3: For controller mode, remove R9 and install 0 ohm resistor (R11), then make appropriate connection to LOGOUT and VSET. In controller mode, the LOGOUT output can be used to drive a variable gain amplifier, or a variable attenuator, either directly or through a buffer or microcontroller. VSET should be connected to an external supply, typically between +0.6 and +1.9V.

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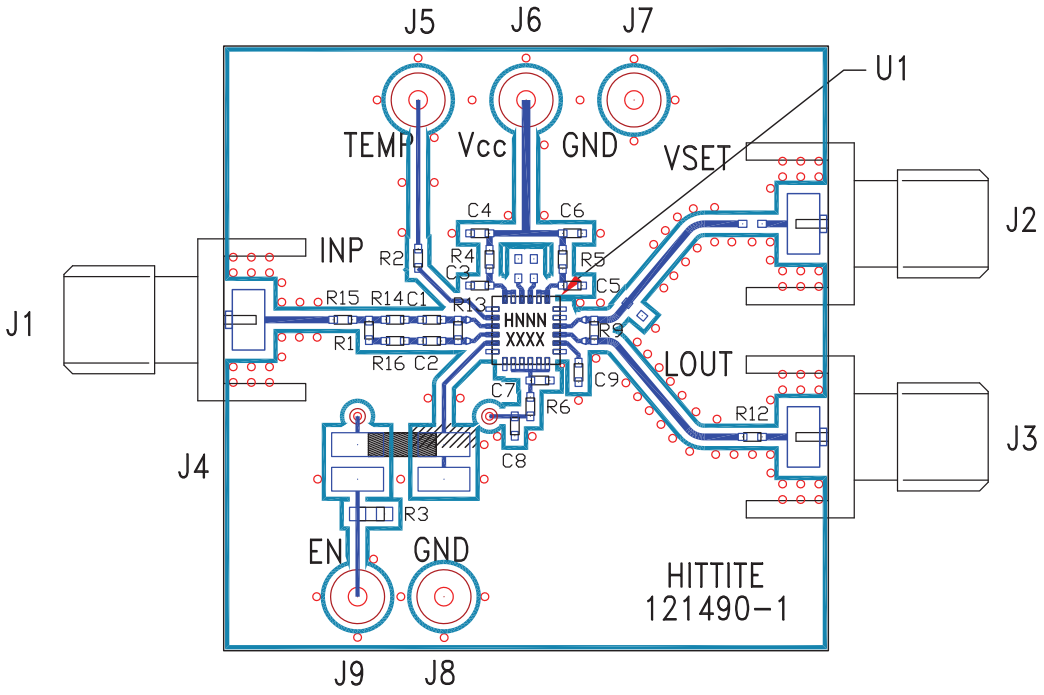
Evaluation PCB



List of Materials for Evaluation PCB 121492 [1]

Item	Description
J1 - J3	PC Mount SMA Connector
J4	Molex Connector Header
J5 - J9	DC Pin
C1, C2, C3, C5, C7	100 pF Capacitor, 0402 Pkg.
C4, C6, C8	0.1µF Capacitor, 0402 Pkg.
C9	220 pF Capacitor, 0402 Pkg.
R1	68Ω Resistor, 0402 Pkg.
R2	1k Ω Resistor, 0402 Pkg.
R3	10k Ω Resistor, 0402 Pkg.
R4 - R6, R9, R12	0Ω Resistor, 0402 Pkg.
R13	180Ω Resistor, 0402 Pkg.
R14	27.4Ω Resistor, 0402 Pkg.
R15	15Ω Resistor, 0402 Pkg.
R16	49.9Ω Resistor, 0402 Pkg.
U1	HMC602LP4 / HMC602LP4E Logarithmic Detector / Controller
PCB [2]	121490 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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