ON Semiconductor®

# FQD5P10

## P-Channel QFET® MOSFET

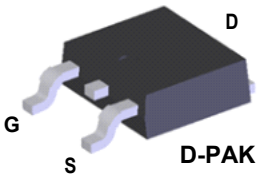
**-100 V, -3.6 A, 1.05Ω**

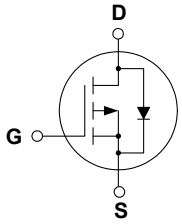
### Description

This P-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### Features

- -3.6 A, -100 V, $R_{DS(on)}$ = 1.05 Ω (Max.) @ $V_{GS}$ = -10 V, $I_D$ = 1.8 A
- Low Gate Charge (Typ. 6.3 nC)
- Low Crss (Typ. 18 pF)
- 100% avalanche tested




## Absolute Maximum Ratings

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | | FQD5P10 | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | -100 | V |
| $I_D$ | Drain Current | - Continuous ($T_C$ = 25°C) | -3.6 | A |
| | | - Continuous ($T_C$ = 100°C) | -2.28 | A |
| $I_{DM}$ | Drain Current | - Pulsed (Note 1) | -14.4 | A |
| $V_{GSS}$ | Gate-Source Voltage | | ± 30 | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 55 | mJ |
| $I_{AR}$ | Avalanche Current | (Note 1) | -3.6 | A |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 2.5 | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | -6.0 | V/ns |
| $P_D$ | Power Dissipation ($T_A$ = 25°C) * | | 2.5 | W |
| | Power Dissipation ($T_C$ = 25°C) | | 25 | W |
| | - Derate above 25°C | | 0.2 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | °C |
| $T_L$ | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | | 300 | °C |

## Thermal Characteristics

| Symbol | Parameter | FQD5P10 | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case, Max. | 5.0 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient * | 50 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient, Max. | 110 | °C/W |

* When mounted on the minimum pad size recommended (PCB Mount)


October-2017,Rev.3

Publication Order Number:
FQD5P10/D

## Electrical Characteristics

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = -250 μA | -100 | -- | -- | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = -250 μA, Referenced to 25°C | -- | -0.1 | -- | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = -100 V, $V_{GS}$ = 0 V | -- | -- | -1 | μA |
| | | $V_{DS}$ = -80 V, $T_C$ = 125°C | -- | -- | -10 | μA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = -30 V, $V_{DS}$ = 0 V | -- | -- | -100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = 30 V, $V_{DS}$ = 0 V | -- | -- | 100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = -250 μA | -2.0 | -- | -4.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = -10 V, $I_D$ = -1.8 A | -- | 0.82 | 1.05 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = -40 V, $I_D$ = -1.8 A | -- | 2.3 | -- | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = -25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | -- | 190 | 250 | pF |
| $C_{oss}$ | Output Capacitance | | -- | 70 | 90 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 18 | 25 | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = -50 V, $I_D$ = -4.5 A, $R_G$ = 25 Ω (Note 4) | -- | 9 | 30 | ns |
| $t_r$ | Turn-On Rise Time | | -- | 70 | 150 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 12 | 35 | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 30 | 70 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = -80 V, $I_D$ = -4.5 A, $V_{GS}$ = -10 V (Note 4) | -- | 6.3 | 8.2 | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 1.7 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 3.0 | -- | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | -3.6 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | -14.4 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = -3.6 A | -- | -- | -4.0 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_S$ = -4.5 A, $dI_F$ / dt = 100 A/μs | -- | 85 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 0.27 | -- | μC |

**Notes:**
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 6.4mH, $I_{AS}$ = -3.6A, $V_{DD}$ = -25V, $R_G$ = 25 Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ -4.5A, di/dt ≤ 300A/μs, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C
4. Essentially independent of operating temperature

## Typical Characteristics

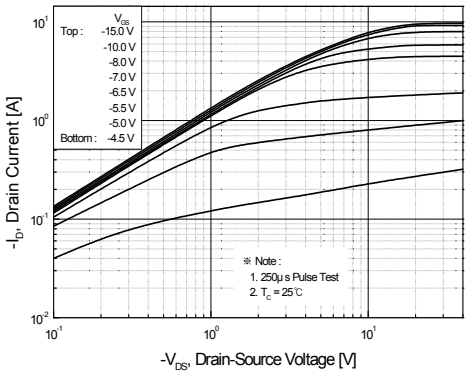



**Figure 1. On-Region Characteristics**

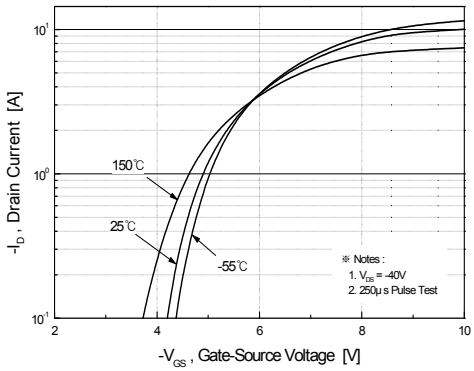



**Figure 2. Transfer Characteristics**

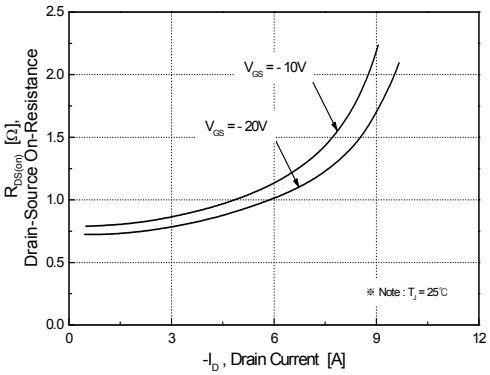



**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

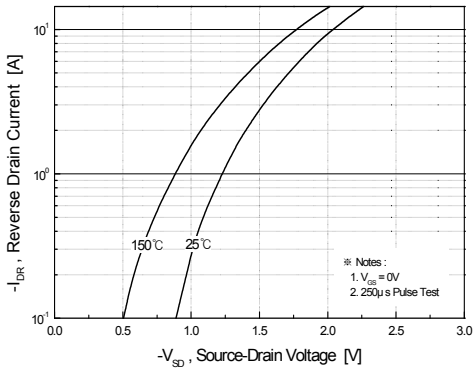



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

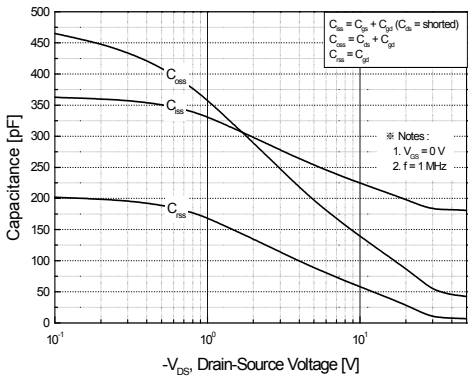



**Figure 5. Capacitance Characteristics**

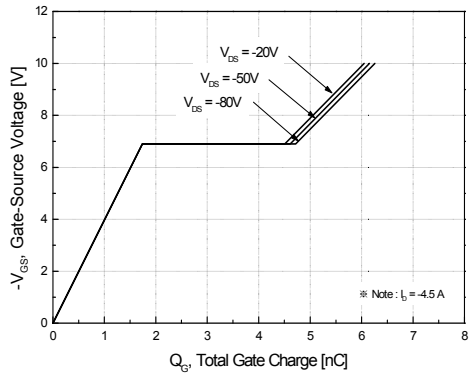



**Figure 6. Gate Charge Characteristics**

## Typical Characteristics (Continued)

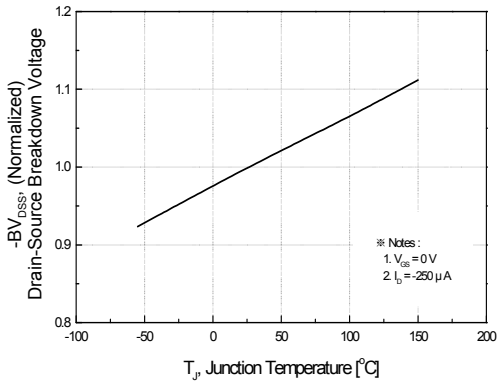



**Figure 7. Breakdown Voltage Variation vs. Temperature**

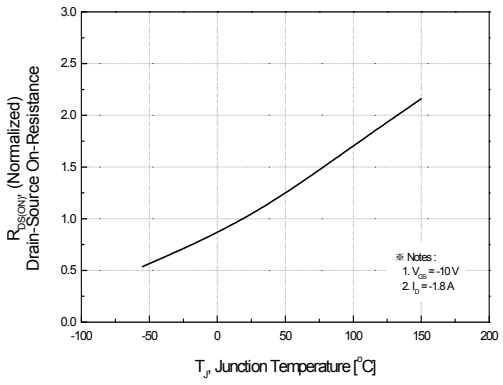



**Figure 8. On-Resistance Variation vs. Temperature**

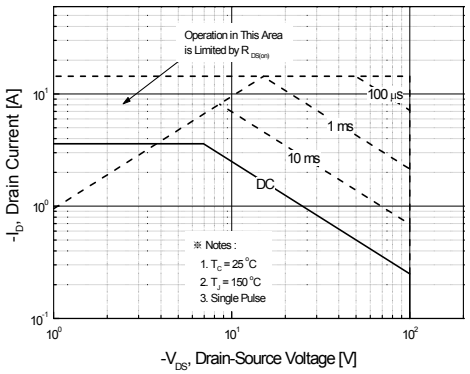



**Figure 9. Maximum Safe Operating Area**

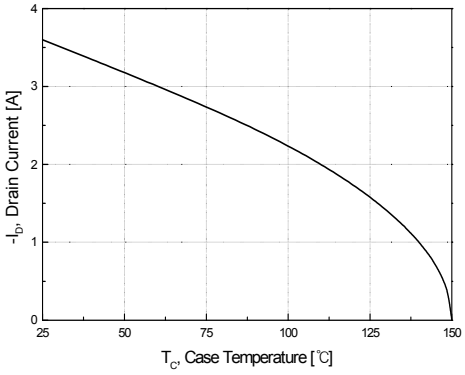



**Figure 10. Maximum Drain Current vs. Case Temperature**

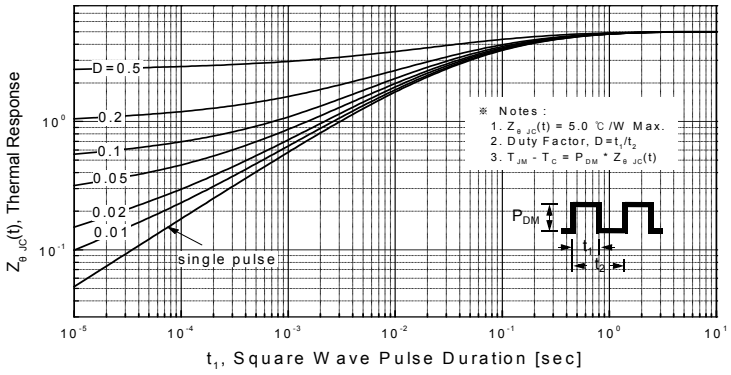
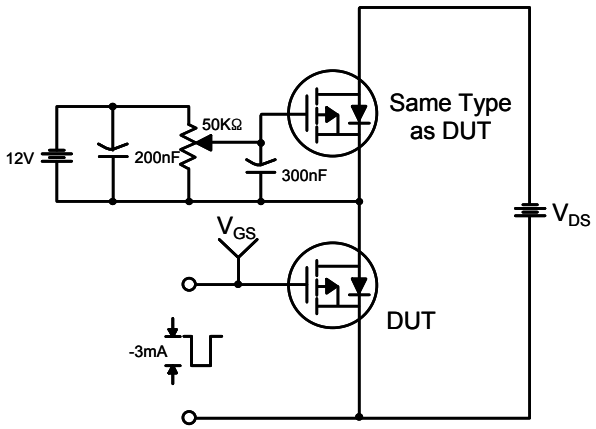
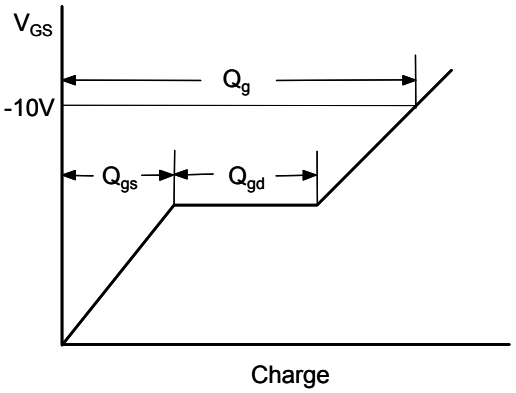


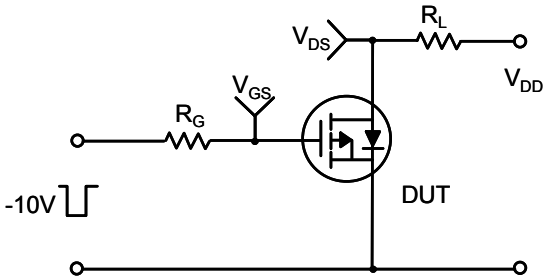

**Figure 11. Transient Thermal Response Curve**

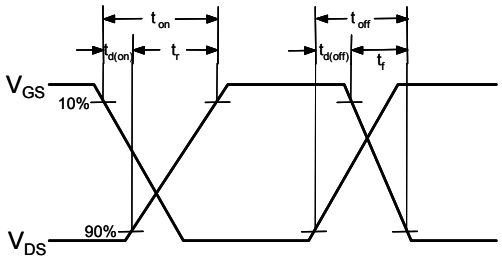
### Gate Charge Test Circuit & Waveform



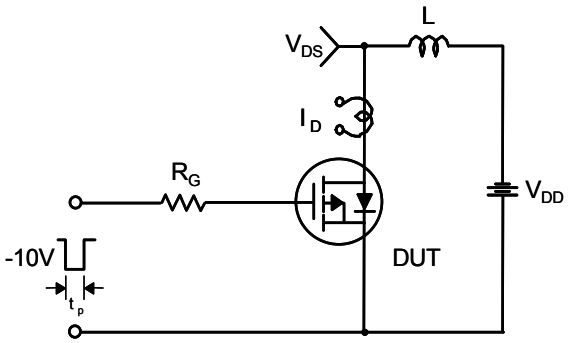




### Resistive Switching Test Circuit & Waveforms

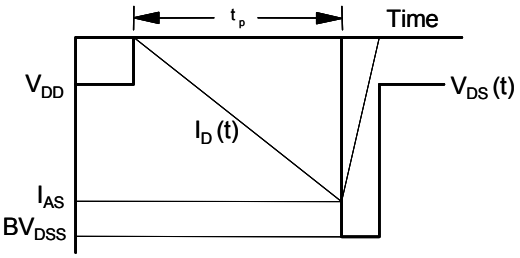


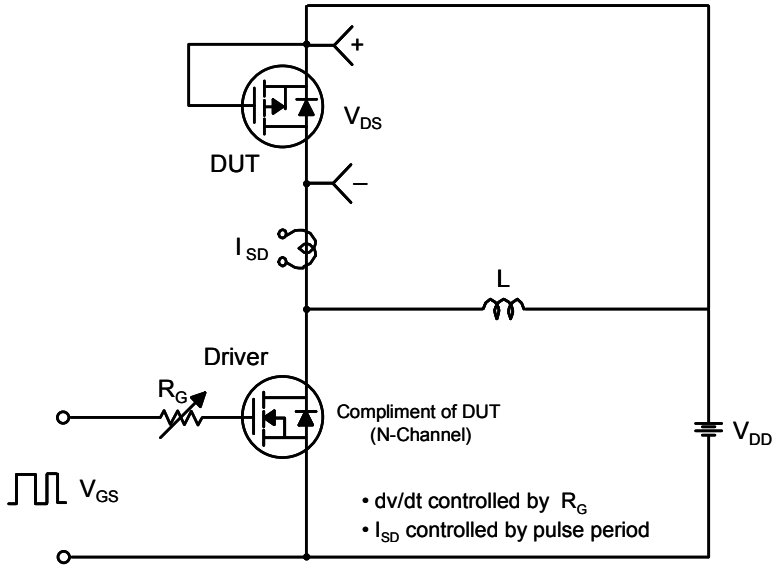

### Unclamped Inductive Switching Test Circuit & Waveforms

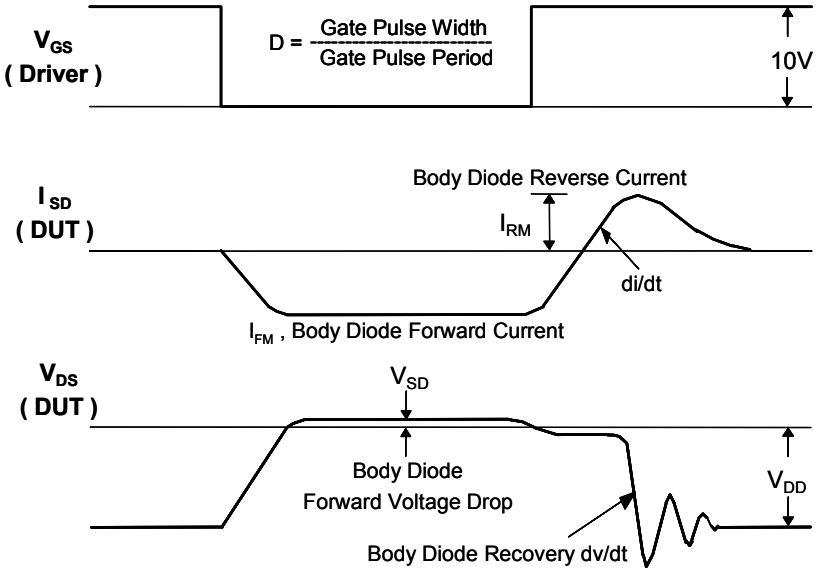



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



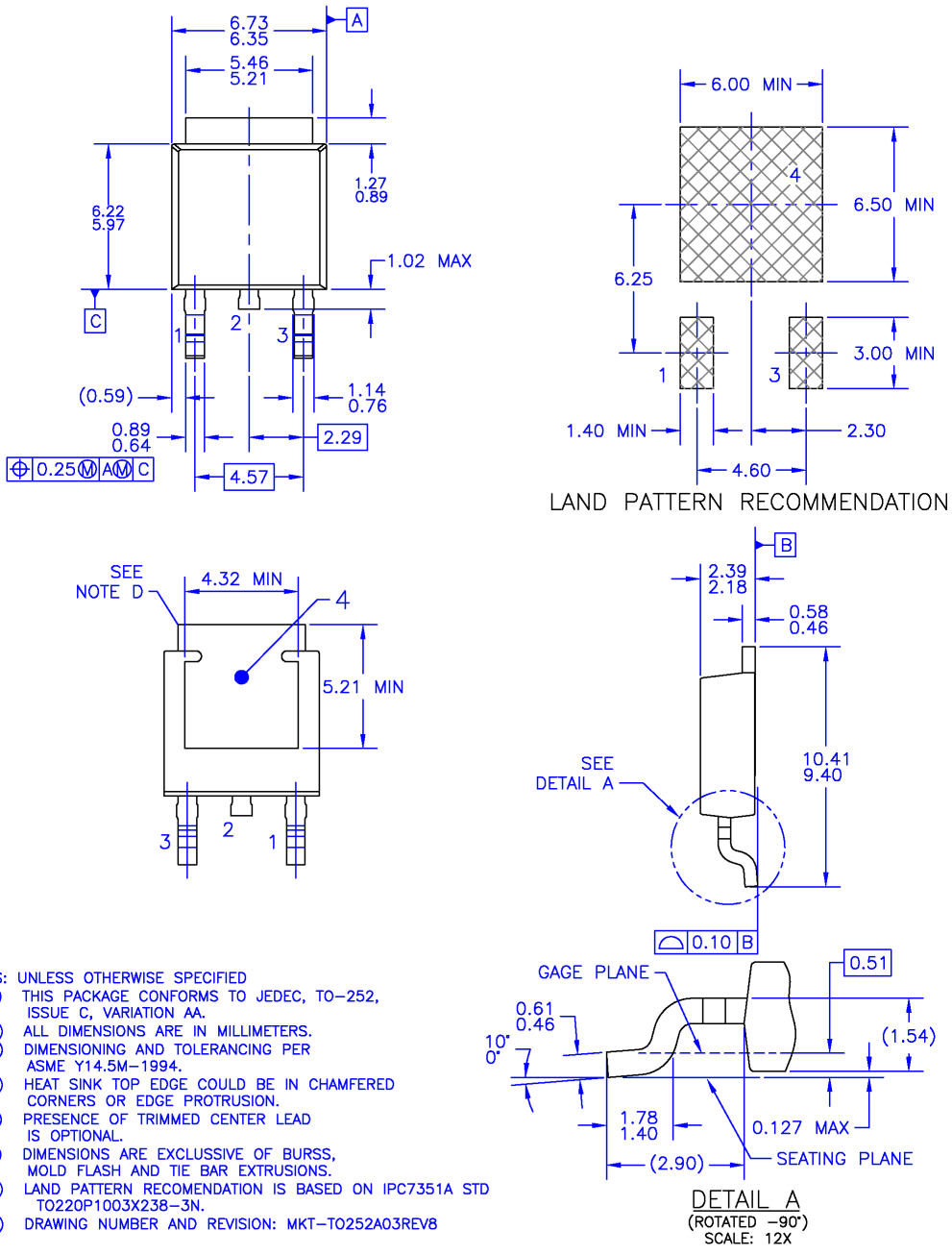
**Peak Diode Recovery dv/dt Test Circuit & Waveforms**



## Package Dimensions

# D-PAK




NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO−252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238−3N.
H) DRAWING NUMBER AND REVISION: MKT−TO252A03REV8

Dimensions in Millimeters

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