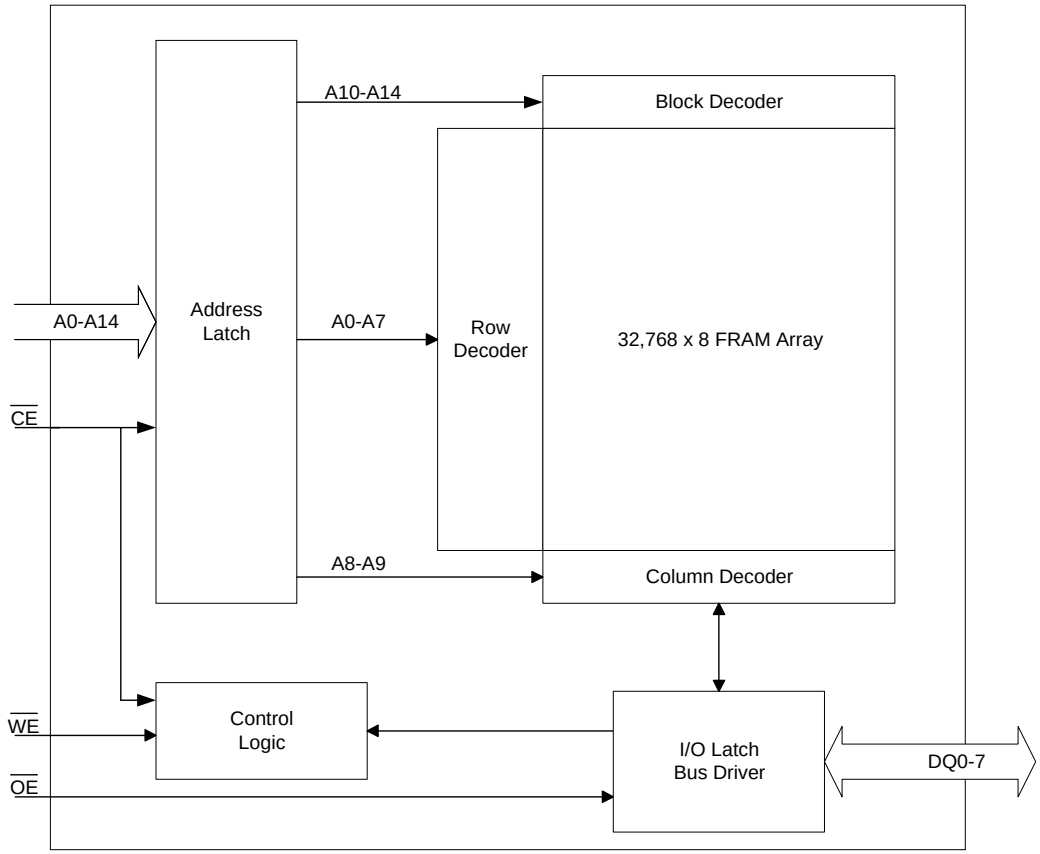


Figure 1. Block Diagram

Pin Description

Pin Name	Type	Description
A0-A14	Input	Address: The 15 address lines select one of 32,768 bytes in the FRAM array. The address value is latched on the falling edge of /CE.
DQ0-7	I/O	Data: 8-bit bi-directional data bus for accessing the FRAM array.
/CE	Input	Chip Enable: /CE selects the device when low. Asserting /CE low causes the address to be latched internally. Address changes that occur after /CE goes low will be ignored until the next falling edge occurs.
/OE	Input	Output Enable: Asserting /OE low causes the FM1808 to drive the data bus when valid data is available. Deasserting /OE high causes the DQ pins to be tri-stated.
/WE	Input	Write Enable: Asserting /WE low causes the FM1808 to write the contents of the data bus to the address location latched by the falling edge of /CE.
VDD	Supply	Supply Voltage: 5V
VSS	Supply	Ground

Functional Truth Table

/CE	/WE	Function
H	X	Standby/Precharge
↓	X	Latch Address (and Begin Write if /WE=low)
L	H	Read
L	↓	Write

Note: The /OE pin controls only the DQ output buffers.

Overview

The FM1808 is a bytewide FRAM memory. The memory array is logically organized as 32,768 x 8 and is accessed using an industry standard parallel interface. All data written to the part is immediately nonvolatile with no delay. Functional operation of the FRAM memory is the same as SRAM type devices, except the FM1808 requires a falling edge of /CE to start each memory cycle.

Memory Architecture

Users access 32,768 memory locations each with 8 data bits through a parallel interface. The complete 15-bit address specifies each of the 32,768 bytes uniquely. Internally, the memory array is organized into 32 blocks of 8Kb each. The 5 most-significant address lines decode one of 32 blocks. This block segmentation has no effect on operation, however the user may wish to group data into blocks by its endurance characteristics as explained on page 4.

The cycle time is the same for read and write memory operations. This simplifies memory controller logic and timing circuits. Likewise the access time is the same for read and write memory operations. When /CE is deasserted high, a precharge operation begins, and is required of every memory cycle. Thus unlike SRAM, the access and cycle times are not equal. Writes occur immediately at the end of the access with no delay. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed.

Note that the FM1808 has no special power-down requirements. It will not block user access and it contains no power-management circuits other than a simple internal power-on reset. It is the user's responsibility to ensure that VDD remains within datasheet tolerances to prevent incorrect operation. Also proper voltage level and timing relationships between VDD and /CE must be maintained in power-up and power-down events.

Memory Operation

The FM1808 is designed to operate in a manner similar to other bytewide memory products. For users familiar with BBSRAM, the performance is comparable but the bytewide interface operates in a slightly different manner as described below. For users familiar with EEPROM, the obvious differences result from the higher write performance of FRAM technology including NoDelay writes and much higher write endurance.

Read Operation

A read operation begins on the falling edge of /CE. At this time, the address bits are latched and a memory cycle is initiated. Once started, a full memory cycle must be completed internally even if /CE goes inactive. Data becomes available on the bus after the access time has been satisfied.

After the address has been latched, the address value may be changed upon satisfying the hold time parameter. Unlike an SRAM, changing address values will have no effect on the memory operation after the address is latched.

The FM1808 will drive the data bus when /OE is asserted low. If /OE is asserted after the memory access time has been satisfied, the data bus will be driven with valid data. If /OE is asserted prior to completion of the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven onto the bus. When /OE is inactive the data bus will remain tri-stated.

Write Operation

Writes occur in the FM1808 in the same time interval as reads. The FM1808 supports both /CE- and /WE-controlled write cycles. In all cases, the address is latched on the falling edge of /CE.

In a /CE controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when /CE falls. In this case, the part begins the memory cycle as a write. The FM1808 will not drive the data bus regardless of the state of /OE.

In a /WE controlled write, the memory cycle begins on the falling edge of /CE. The /WE signal falls after the falling edge of /CE. Therefore, the memory cycle begins as a read. The data bus will be driven according to the state of /OE until /WE falls. The timing of both /CE- and /WE-controlled write cycles is shown in the electrical specifications.

Write access to the array begins asynchronously after the memory cycle is initiated. The write access terminates on the rising edge of /WE or /CE, whichever is first. Data set-up time, as shown in the electrical specifications, indicates the interval during which data cannot change prior to the end of the write access.

Unlike other truly nonvolatile memory technologies, there is no write delay with FRAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the

bus. The entire memory operation occurs in a single bus cycle. Therefore, any operation including read or write can occur immediately following a write. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Precharge Operation

The precharge operation is an internal condition that prepares the memory for a new access. All memory cycles consist of a memory access and a precharge. The precharge is initiated by deasserting the /CE pin high. It must remain high for at least the minimum precharge time t_{PC}.

The user determines the beginning of this operation since a precharge will not begin until /CE rises. However, the device has a maximum /CE low time specification that must be satisfied.

Endurance

Internally, a FRAM operates with a read and restore mechanism. Therefore, each read and write cycle involves a change of state. The memory architecture is based on an array of rows and columns. Each read or write access causes an endurance cycle for an entire row. In the FM1808, a row is 32 bits wide. Every 4-byte boundary marks the beginning of a new row. Endurance can be optimized by ensuring frequently accessed data is located in different rows. Regardless, FRAM offers substantially higher write endurance than other nonvolatile memories. The rated endurance limit of 10^{10} cycles will allow 30 accesses per second to the same row for over 10 years.

FRAM Design Considerations

When designing with FRAM for the first time, users of SRAM will recognize a few minor differences. First, bytewide FRAM memories latch each address on the falling edge of chip enable. This allows the address bus to change after starting the memory access. Since every access latches the memory address on the falling edge of /CE, users cannot ground it as they might with SRAM.

Users who are modifying existing designs to use FRAM should examine the memory controller for timing compatibility of address and control pins. Each memory access must be qualified with a low transition of /CE. In many cases, this is the only change required. An example of the signal relationships is shown in Figure 2 below. Also shown is a common SRAM signal relationship that will not work for the FM1808.

The reason for /CE to strobe for each address is two-fold: it latches the new address and creates the necessary precharge period while /CE is high.

A second design consideration relates to the level of V_{DD} during operation. Battery-backed SRAMs are forced to monitor V_{DD} in order to switch to battery backup. They typically block user access below a certain V_{DD} level in order to prevent loading the battery with current demand from an active SRAM. The user can be abruptly cut off from access to the nonvolatile memory in a power down situation with no warning or indication.

FRAM memories do not need this system overhead. The memory will not block access at any V_{DD} level. The user, however, should prevent the processor from accessing memory when V_{DD} is out-of-tolerance. The common design practice of holding a processor in reset when V_{DD} drops is adequate; no special provisions must be taken for FRAM design.

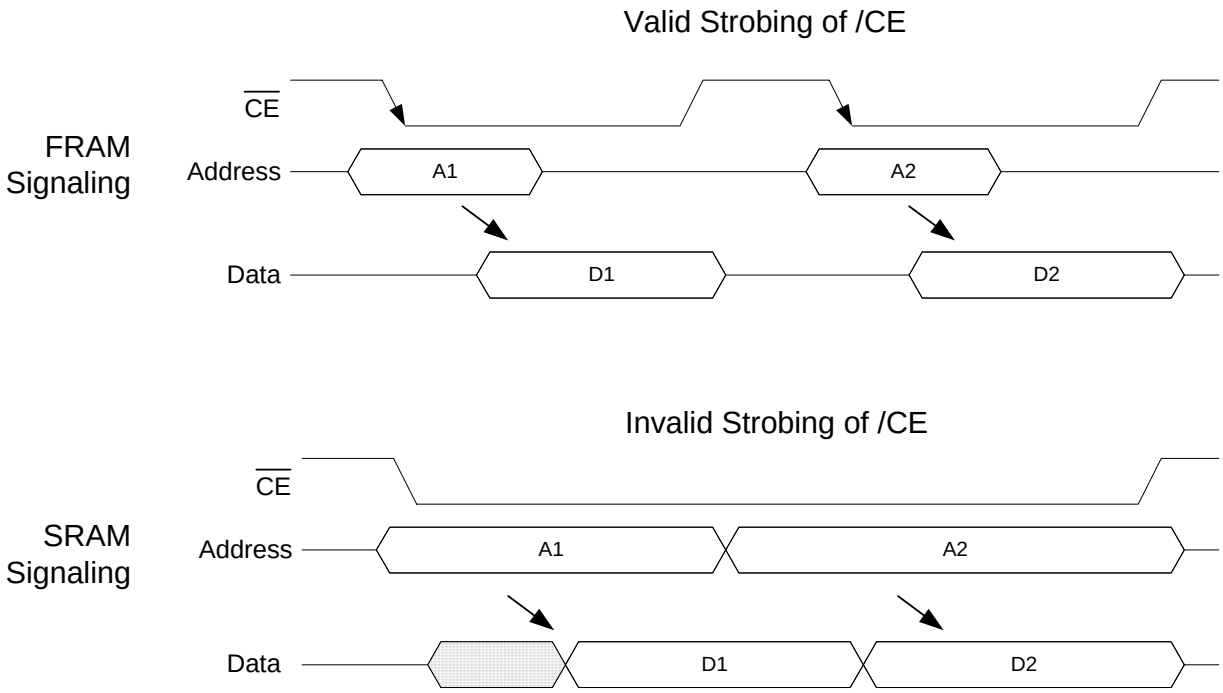


Figure 2. Chip Enable and Memory Address Relationships

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +7.0V
V_{IN}	Voltage on any pin with respect to V_{SS}	-1.0V to +7.0V and $V_{IN} < V_{DD}$+1.0V
T_{STG}	Storage Temperature	-55°C to + 125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply	4.5	5.0	5.5	V	
I_{DD1}	V_{DD} Supply Current (180 ns cycle)		7	15	mA	1
I_{DD2}	V_{DD} Supply Current (130 ns cycle)		12	25	mA	1
I_{SB1}	Standby Current – TTL input levels			400	µA	2
I_{SB2}	Standby Current – CMOS input levels		7	20	µA	3
I_{LI}	Input Leakage Current	-		10	µA	4
I_{LO}	Output Leakage Current	-		10	µA	4
V_{IH}	Input High Voltage	2.0		V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{OH}	Output High Voltage (I_{OH} = -2.0 mA)	2.4		-	V	
V_{OL}	Output Low Voltage (I_{OL} = -4.2 mA)	-		0.4	V	

Notes

1. V_{DD} = 5.5V, /CE cycling at minimum cycle time. All inputs at CMOS levels, all outputs unloaded.
2. V_{DD} = 5.5V, /CE at V_{IH}, All other pins at TTL levels.
3. V_{DD} = 5.5V, /CE at V_{IH}, All other pins at CMOS levels.
4. V_{IN}, V_{OUT} between V_{DD} and V_{SS}.

Data Retention (V_{DD} = 4.5V to 5.5V unless otherwise specified)

Parameter	Min	Units	Notes
Data Retention	10	years	

Read Cycle AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CE}	Chip Enable Access Time (to data valid)		70	ns	
t_{CA}	Chip Enable Active Time	70	2,000	ns	
t_{RC}	Read Cycle Time	130		ns	
t_{PC}	Precharge Time	60		ns	
t_{AS}	Address Setup Time	4		ns	3
t_{AH}	Address Hold Time	10		ns	
t_{OE}	Output Enable Access Time		10	ns	
t_{HZ}	Chip Enable to Output High-Z		15	ns	1
t_{OHZ}	Output Enable to Output High-Z		15	ns	1

Write Cycle AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CA}	Chip Enable Active Time	70	2,000	ns	
t_{CW}	Chip Enable to Write High	70		ns	
t_{WC}	Write Cycle Time	130		ns	
t_{PC}	Precharge Time	60		ns	
t_{AS}	Address Setup Time	4		ns	3
t_{AH}	Address Hold Time	10		ns	
t_{WP}	Write Enable Pulse Width	40		ns	
t_{DS}	Data Setup	30		ns	
t_{DH}	Data Hold	5		ns	
t_{WZ}	Write Enable Low to Output High Z		15	ns	1
t_{WX}	Write Enable High to Output Driven	10		ns	1
t_{HZ}	Chip Enable to Output High-Z		15	ns	1
t_{WS}	Write Enable Setup	0		ns	2
t_{WH}	Write Enable Hold	0		ns	2

Notes

1 This parameter is periodically sampled and not 100% tested.

2 The relationship between /CE and /WE determines if a /CE- or /WE-controlled write occurs. There is no timing specification associated with this relationship.

3 The minimum address setup time is 0 ns when the device is operating above 0° C.

Power Cycle Timing (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{PU}	V_{DD}(min) to First Access Start	1	-	µS	
t_{PD}	Last Access Complete to V_{DD}(min)	0	-	µS	

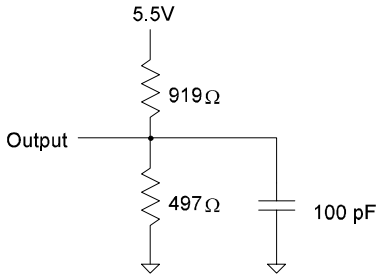
Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 5V)

Symbol	Parameter	Min	Max	Units	Notes
$C_{I/O}$	Input Output Capacitance	-	8	pF	
C_{IN}	Input Capacitance	-	6	pF	

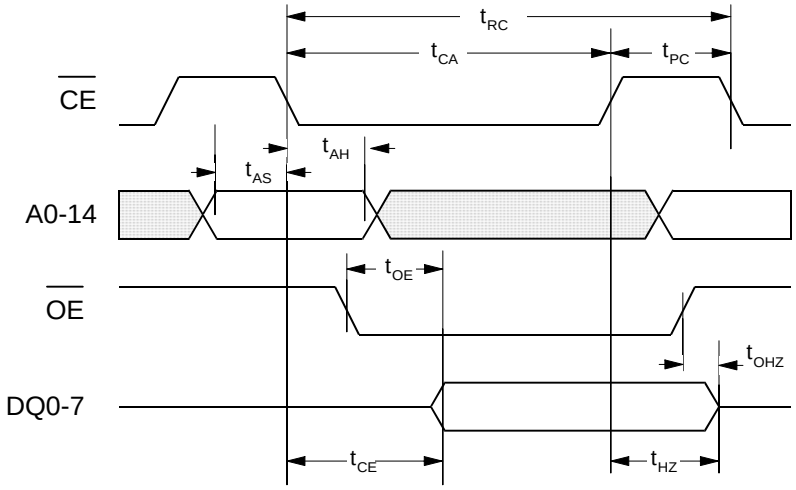
AC Test Conditions

Input Pulse Levels	0 to 3V
Input rise and fall times	10 ns
Input and output timing levels	1.5V

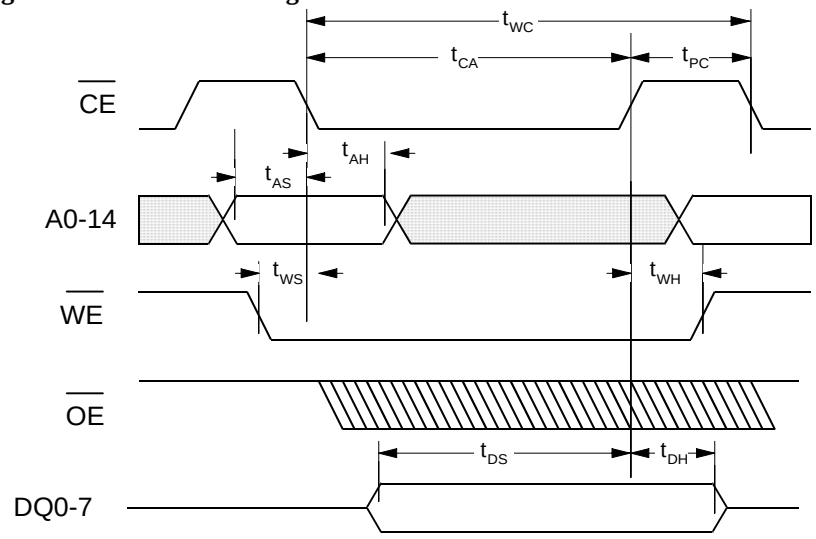
Equivalent AC Load Circuit



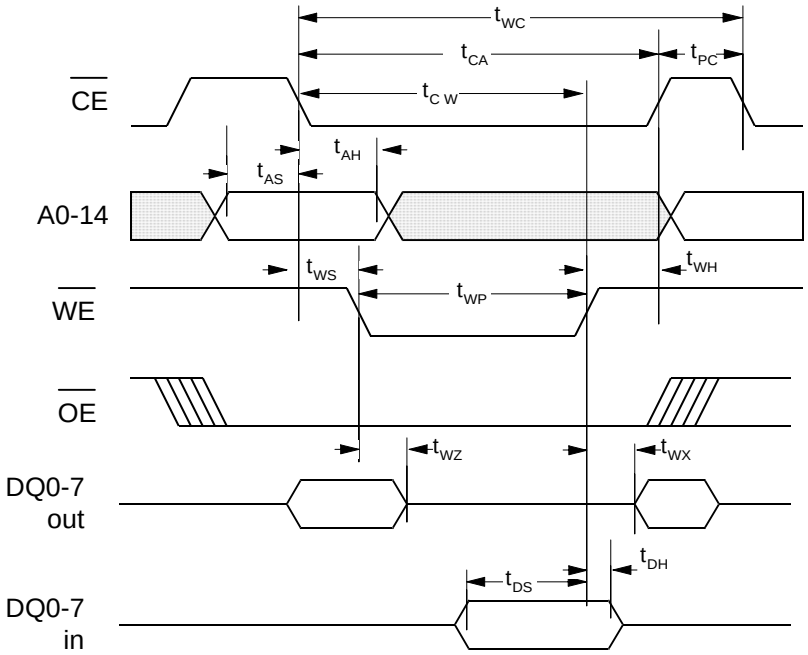
Read Cycle Timing



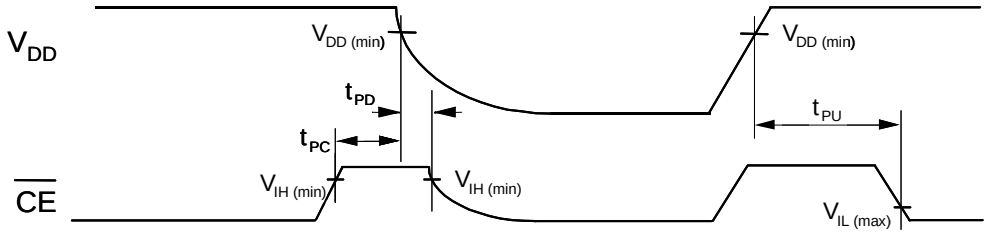
Write Cycle Timing - /CE Controlled Timing



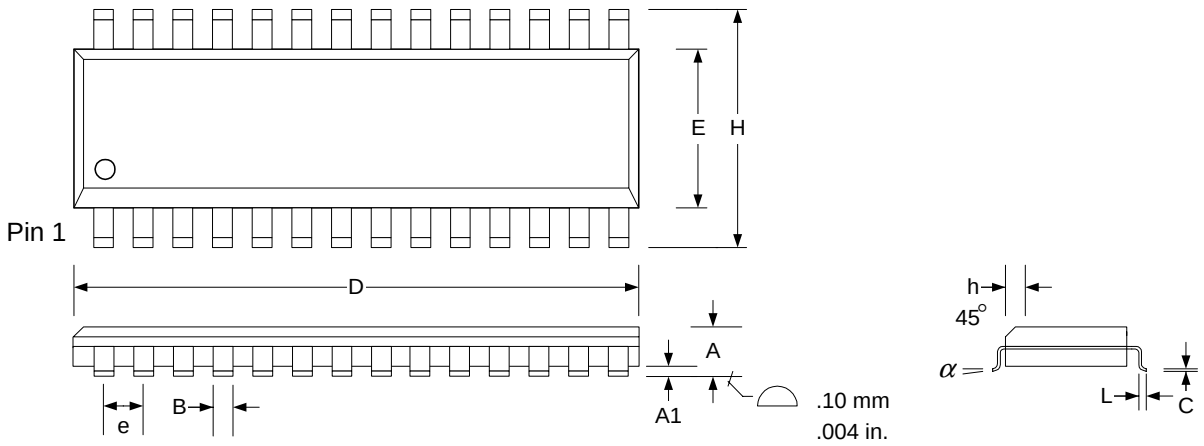
Write Cycle Timing - /WE Controlled Timing



Power Cycle Timing



28-pin SOIC (JEDEC MS-013 variation AE)

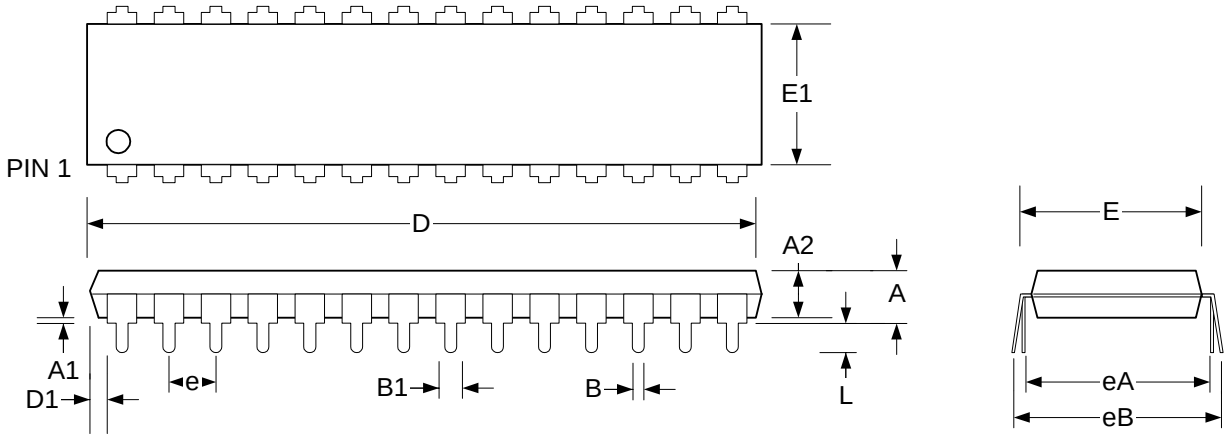


Selected Dimensions

For complete dimensions and notes, refer to JEDEC MS-013
Controlling dimensions in millimeters.
Conversions to inches are not exact.

Symbol	Dim	Min	Nom.	Max
A	mm in.	2.35 0.0926		2.65 0.1043
A1	mm in.	0.10 0.004		0.30 0.0118
B	mm in.	0.33 0.013		0.51 0.020
C	mm in.	0.23 0.0091		0.32 0.0125
D	mm in.	17.70 0.6969		18.10 0.7125
E	mm in.	7.40 0.2914		7.60 0.2992
e	mm in.		1.27 BSC 0.050 BSC	
H	mm in.	10.00 0.394		10.65 0.419
h	mm in.	0.25 0.010		0.75 0.029
L	mm in.	.40 0.016		1.27 0.050
α		0°		8°

28-pin DIP JEDEC MS-011



Selected Dimensions

For complete dimensions and notes, refer to JEDEC MS-011
Controlling dimensions in inches.
Conversions to millimeters are not exact.

Symbol	Dim	Min	Nom.	Max
A	in.			0.250
	mm			6.35
A1	in.	0.015		
	mm	0.39		
A2	in.	0.125		0.195
	mm	3.18		4.95
B	in.	0.014		0.022
	mm	0.356		0.558
B1	in.	0.030		0.070
	mm	0.77		1.77
D	in.	1.380		1.565
	mm	35.1		39.7
D1	in.	0.005		
	mm	0.13		
E	in.	0.600		0.625
	mm	15.24		15.87
E1	in.	0.485		0.580
	mm	12.32		14.73
e	in.		0.100 BSC	
	mm		2.54 BSC	
eA	in.		0.600 BSC	
	mm		15.24 BSC	
eB	in.			0.700
	mm			17.78
L	in.	0.115		0.200
	mm	2.93		5.08