

ON Semiconductor®

# FDD8444L-F085

# N-Channel PowerTrench<sup>®</sup> MOSFET

# **40V**, **50A**, **6.0m** $\Omega$

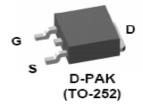
#### **Features**

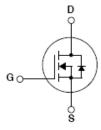
- Typ  $r_{DS(on)}$  = 3.8m $\Omega$  at  $V_{GS}$  = 5V,  $I_D$  = 50A
- Typ  $Q_{q(tot)}$  = 46nC at  $V_{GS}$  = 5V
- Low Miller Charge
- Low Q<sub>rr</sub> Body Diode
- UIS Capability (Single Pulse/ Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant



## **Applications**

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Transmission
- Distributed Power Architecture and VRMs
- Primary Switch for 12V and 24V systems





# **MOSFET Maximum Ratings** $T_C = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain to Source Voltage		40	V
V <sub>GS</sub>	Gate to Source Voltage		±20	V
	Drain Current Continuous (T <sub>C</sub> < 150°C, V <sub>GS</sub> = 10V)	(Note 1)	50	
$I_D$	Continuous ( $T_{amb} = 25^{\circ}C$ , $V_{GS} = 10V$ , with $R_{\theta JA} = 52^{\circ}C/W$ )		16	Α
	Pulsed		See Figure 4	
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 2)	295	mJ
П	Power Dissipation		153	W
$P_{D}$	Derate above 25°C		1.02	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature		-55 to +175	°C

### **Thermal Characteristics**

$R_{ heta JC}$	Thermal Resistance, Junction to Case	0.98	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient TO-252, 1in <sup>2</sup> copper pad area	52	°C/W

# **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8444L	FDD8444L-F085	TO-252AA	13"	12mm	2500 units

# **Electrical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted

**Parameter** 

Off Cha	Off Characteristics						
B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	40	-	-	V	
		1/ 001/					

**Test Conditions** 

Min

Тур

Max

B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	/	40	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 32V$ ,		-	-	1	^
		$V_{GS} = 0V$	$T_J = 150^{\circ}C$	-	-	250	μА
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20V$		-	-	±100	nA

#### On Characteristics

Symbol

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	1	1.8	3	V
	Drain to Source On Resistance	I <sub>D</sub> = 50A, V <sub>GS</sub> = 10V	-	3.5	5.2	
		I <sub>D</sub> = 50A, V <sub>GS</sub> = 5V	-	3.8	6.0	
r <sub>DS(on)</sub>		I <sub>D</sub> = 50A, V <sub>GS</sub> = 4.5V	-	4.0	6.5	mΩ
		I <sub>D</sub> = 50A, V <sub>GS</sub> = 5V, T <sub>J</sub> = 175°C	-	6.8	10.7	

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	\\ - 05\\ \\ - 0	2) (	-	5530	-	pF
Coss	Output Capacitance		$V_{DS} = 25V, V_{GS} = 0V,$ f = 1MHz		605	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 11/11/12			400	-	pF
$R_G$	Gate Resistance	f = 1MHz		-	1.7	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 5V	$V_{GS} = 0$ to 5V		-	46	60	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0$ to $2V$	V <sub>DD</sub> = 20V	-	5.4	7	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		I <sub>D</sub> = 50A	-	16.3	-	nC
Q <sub>gs2</sub>	Gate Charge Threshold to Plateau	I <sub>g</sub> = 1	$I_g = 1.0 mA$	-	10.9	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge			-	21	-	nC

# **Electrical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units

# **Switching Characteristics**

t <sub>on</sub>	Turn-On Time		-	-	104	ns
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD}$ = 20V, $I_{D}$ = 50A $V_{GS}$ = 5V, $R_{GS}$ = 2 $\Omega$	-	18.7	-	ns
t <sub>r</sub>	Turn-On Rise Time		-	46	-	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	42	-	ns
t <sub>f</sub>	Turn-Off Fall Time		-	19.2	-	ns
t <sub>off</sub>	Turn-Off Time		-	-	96	ns

#### **Drain-Source Diode Characteristics**

V	Source to Drain Diode Voltage	I <sub>SD</sub> = 50A	-	0.9	1.25	V
v <sub>SD</sub>	Source to Drain Diode Voltage	I <sub>SD</sub> = 25A	-	0.8	1.0	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>E</sub> = 50A, dI <sub>E</sub> /dt = 100A/μs	-	34	44	ns
Q <sub>rr</sub>	Reverse Recovery Charge	I <sub>F</sub> = 50A, dI <sub>F</sub> /dt = 100A/μS	-	29	38	nC

Package current limitation is 50A.
 Starting T<sub>J</sub> = 25°C, L = 0.37mH, I<sub>AS</sub> = 40A.

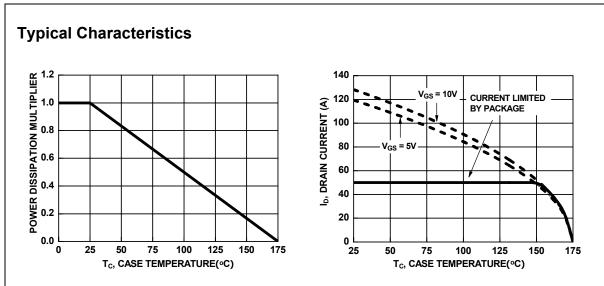


Figure 1. Normalized Power Dissipation vs Case Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

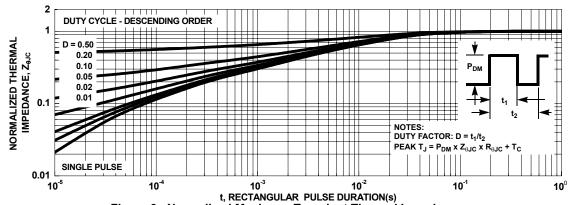


Figure 3. Normalized Maximum Transient Thermal Impedance

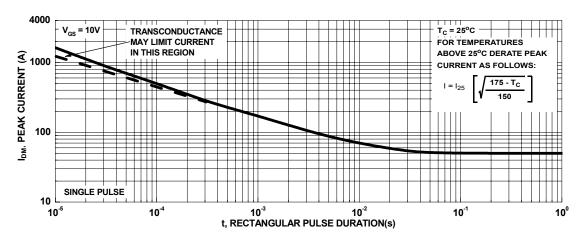


Figure 4. Peak Current Capability

## **Typical Characteristics**

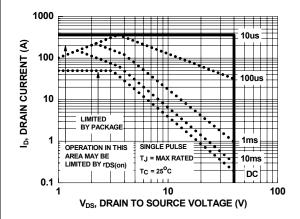


Figure 5. Forward Bias Safe Operating Area

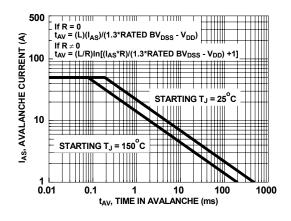


Figure 6. Unclamped Inductive Switching Capability

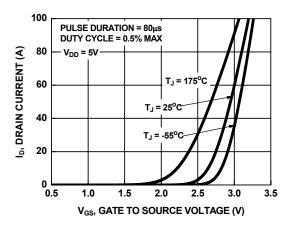


Figure 7. Transfer Characteristics

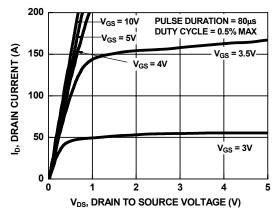


Figure 8. Saturation Characteristics

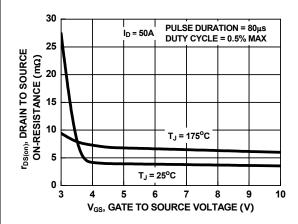


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

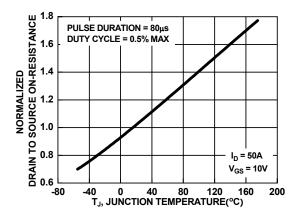


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

# **Typical Characteristics**

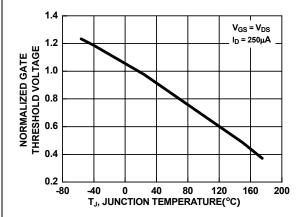


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

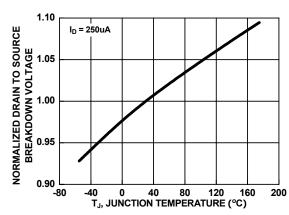


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

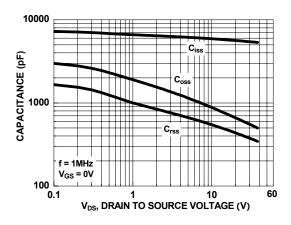


Figure 13. Capacitance vs Drain to Source Voltage

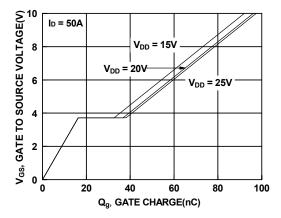


Figure 14. Gate Charge vs Gate to Source Voltage

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