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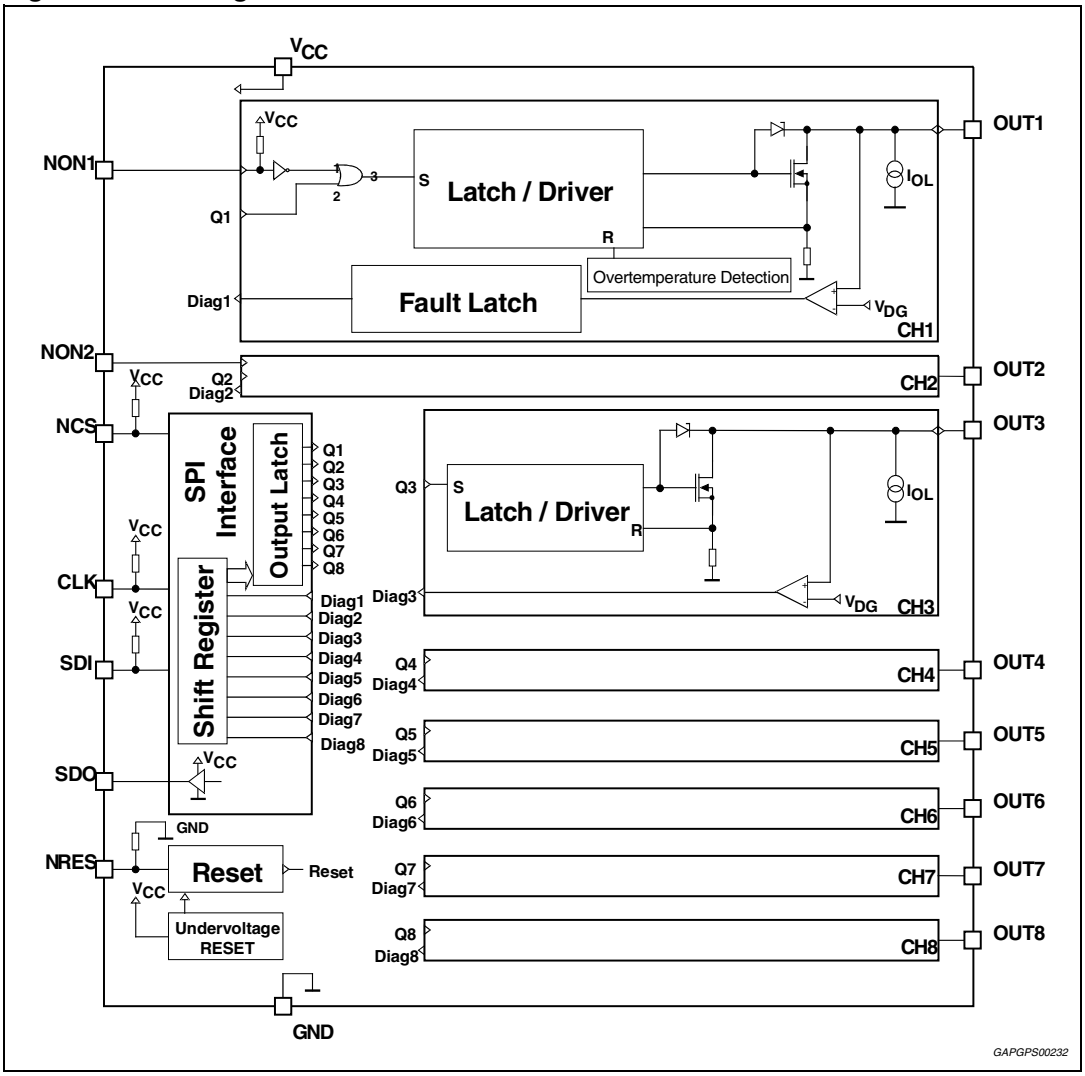
1 Block Diagram

Figure 1.Block diagram



2 Pins description

Figure 2. Connection diagram (top view)

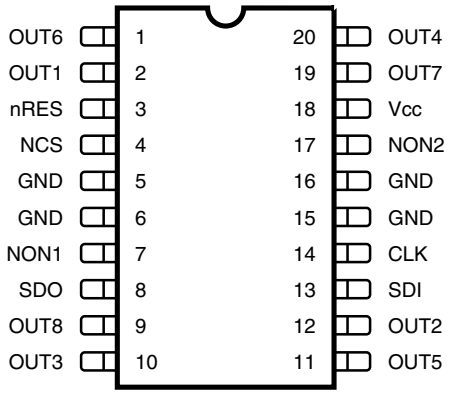


Table 2. Pin description

N°	Pin	Description
1	Out 6	Output 6
2	Out 1	Output 1
3	NRes	Asynchronous reset
4	NCS	Chip select (active low)
5	GND	Device ground
6	GND	Device ground
7	NON1	Control input 1
8	SDO	Serial data output
9	Out 8	Output 8
10	Out 3	Output 3
11	Out 5	Output 5
12	Out 2	Output 2
13	SDI	Serial data input
14	CLK	Serial clock
15	GND	Device ground
16	GND	Device ground
17	NON2	Control input 2
18	V_{CC}	Supply voltage
19	Out 7	Output 7
20	Out 4	Output 4

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings for voltages and currents applied externally to the device

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	-	-0.3	-	7	V
Inputs and data lines (NONx, NCS, CLK, SDI, nRes)						
V_{IN}	Voltage (NONx, NCS, CLK, SDI, nRes)		-0.3	-	7	V
I_{IN}	Protection diodes current(1)	$T \leq 1ms$	-20	-	20	mA
Outputs (Out1 ... Out8)						
V_{OUTc}	Continuous output voltage	-	-0.7	-	45	V
I_{OUT}	Output current (2)	-	-2	-	1.0	A
E_{OUTcl}	Output clamp energy	$I_{OUT} \leq 150mA$	-	-	10	mJ

1. All inputs are protected against ESD according to MIL 883C; tested with HBM at 2 kV. It corresponds to a dissipated energy $E \leq 0.2$ mJ.
2. Transient pulses in accordance to DIN40839 part 1, 3 and ISO 7637 Part 1, 3.

Table 4. Absolute maximum ratings for currents determined within the device

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Outputs (Out1 ... Out8)						
I_{OUT}	Output current (Out1, Out2)	-	-	-	I_{LIM}	A
	Output current (Out3 ... Out8)	-	-	-	I_{SCB}	A
ΣI_{OUT1} i = 1-8	Total average-current all outputs (1)	T_{amb} = 60°C	2.0	-	-	A

1. When operating the device with short circuit 1ch and 2ch outputs at the same time, damage due to electrical overstress might occur.

3.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Thermal shutdown						
T_{JSC}	Thermal shutdown threshold	-	150	165	-	°C
Thermal resistance						
$R_{thj\ a\text{-}one}$	Single output (junction ambient)	-	-	-	90	°C/W
$R_{thj\ a\text{-}all}$	All outputs (junction ambient)	-	-	-	75	°C/W
$R_{th\ j\text{-}pin}$	Junction to Pin	-	-	-	18	°C/W

3.3 Electrical characteristics

Refer to 4.5 V ≤ V_{CC} ≤ 5.5 V; -40 °C ≤ T_J ≤ 150 °C; unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
I_{ccSTB}	Standby current	without load (nRes = Low)	-	-	70	µA
I_{ccOPM}	Operating mode	$I_{OUT1 \ldots 8}$ = 500 mA SPI - CLK = 3 MHz NCS = LOW SDO no load	-	-	5	mA
ΔI_{CC}	ΔI_{CC} during reverse output current	I_{out} = -2 A	-	-	100	mA
V_{DDRES}	Undervoltage reset	Reset of all registers and disable of all outputs	3	-	4	V
Inputs (NONx. NCS, CLK, SDI, nRES)						
V_{INL}	Low level	-	-0.3	-	$0.2 \cdot V_{CC}$	V
V_{INH}	High level	-	$0.7 \cdot V_{CC}$	-	V_{CC} +0,3	V
V_{hyst}	Hysteresis voltage	-	0.85	-	-	V
I_{IN}	Input current	NONx, NCS, CLK, SDI $V_{IN} = V_{CC}$	-	-	10	µA
		NRES (V_{IN} = 0V)	-10	-	-	µA
R_{IN}	Pull-up resistance	(NONx, NCS, CLK, SDI) Pull-down resistance (NRes)	50	-	250	kΩ
C_{IN}	Input capacitance	Guaranteed by design	-	-	10	pF
Serial data outputs						
V_{SDOH}	High output level	I_{SDO} = -4mA	V_{CC} -0.4	-	-	V
V_{SDOL}	Low output level	I_{SDO} = 3,2mA		-	0.4	V
I_{SDOL}	Tristate leakage current	NCS = high; 0V ≤ V_{SDO} ≤ V_{CC}	-10	-	10	µA
C_{SDO}	Output capacitance	f_{SDO} = 300 kHz, Guaranteed by design	-	-	10	pF
Outputs OUT 1 ... 8						
$I_{OUTL1 - 8}$	Leakage current	OUTx = OFF; V_{OUTx} = 25 V; V_{CC} = 5 V	-	-	100	µA
		OUTx = OFF; V_{OUTx} = 16 V; V_{CC} = 5 V	-	-	100	µA
		OUTx = OFF; V_{OUTx} = 16 V; V_{CC} = 1 V	-	-	10	µA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{clp}	Output clamp voltage	1 mA ≤ I_{clp} ≤ I_{outp}; I_{test} = 10 mA with correlation	45	-	62	V
R_{DSon}	On resistance OUT 1 ... 8	I_{OUT} = 250 mA; T_j = +150 °C	-	-	3.0	Ω
C_{OUT}	Output capacitance	V_{OUT} = 16 V; f = 1 MHz guaranteed by design	-	-	300	pF
Outputs short circuit protection						
I_{SBC}	Overcurrent shutoff threshold	OUT3 ... OUT8	0.45	-	1.1	A
I_{LIM}	Short circuit current limitation	OUT1; OUT2	0.5	-	1.1	A
t_{SCB}	Delay shutdown	-	0.2	3,0	12	µs
Diagnostics						
V_{DG}	Diagnostic threshold voltage	-	0.32 ·V_{CC}	-	0.4·V_{CC}	V
I_{OL}	Open load detection sink current	V_{out} = V_{DG}	20	-	100	µA
t_{df}	Diagnostic detection filter time	for output 1 & 2 on each diagnostic condition	15	-	50	µs
Outputs timing						
t_{don1}	Turn ON delay of OUT 1 and 2	$NON_{1,2}$ = 50% to V_{OUT} = 0,9·V_{bat} NCS = 50% to V_{OUT} = 0,9·V_{bat} (V_{BAT} = 16V, R_L = 500Ω)	-	-	5	µs
t_{don2}	Turn ON delay of OUT 3 to 8	NCS = 50% to V_{OUT} = 0,9·V_{bat} (V_{BAT} = 16V, R_L = 500Ω)	-	-	10	µs
t_{doff}	Turn OFF delay of OUT 1 to 8	NCS = 50% to V_{OUT} = 0,1·V_{bat} $NON_{1,2}$ = 50% to V_{OUT} = 0,1·V_{bat} (V_{BAT} = 16V, R_L = 500Ω)	-	-	10	µs
$dU_{on1/dt}$	Turn ON voltage slew-rate	For output 3 to 8; 90% to 30% of V_{bat}; R_L = 500Ω; V_{bat} = 16V	0.7	-	3.5	V/µs
$dU_{on2/dt}$	Turn ON voltage slew-rate	For output 1 and 2; 90% to 30% of V_{bat}; R_L = 500Ω; V_{bat} = 16V	2	-	10	V/µs
$dU_{off1/dt}$	Turn OFF voltage slew-rate	For output 1 to 8; 30% to 90% of V_{bat}; R_L = 500Ω; V_{bat} = 16V	2	-	10	V/µs
$dU_{off2/dt}$	Turn OFF voltage slew-rate	For output 1 to 8; 30% to 80% of V_{bat}; R_L = 500Ω; V_{bat} = 0.9 · V_{clp}	2	-	15	V/µs
Serial diagnostic link (load capacitor at SDO = 100 pF)						
f_{clk}	Clock frequency	50 % duty cycle	-	-	3	MHz
t_{clh}	Minimum time CLK = high	-	160	-	-	ns
t_{cll}	Minimum time CLK = low	-	160	-	-	ns
t_{pcld}	Propagation delay CLK to data at SDO valid	4.9 V ≤ V_{CC} ≤ 5.1V	-	-	100	ns

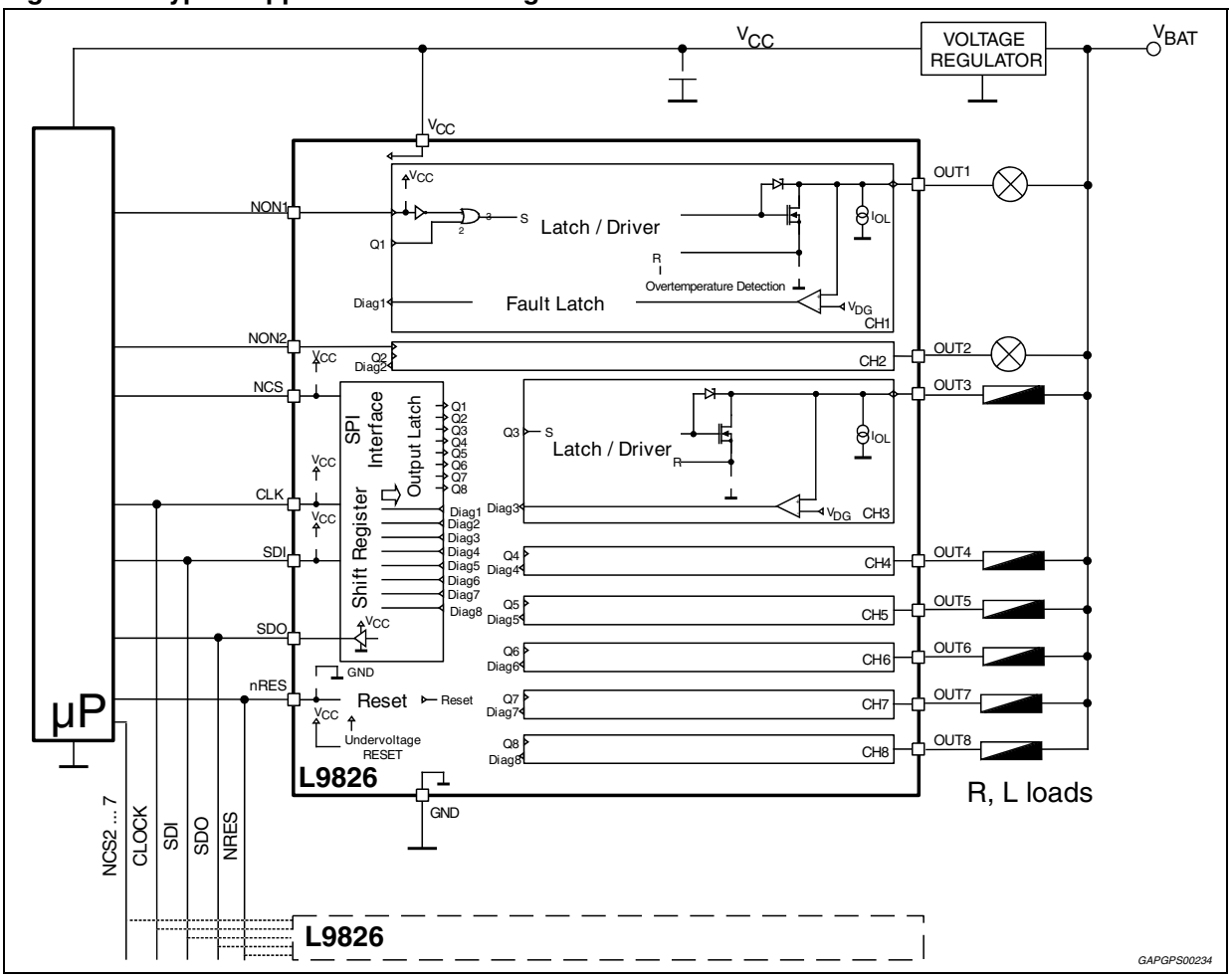
Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{csdv}	NCS = LOW to data at SDO active	-	-	-	100	ns
t_{sclch}	CLK low before NCS low	Setup time CLK to NCS change H/L	100	-	-	ns
t_{hclcl}	CLK change L/H after NCS = low	-	100	-	-	ns
t_{scld}	SDI input setup time	CLK change H/L after SDI data valid	20	-	-	ns
t_{hcld}	SDI input hold time	SDI data hold after CLK change H/L	-	-	20	ns
t_{sclcl}	CLK low before NCS high	-	150	-	-	ns
t_{hclch}	CLK high after NCS high	-	150	-	-	ns
t_{pchdz}	NCS L/H to output data float	-	-	-	100	ns
-	NCS pulse filter time	Multiple of 8 CLK cycles inside NCS period	-	-	-	-

4 Application information

The typical application diagram is shown in *Figure 3*.

Figure 3. Typical application circuit diagram



For higher current capability the two outputs of the same kind can be paralleled and the maximum flyback energy should not exceed the limit for a single output.

The circuit immunity at output transients have been verified during the characterization with Test Pulses 1, 2, 3a and 3b, DIN40839 or ISO7637 part 3.

The Test Pulses are coupled to the outputs with 200 pF series capacitor and all the outputs are able to withstand to test pulses without damage. The load applied was in the range of 30 to 100 ohm for the resistive part and 0 to 600 mH for the inductive one.

5 Functional description

5.1 General

The L9826 is an 8-channel low-side driver assembled in SO20 package. Its 8-bit SPI serial interface is designed to control all the outputs and to provide their diagnosis. Channels 1 and 2 are controlled either via SPI or via parallel through the inputs pins NON1 and NON2. Diagnostic recognizes operative fault conditions: open load, short circuits to GND or to VB and overcurrent.Thermal shutdown for outputs 1 and 2 is available as well the output voltage clamp which is essential in case of working with inductive loads.

The reset feature is an OR function of the external reset nRes and the internal reset generate during the undervoltage condition

5.2 Output stage control

5.2.1 Via parallel, only for output 1 and 2

This is valid only for Outputs 1 and 2 which are controlled through the dedicated inputs NON1 and NON2 (both active low) which are internally configured as pull-up (see *Figure 3*). This is to guarantee that the outputs are off in case of inputs open.

A further feature is the possibility to drive these outputs through a PWM signal independently by SPI commands.

Reset signal is common for all the eight channels and it is active low. After an external reset condition (that means NRES pin switched from low to high) to drive outputs 1 and 2 through the parallel input (NON1 and NON2) it is necessary to disable the parallel input itself (NON1, NON2 high) and then subsequently to drive the outputs 1 and 2 at the logic state desiderated through NON1 and NON2. The duration of the command (T) as reported in the *Figure 4* should be at less in the order of 100 nSecond.

In the next *Figure 4* is shown this behavior and in the next *Table 7* is summarized the scenario of parallel/series commands.

Figure 4. Parallel control for output 1 and 2 (Example for Power-on)

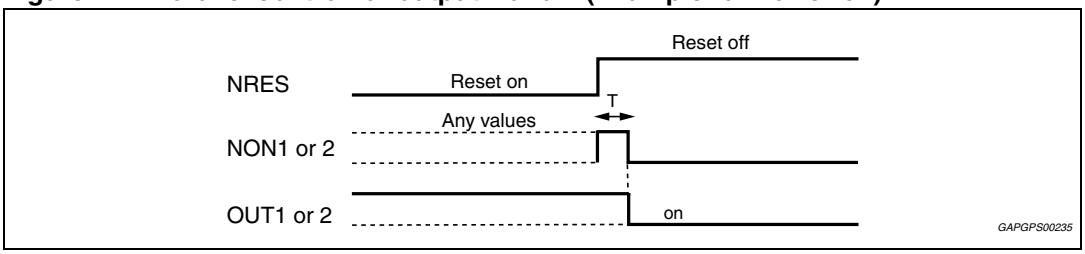


Table 7. Outputs control tables

Outputs 1, 2:					Outputs 3 to 8:		
NON1, 2	1	0	0	1	-	-	-
SPI-bit 1, 2	0	0	1	1	SPI-bit 3 ... 8	0	1
Output 1, 2	off	on	on	on	Output 3 ... 8	off	on

5.2.2 Via 8-bit SPI for all the outputs

Control data are transmitted to SDI through a microcontroller in configuration master. The device is selected when NCS signal is low. The 8-bit command data are transmitted into L9826 shift registers every CLK falling edge (see *Figure 6* for SPI signals timing).

The NCS rising edge latches the new data from the shift register to the driver and the output are driven following the commands just sent.

The digital filter between NCS and the output latch ensures that the data are transferred only after 8 CLK cycles or multiple of 8 CLK cycles since the last NCS falling edge.

The NCS changes only at low CLK.

Figure 5 shows the control register structure and in the detail its control-bit, while in the *Table 7* are summarized the controls outputs via SPI or dedicated input pins (NON1 and NON2).

Figure 5. Output control register structure

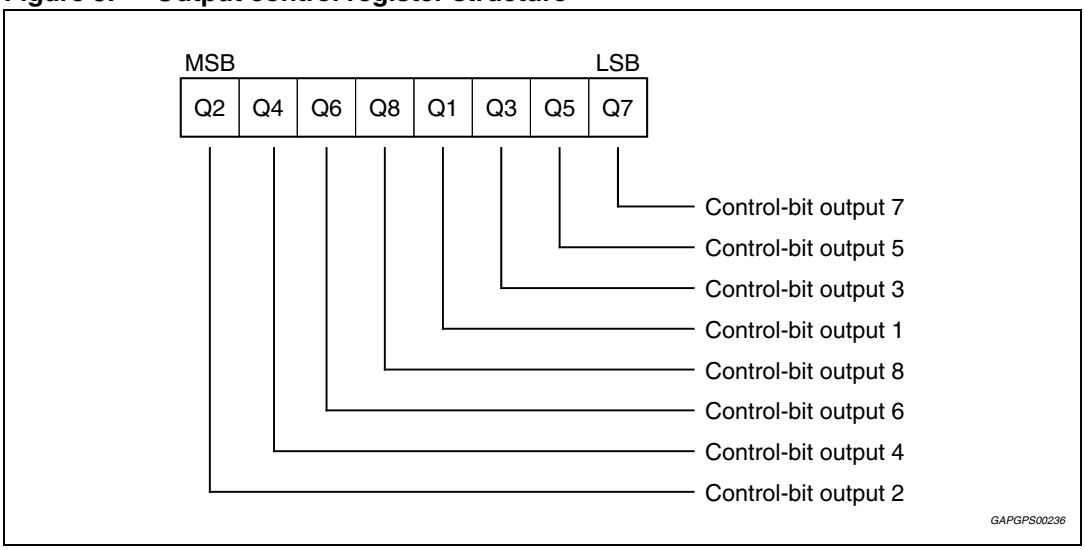
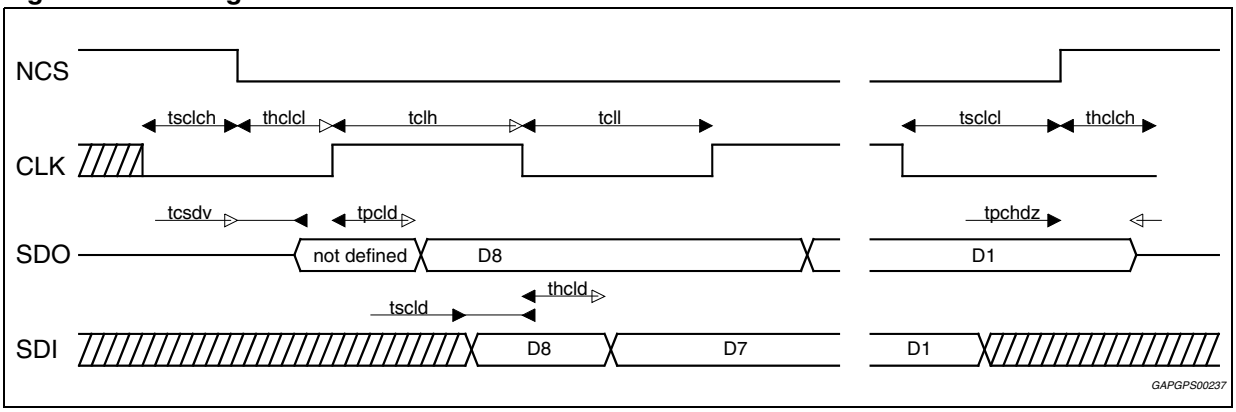


Figure 6. Timing of the serial interface



5.3 Output stage diagnostics

All the outputs voltage are compared with the diagnostic threshold (0.38 Typ · VCC) and this information is transferred in dedicated fault latches which are cleared when the NCS reaches the state low. Afterward the latch stores the status bit and the first reading after the error might be wrong. The second one is considered right.

The next *Figure 7* and *8* show the diagnostic bits read out on SDO and their organization into the dedicated registers.

When NCS is low the data contained in the shift register are transferred to SDO output every CLK rising edge.

Figure 7. The pulse diagram to read the outputs status register

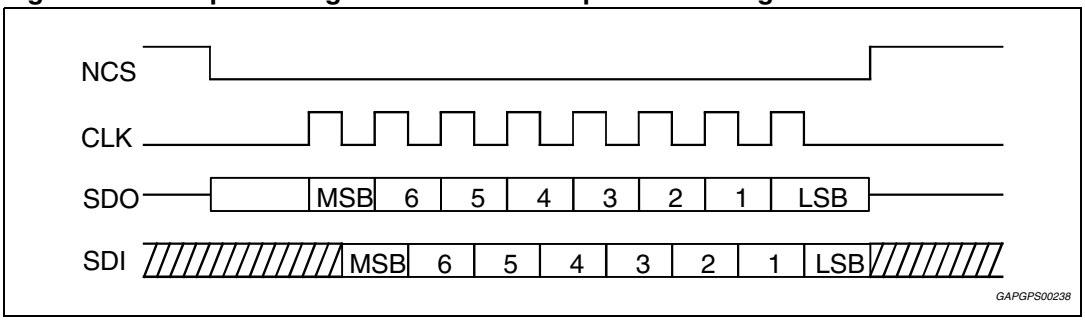
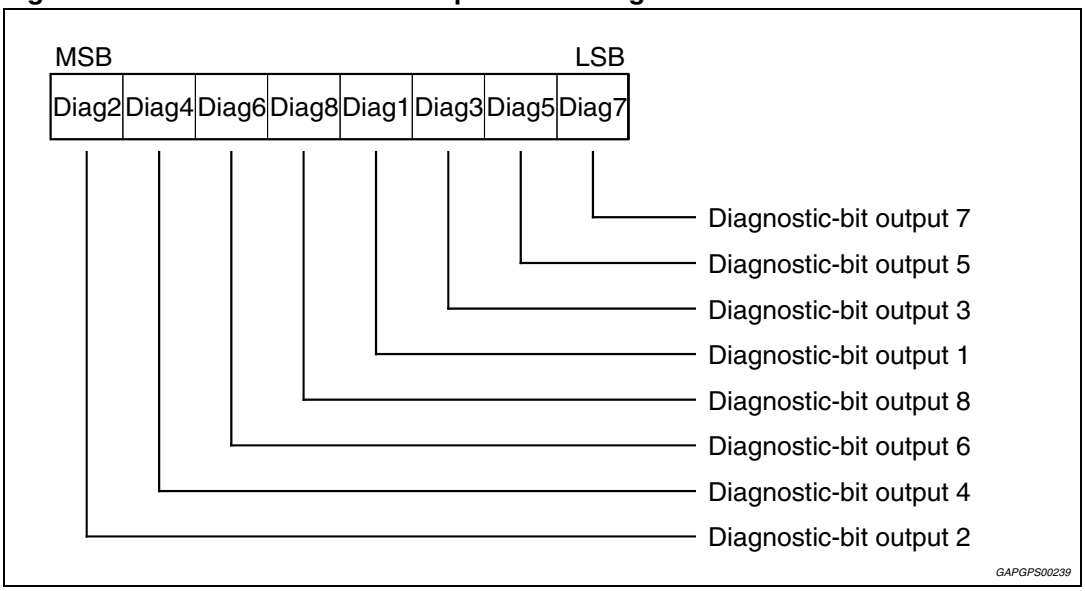


Figure 8. The structure of the outputs status register



5.3.1 Diagnostic on Outputs 1 and 2 controlled via NON1/NON2

Fault condition (1) "output shorted to Vbat"

The output has been previously switched-on and its voltage exceeds the diagnostics threshold. It operates in current regulation mode or it is switched-off if thermal shutdown threshold (T_{JSC}) is reached. The status bit is low.

Fault condition (2) "open load" or "output shorted to GND"

The output is switched-off and its voltage drops below the diagnostics threshold because the load current is lower than the output diagnostic current source. The diagnostic bit is low.

Table 8. Diagnostic table for outputs 1 and 2 in parallel controlled mode

Output 1, 2	Output-voltage	Status-bit	Output-mode
off	> DG-threshold	high	correct operation
off	< DG-threshold	low	fault condition 2)
on	< DG-threshold	high	correct operation
on	> DG-threshold	low	fault condition 1)

5.3.2 Diagnostic on Outputs 1 to 8 controlled via SPI

Fault condition (1) "output shorted to Vbat"

The output was previously switched-on, its voltage exceeds the diagnostic threshold and the result is that the output is switched-off. The diagnostic bit is high.

Fault condition (2) "open load" or "output shorted to GND"

It is the same behavior explained for the outputs 1 and 2 (see paragraph 5.3.1), at NCS falling edge the output status data are transferred to the shift register.

Table 9. Diagnostic table for outputs 1 to 8 in SPI controlled mode

Output 1 ... 8	Output-voltage	Status-bit	Output-mode
off	> DG-threshold	high	correct operation
off	< DG-threshold	low	fault condition 2)
on	< DG-threshold	low	correct operation
on	> DG-threshold	high	fault condition 1)

Load diagnostic: when the output is in OFF condition a typical diagnostic current of 60 µA is sinked.

5.4 Protections

5.4.1 Flyback current

Turning off the low side driver with an inductive load, its output voltage rises due to the inductor that tries to drive current. This voltage is internally clamped by the flyback circuit at V_{CPL} value, typical 50V

5.4.2 Current regulation mode outputs 1 and 2

Outputs 1 and 2 which are particularly dedicated for loads with inrush current (as lamps). When the channel is switched on and the current through the load exceeds the short circuit limit value ($_{Ilim}$) for at least t_{df} time, the corresponding output goes in current regulation mode.

The output current is determinated by the output characteristic and its voltage depends on load resistance. In this mode, high power is dissipated in the output stage and its temperature increases rapidly. When the output stage temperature exceeds the thermal shutdown (T_{JSC}), the overload latch is set and the corresponding output is switched off.

5.4.3 Short circuits outputs 3 to 8

Outputs 3 to 8 which are dedicated for loads without inrush currents. When the output current exceeds the short circuit threshold (I_{sbc}) for at least T_{scb} time, the corresponding output is switched-off immediately and in the same time, the relative latch store the overload status.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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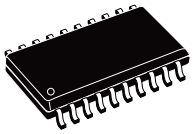
Figure 9. SO20 mechanical data and package dimensions

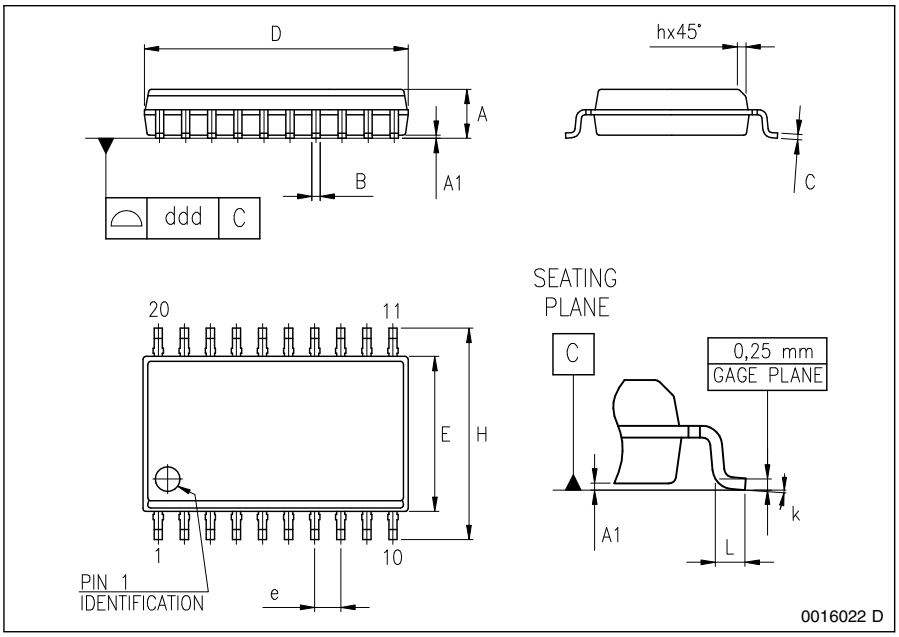
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20



GAPGPS00528

7 Revision history

Table 10. Document revision history

Date	Revision	Changes
22-Apr-2004	7	Initial release in EDOCS
26-Jul-2005	8	Document reformatted. Modify value R_{ON} in the “Features”.
08-Feb-2011	9	Updated *Features* and *Description on page 1*. Updated *Table 1: Device summary on page 1*. Updated *Figure 3: Typical application circuit diagram*. Reworked the content of the *Section 5: Functional description*.
19-Sep-2013	10	Updated Disclaimer.

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