1 Characteristics

Figure 1. Functional diagram

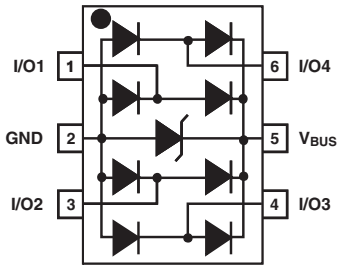


Table 1. Absolute ratings

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	ISO 10605 (C = 330 pF, R = 330 Ω) air discharge contact discharge ISO 10605 (C = 150 pF, R = 330 Ω) air discharge contact discharge MIL STD883G-Method 3015-7	 ±18 ±18 ±18 ±18 ±25	kV
T_{stg}	Storage temperature range		-65 to +150	°C
T_j	Operating junction temperature range		-40 to +150	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
I_{RM}	Leakage current	V_{RM} = 5 V			0.5	µA
V_{BR}	Breakdown voltage between V_{BUS} and GND	I_R = 1 mA	6			V
V_{CL}	Clamping voltage	I_{PP} = 1 A, t_p = 8/20 µs Any I/O pin to GND			12	V
		I_{PP} = 5 A, t_p = 8/20 µs Any I/O pin to GND			17	V
$C_{i/o-GND}$	Capacitance between I/O and GND	V_R = 0 V, F= 1 MHz		0.85	1	pF
		V_R = 0 V, F= 825 MHz		0.6		
$\Delta C_{i/o-GND}$	Capacitance variation between I/O and GND			0.015		
$C_{i/o-i/o}$	Capacitance between I/O	V_R = 0 V, F= 1 MHz		0.42	0.5	pF
		V_R = 0 V, F= 825 MHz		0.3		
$\Delta C_{i/o-i/o}$	Capacitance variation between I/O			0.007		

Figure 2. Line capacitance versus line voltage (typical values)

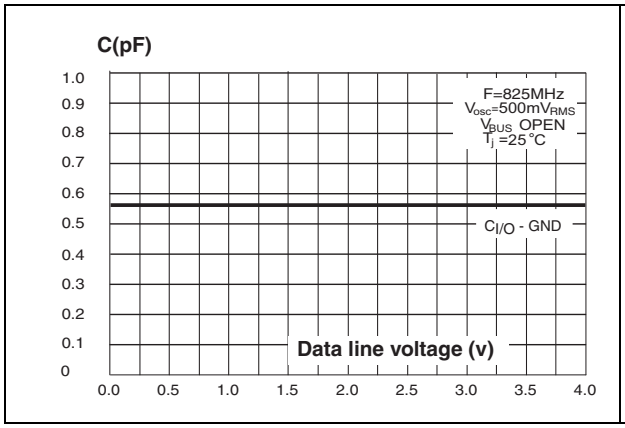


Figure 3. Line capacitance versus frequency (typical values)

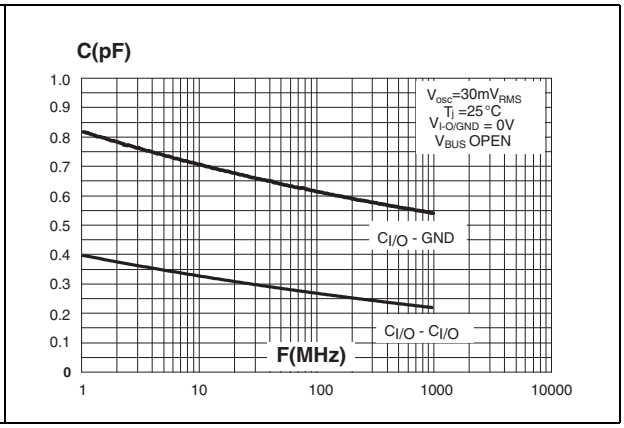


Figure 4. Relative variation of leakage current versus junction temperature (typical values)

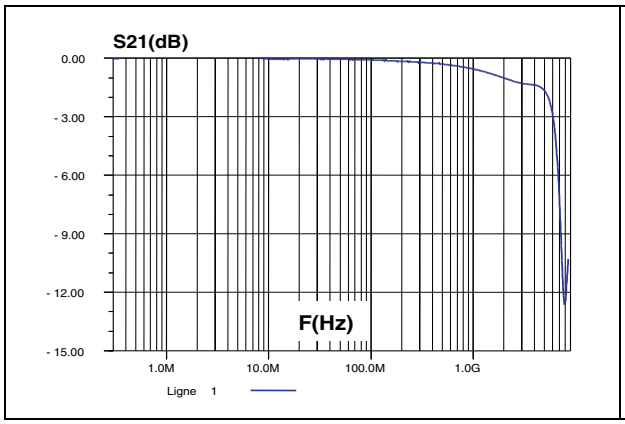


Figure 5. Frequency response

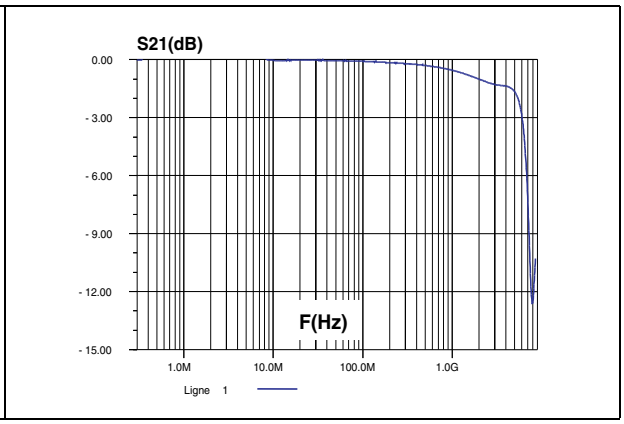


Figure 6. Remaining voltage after the DVIULC6-4SC6Y during positive ESD surge(1)

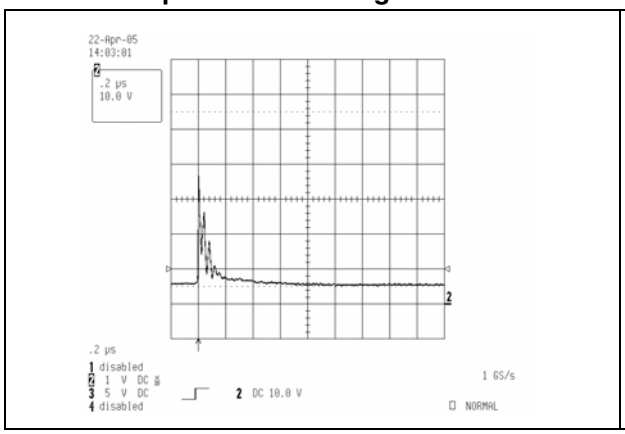
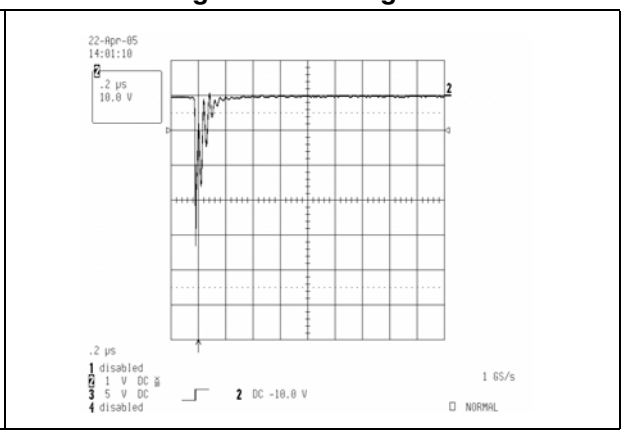


Figure 7. Remaining voltage after the DVIULC6-4SC6Y during negative ESD surge(1)



1. measurements were done with DVIULC-4SC6 in open circuit

Figure 8. Analog crosstalk results

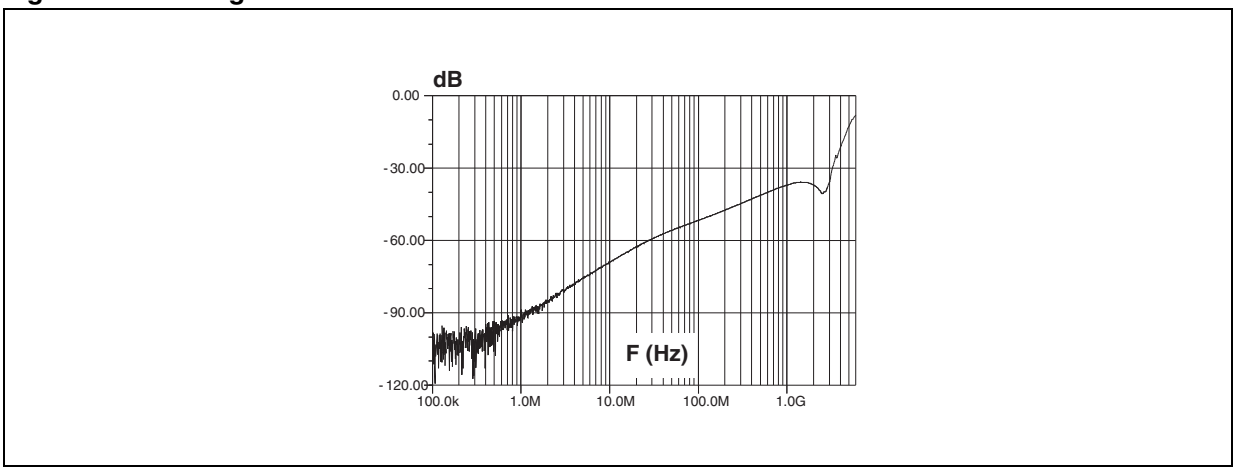


Figure 9. ISO 7637-2 pulse 3a response (V_S = -150 V)

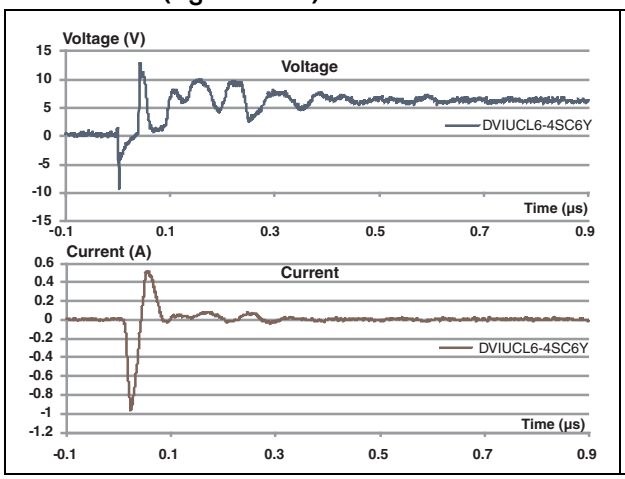
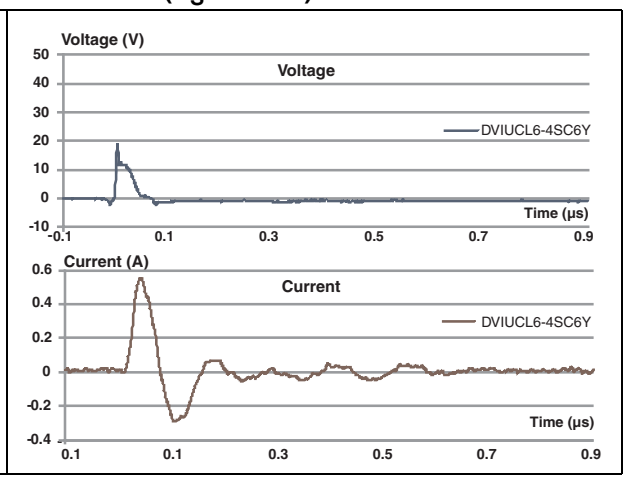


Figure 10. ISO 7637-2 pulse 3b response (V_S = 100 V)



2 Application examples

More information is available in the STMicroelectronics Application note AN2689 “Protection of automotive electronics from electrical hazards, guidelines for design and component selection”.

Figure 11. DVI/HDMI digital single link application

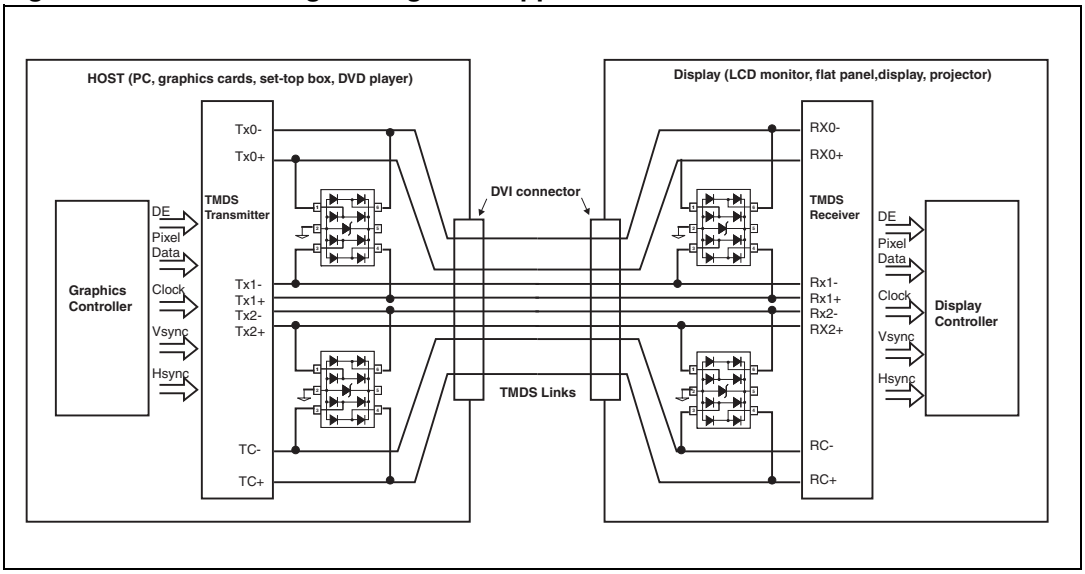
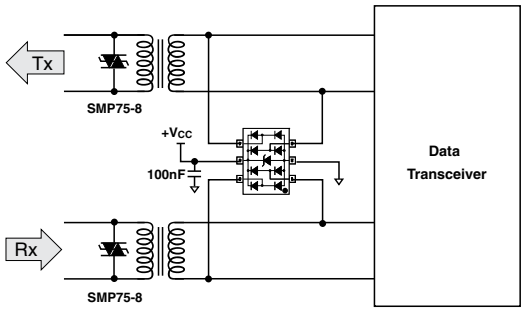


Figure 12. T1/E1/Ethernet protection



3 Technical information

3.1 Surge protection

The DVIULC6-4SC6Y is particularly optimized to perform ESD surge protection based on the rail to rail topology.

The clamping voltage V_{CL} can be calculated as follows:

$V_{CL}+ = V_{BUS} + V_F$, for positive surges

$V_{CL}- = - V_F$, for negative surges

with: $V_F = V_T + R_d.I_p$

(V_F = forward drop voltage) / (V_T = forward drop threshold voltage)

Calculation example

We can assume that the value of the dynamic resistance of the clamping diode is typically: R_d = 1.4 Ω and V_T = 1.2 V.

For an IEC 61000-4-2 surge Level 4 (Contact Discharge: V_g= 8 kV, R_g= 330 Ω), V_{BUS} = +5 V, and, in a first approximation, we assume that: $I_p = V_g / R_g$ = 24 A.

We find:

$V_{CL}+ = +39$ V

$V_{CL}- = -34$ V

Note: The calculations do not take into account phenomena due to parasitic inductances.

3.2 Surge protection application example

If we consider that the connections from the pin V_{BUS} to V_{CC} and from GND to PCB GND plane are two tracks 10 mm long and 0.5 mm wide, we can assume that the parasitic inductances, L_W of these tracks are about 6 nH. So when an IEC 61000-4-2 surge occurs, due to the rise time of this spike (tr = 1 ns), the voltage V_{CL} has an extra value equal to L_W.dI/dt.

The dI/dt is calculated as: $dI/dt = I_p/t_r$ = 24 A/ns for an IEC 61000-4-2 surge level 4 (contact discharge V_g = 8 kV, R_g = 330 Ω)

The over voltage due to the parasitic inductances is: $L_W.dI/dt = 6 \times 24 = 144$ V

By taking into account the effect of these parasitic inductances due to unsuitable layout, the clamping voltage will be:

$V_{CL}+ = +39 + 144 = 183$ V

$V_{CL}- = -34 - 144 = -178$ V

We can reduce as much as possible these phenomena with simple layout optimization.

This is the reason why some recommendations have to be followed (see *Section 3.3: How to ensure good ESD protection*).

3.3 How to ensure good ESD protection

While the DVIULC6-4SC6Y provides a high immunity to ESD surge, an efficient protection depends on the layout of the board. In the same way, with the rail to rail topology, the track from V_{BUS} pin to the power supply $+V_{CC}$, and from V_{BUS} pin to GND pin must be as short as possible to avoid over voltages due to parasitic phenomena (see *Figure 13* and *Figure 14* for layout considerations).

Figure 13. IESD behavior: parasitic phenomena due to unsuitable layout

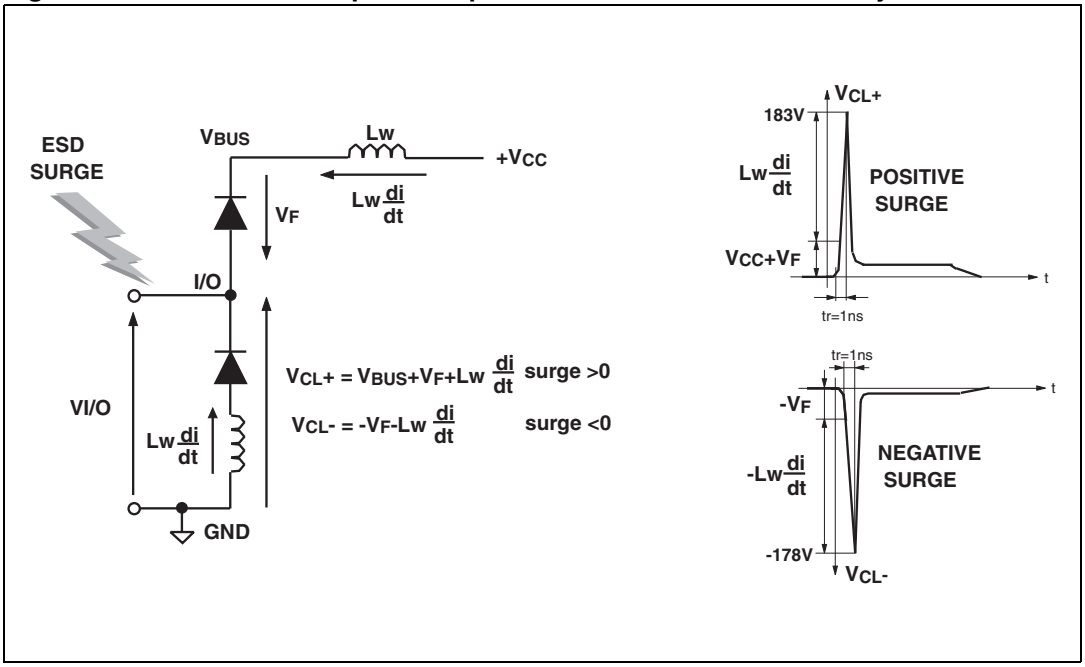


Figure 14. ESD behavior: layout optimization and addition of a 100 nF capacitor

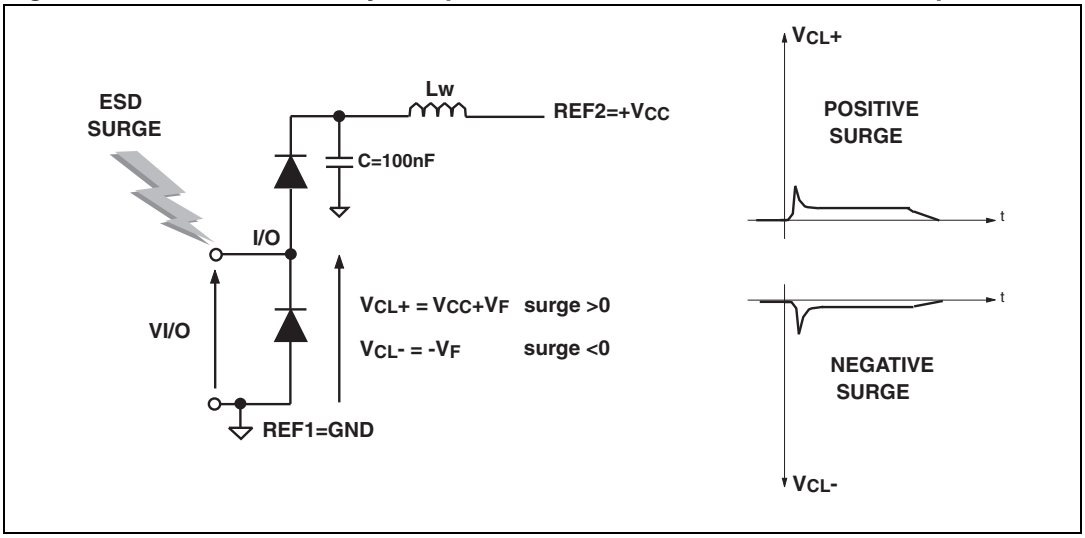
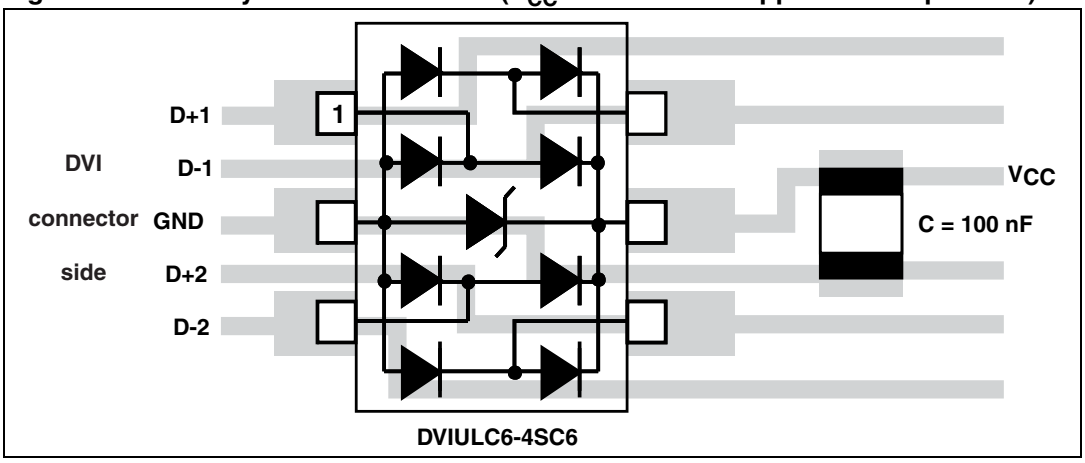


Figure 15. PCB layout considerations (V_{CC} connection is application dependent)



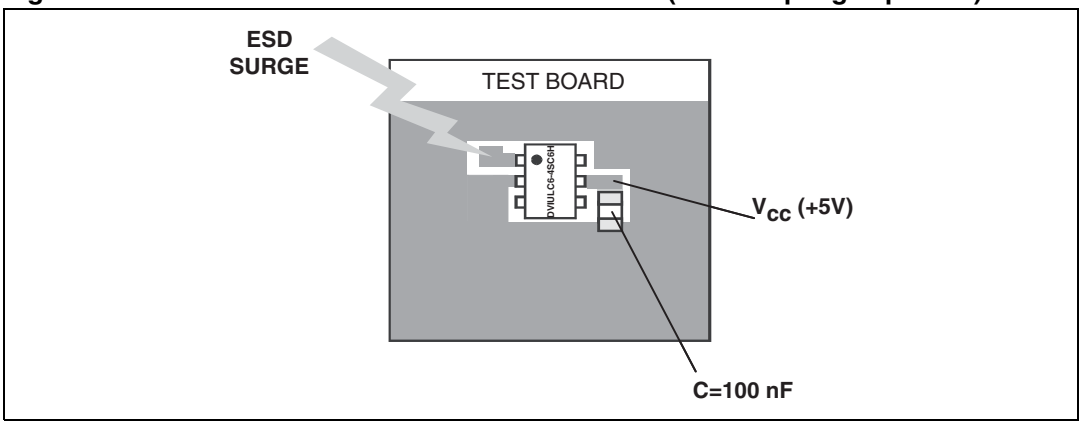
It's often harder to connect the power supply near to the DVIULC6-4SC6Y unlike the ground thanks to the ground plane that allows a short connection.

To ensure the same efficiency for positive surges when the connections can't be short enough, we recommend to put close to the DVIULC6-4SC6Y, between V_{BUS} and ground, a capacitance of 100 nF to prevent from these kinds of overfatigue disturbances (see *Figure 14* and *Figure 15*).

The addition of this capacitance will allow a better protection by providing a constant voltage during a surge.

Figure 16, *Figure 6*, and *Figure 7* show the improvement of the ESD protection according to the recommendations described in *Section 3.3*.

Figure 16. ESD behavior: measurement conditions (with coupling capacitor)

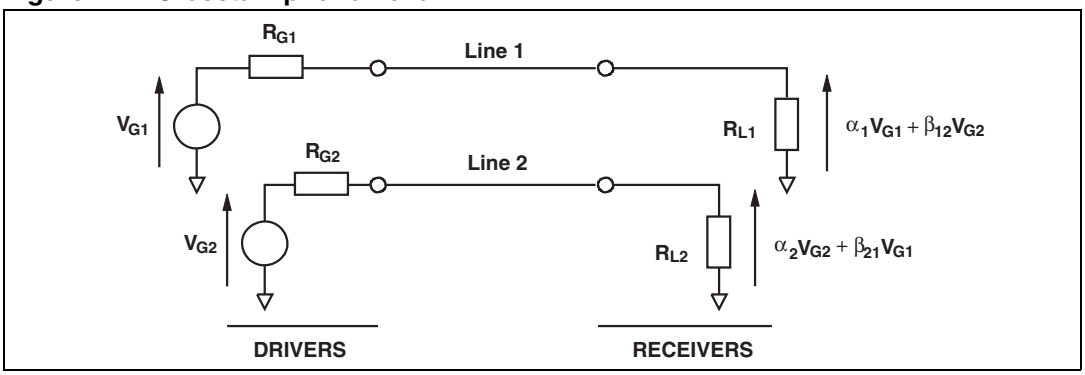


Important

An important precaution to take is to put the protection device as close as possible to the disturbance source (generally the connector).

3.4 Crosstalk behavior

Figure 17. Crosstalk phenomena



The crosstalk phenomena is due to the coupling between 2 lines. The coupling factor (β_{12} or β_{21}) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of line 1 on line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Figure 18. Analog crosstalk measurements

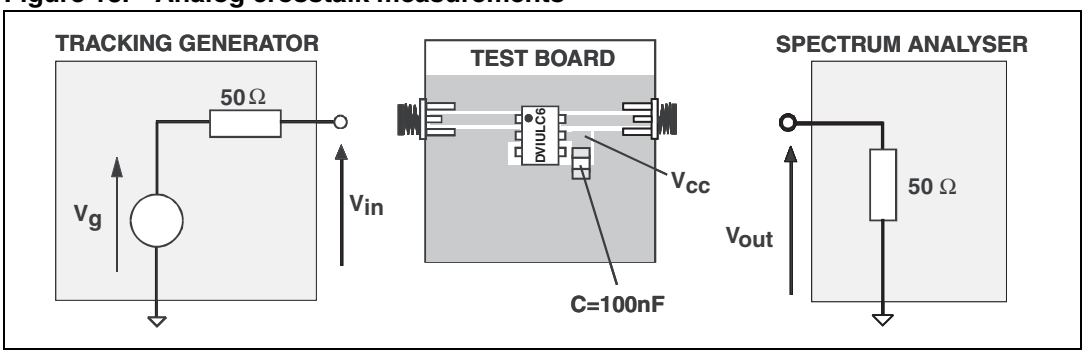


Figure 18 gives the measurement circuit for the analog application. In usual frequency range of analog signals (up to 240 MHz) the effect on disturbed line is less than -45 dB (see *Figure 8*).

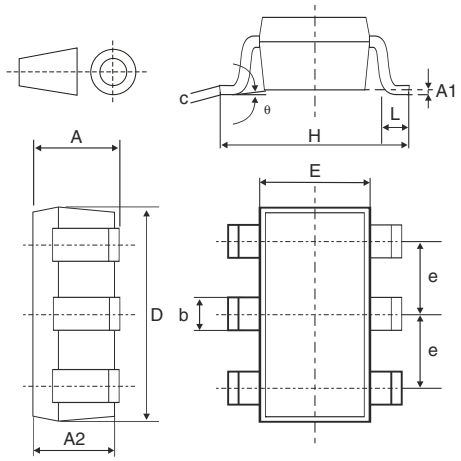
As the DVIULC6-4SC6Y is designed to protect high speed data lines, it must ensure a good transmission of operating signals. The frequency response (*Figure 5*) gives attenuation information and shows that the DVIULC6-4SC6Y is well suitable for data line transmission up to 1.65 Gb/s.

4 Package information

- Epoxy meets UL94, V0
- Lead-free package

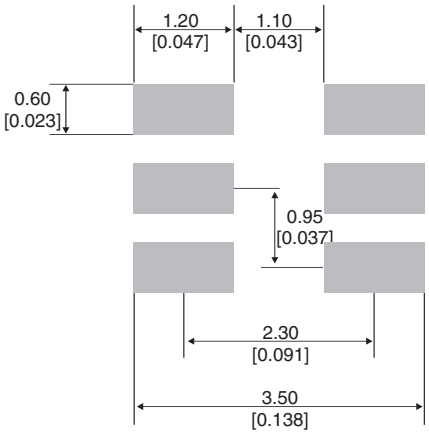
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. SOT23-6L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.15	0		0.006
A2	0.90		1.30	0.035		0.051
b	0.30		0.50	0.012		0.020
c	0.09		0.20	0.004		0.008
D	2.80		3.05	0.11		0.118
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.30		0.60	0.012		0.024
θ	0°		10°	0°		10°

Figure 19. Footprint - dimensions in mm (inches)



5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
DVIULC6-4SC6Y	DL4Y	SOT23-6L	16.7 mg	3000	Tape and reel

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
24-May-2011	1	First issue.
06-Sep-2012	2	Updated dimension A1 max., b min., and L min. in *Table 3*.

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