

Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Units		
Drain-Source Voltage	V_{DSS}	-20	V		
Gate-Source Voltage			V_{GSS}	±8	V
Continuous Drain Current (Note 5) V _{GS} = -4.5V	Steady State	T _A = 25°C T _A = 70°C	I _D	-330 -260	mA
	t<10s	$T_A = 25$ °C $T_A = 70$ °C	I _D	-400 -310	mA
Continuous Durin Courset (Nata 5) V	Steady State	T _A = 25°C T _A = 70°C	I _D	-250 -200	mA
Continuous Drain Current (Note 5) V _{GS} = -1.8V	t<10s	T _A = 25°C T _A = 70°C	I _D	-310 -240	mA
Pulsed Drain Current (Note 6)	I _{DM}	-800	mA		

Thermal Characteristics @TA = 25°C unless otherwise specified

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	Steady state	P_{D}	400	mW
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	6	310	°C/W
Thermal Resistance, Junction to Ambient (Note 5)	t<10s	$R_{ heta JA}$	220	°C/W
Operating and Storage Temperature Range		$T_{J_i}T_{STG}$	-55 to +150	°C

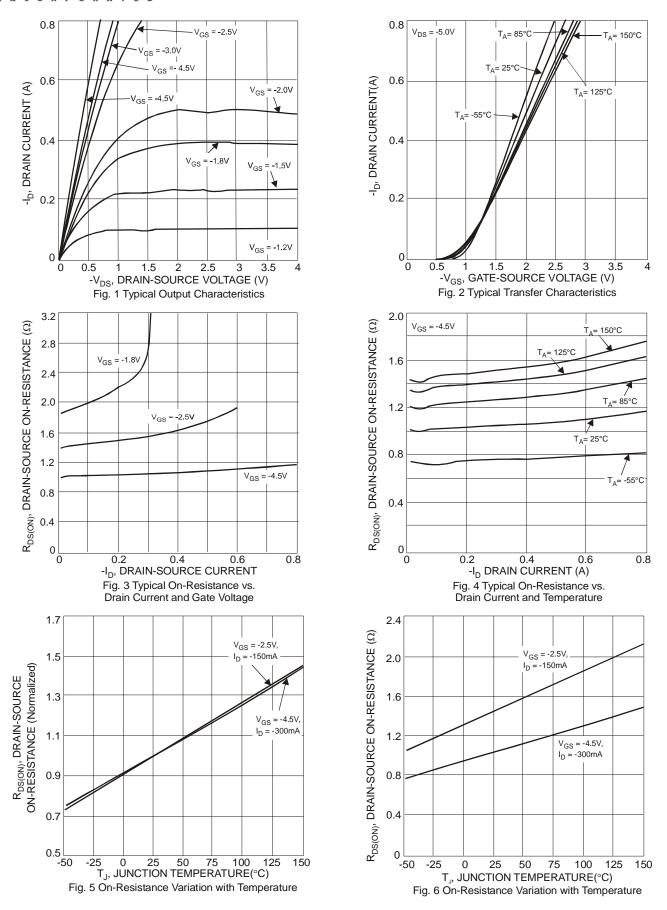
Electrical Characteristics @TA = 25°C unless otherwise specified

Characteristic		Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							•	
Drain-Source Breakdown Voltage		BV _{DSS}	-20	-	-	V	$V_{GS} = 0V, I_D = -250\mu A$	
Zara Cata Valtara Drain Correct	@T _c = 25°C	I _{DSS}	-	-	100	nA	V _{DS} = -16V, V _{GS} = 0V	
Zero Gate Voltage Drain Current			-	-	50		$V_{DS} = -5V, V_{GS} = 0V$	
Gate-Source Leakage		I _{GSS}	-	-	±100	nA	$V_{GS} = \pm 5V$, $V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)				•				
Gate Threshold Voltage		$V_{GS(th)}$	-0.4	-	-1.0	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
			1	1.2	1.9	Ω	$V_{GS} = -4.5V$, $I_D = -100mA$	
			-	1.5	2.4		$V_{GS} = -2.5V, I_D = -50mA$	
Static Drain-Source On-Resistance		R _{DS (ON)}	-	2.1	3.4		$V_{GS} = -1.8V, I_D = -20mA$	
			-	2.5	5		$V_{GS} = -1.5V, I_D = -10mA$	
			-	4.0	-		$V_{GS} = -1.2V, I_D = -1mA$	
Forward Transfer Admittance		Y _{fs}	100	450	-	mS	$V_{DS} = -5V, I_{D} = -125mA$	
Diode Forward Voltage		V _{SD}	-	-0.6	-1.0	V	$V_{GS} = 0V, I_{S} = -10mA$	
DYNAMIC CHARACTERISTICS (Note 8)								
Input Capacitance		C _{iss}	-	28.7	-	pF	V _{DS} = -15V, V _{GS} = 0V, -f = 1.0MHz	
Output Capacitance		Coss	-	4.2	-	pF		
Reverse Transfer Capacitance		C _{rss}	-	2.9	-	pF		
Gate Resistance		Rg	-	0.4	-	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$	
Total Gate Charge		Qg	-	0.4	-	nC		
Gate-Source Charge		Q _{gs}	-	0.08	-	nC	V _{GS} = -4.5V, V _{DS} =- 10V,	
Gate-Drain Charge		Q _{qd}	-	0.06	-	nC	$I_D = -250 \text{mA}$	
Turn-On Delay Time		t _{D(on)}	-	5.8	-	ns		
Turn-On Rise Time			-	5.7	-	ns	$V_{DD} = -15V, V_{GS} = -4.5V,$	
Turn-Off Delay Time		t _{D(off)}	-	31.1	-	ns	$R_G = 2\Omega, I_D = -200 \text{mA}$	
Turn-Off Fall Time		t _f	-	16.4	-	ns	7	

5. Device mounted on FR-4 PCB, with minimum recommended pad layout. Notes:

Device mounted on minimum recommended pad layout test board, 10µs pulse duty cycle = 1%.
Short duration pulse test used to minimize self-heating effect.
Guaranteed by design. Not subject to product testing.







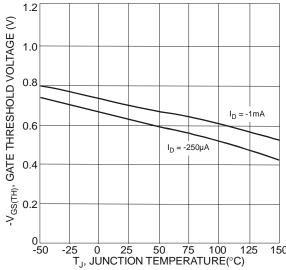
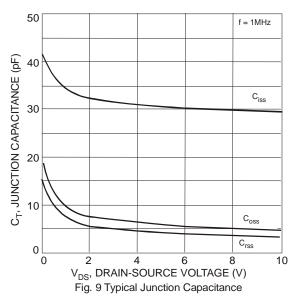
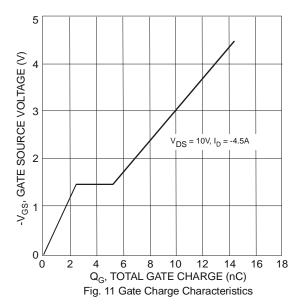
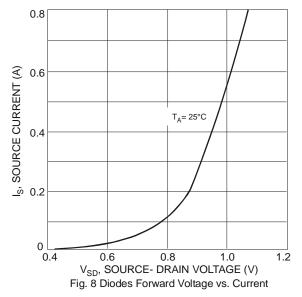
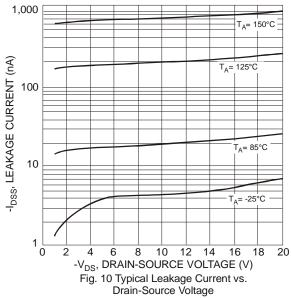


Fig. 7 Gate Threshold Variation vs. Ambient Temperature



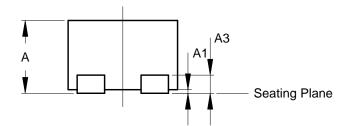


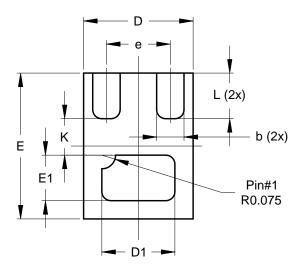






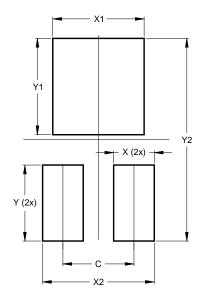
Package Outline Dimensions





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X2-DFN0806-3					
Dim	Min	Max	Тур		
Α	0.375	0.40	0.39		
A1	0	0.05	0.02		
А3	-	-	0.10		
b	0.10	0.20	0.15		
D	0.55	0.65	0.60		
D1	0.35	0.45	0.40		
E	0.75	0.85	0.80		
E1	0.20	0.30	0.25		
е	-	-	0.35		
K	-	-	0.20		
L	0.20	0.30	0.25		
All Dimensions in mm					

Suggested Pad Layout



Dimensions	Value (in mm)			
C	0.350			
Х	0.200			
X1	0.450			
X2	0.550			
Υ	0.375			
Y1	0.475			
Y2	1.000			



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