

Maximum Ratings (@T_A = +25°C, unless otherwise specified)

Characteristic	Symbol	Value	Unit	Conditions
Operating Supply Voltage	V _P - V _N	6.0	V	_
DC Voltage at any Channel Input	-	$(V_N - 0.5)$ to $(V_P + 0.5)$	V	_
Peak Pulse Current	I _{PP}	5	Α	8/20µs, Per Figure 3
ESD Protection – Contact Discharge	V _{ESD_Contact}	±8	kV	Standard IEC 61000-4-2
ESD Protection – Air Discharge	V_{ESD_Air}	±15	kV	Standard IEC 61000-4-2

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P _D	400	mW
Thermal Resistance, Junction to Ambient (Note 5)	$R_{ hetaJA}$	310	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-65 to +150	°C

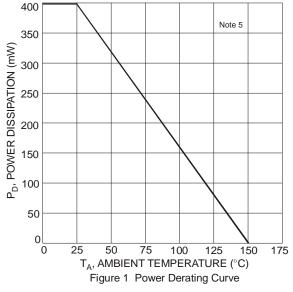
Electrical Characteristics (@T_A = +25°C, unless otherwise specified)

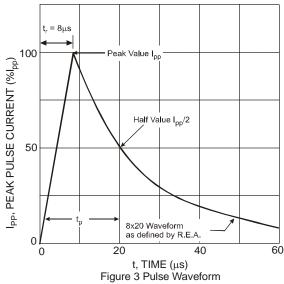
Characteristic	Symbol	Min	Тур	Max	Unit	Test Conditions
Operating Supply Voltage	V_P	_	3.3	5.5	V	_
Operating Supply Current (Note 6)	lρ	_	_	8.0	μΑ	$(V_P - V_N) = 3.3V$
Channel Leakage Current (Note 6)	I _R	_	±0.1	±1.0	μΑ	$V_P = 5V$, $V_N = 0V$
Reverse breakdown voltage	V_{BR}	6.0	_	_	V	$I_R = 1mA$
Clamping Voltage, Positive Transients	V _{CL1}	_	10.0	_	V	$I_{PP} = 1A, t_p = 8/20 \mu s$
Clamping Voltage, Negative Transients	V_{CL2}	_	-1.7	_	V	$I_{PP} = -1A$, $t_p = 8/20 \mu s$
Forward Voltage for Top Diode	V _{FD1}	0.60	0.80	0.95	V	$I_F = 8mA$, CH1 to V_P or CH2 to V_P
Forward Voltage for Bottom Diode	V_{FD2}	0.60	0.80	0.95	V	$I_F = 8mA$, V_N to CH1 or V_N to CH2
Dynamic Resistance	R _{DYN}	_	0.9	_	Ω	$I_{PP} = 1A, t_p = 8/20 \mu s$
Channel Input Capacitance	СТ	_	0.85	1.2	pF	$V_{IN} = 1.65V, V_P = 3.3V, V_N = 0V, f = 1MHz$

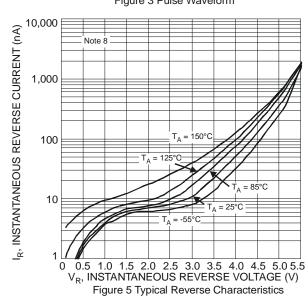
Notes:

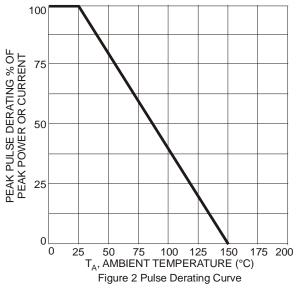
- 5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes, Inc. suggested pad layout AP02001, which can be found on our website at http://www.diodes.com.
- 6. Short duration pulse test used to minimize self-heating effect.
- 7. Measured from CH1 to Vn or CH2 to Vn.
- 8. Measured from $\ensuremath{V_P}$ to $\ensuremath{V_N}.$
- 9. For information on the impact of Diodes' USB 2.0 compatible ESD protectors on signal integrity including eye diagram plots, please refer to AN77 at the following URL: http://www.diodes.com/destools/appnote_dnote.html.

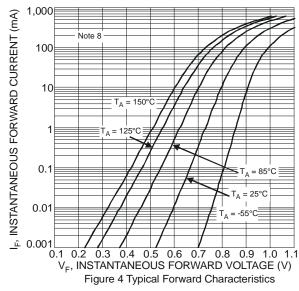












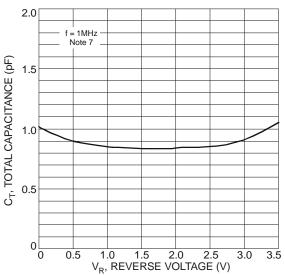
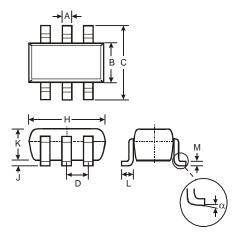


Figure 6 Typical Total Capacitance vs. Reverse Voltage



Package Outline Dimensions

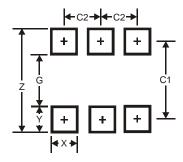
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SOT26				
Dim	Min	Max	Тур	
Α	0.35	0.50	0.38	
В	1.50	1.70	1.60	
С	2.70	3.00	2.80	
D	_	_	0.95	
Н	2.90	3.10	3.00	
J	0.013	0.10	0.05	
K	1.00	1.30	1.10	
L	0.35	0.55	0.40	
M	0.10	0.20	0.15	
α	0°	8°	_	
All Dimensions in mm				

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95



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