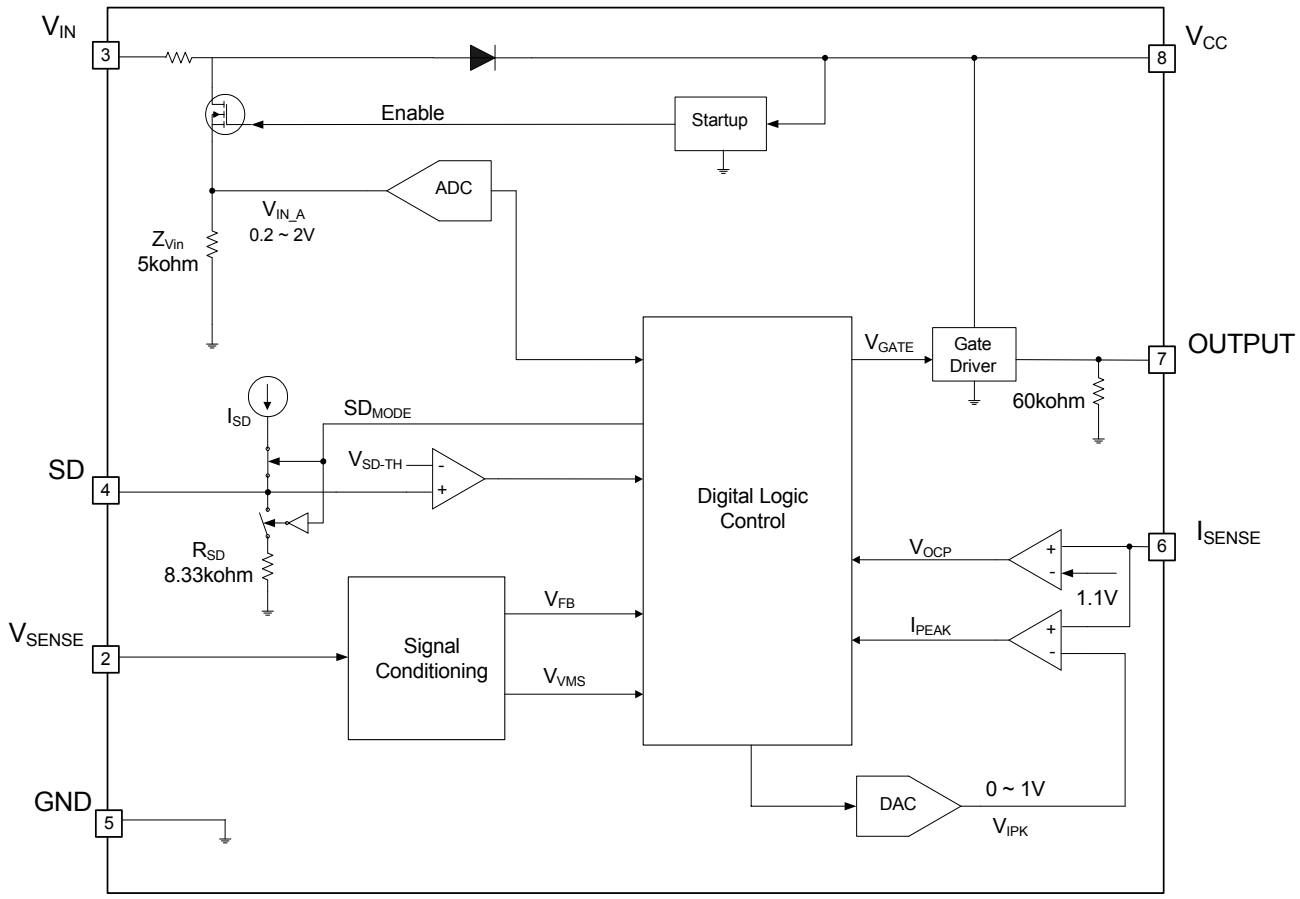
Contents

Features **1**
Description **1**
Contents **2**
Logic Block Diagram **3**
Functional Description **3**
Overview 3
Constant Current Operation 4
Valley Mode Switching 4
Protection Features 4
Understanding Primary Feedback 5
Constant Voltage Operation 6
Dynamic Load Transient 6
Variable Frequency Operation 6
Internal Loop Compensation 6
PFM Mode at Light Load 6
Pin Information **7**
Electrical Specifications **8**
Absolute Maximum Ratings 8
Electrical Characteristics **9**
Typical Performance Characteristics **10**
Ordering Information **12**
Ordering Code Definitions **12**
Packaging Information **13**
Physical Package Dimensions 13
Acronyms **14**
Document Conventions **14**
Units of Measure 14
Document History Page **15**
Sales, Solutions, and Legal Information **15**
Worldwide Sales and Design Support 15
Products 15
PSoC Solutions 15

Logic Block Diagram

Figure 2. Logic Block Diagram



Functional Description

Overview

The digital logic control block is the main block. All other blocks are inputs or outputs for the control block.

The control block receives signals to determine the input voltage (V_{IN}), output voltage (V_{SENSE}), temperature (SD), output operation (V_{CC}), and output current (I_{SENSE}).

The control block has three output controls; SD_{MODE} (shutdown mode control), DAC V_{IPK} (current control), and V_{GATE} (gate drive control).

The control block does not start operation until V_{CC} has charged to the startup threshold (V_{CCST}) as shown in Figure 3 on page 4. V_{CC} is charged through a diode connection from V_{IN}. V_{IN} receives a voltage from a rectified main power input. When V_{CC} is charged to V_{CCST}, the startup block enables the V_{IN} scaling resistance (Z_{Vin}) and the control block. The startup block also monitors the V_{CC} level and resets the system when V_{CC} decreases to a brown-out level (V_{CCUVL}). The reset initiates a startup sequence where V_{CC} is charged to V_{CCST} level through a diode connection from V_{IN}.

When the Z_{Vin} resistor is enabled, a voltage V_{IN_A} is measurable by an ADC. The output of the ADC is provided to the control block for auto-calculation of the $V_{IN}t_{ON}$ product where t_{ON} is the on time for the flyback MOSFET. After the voltage on V_{IN_A} is above the startup low voltage threshold ($V_{INSTLOW}$), the CY8CLEDAC01 commences an adaptive soft start function. The soft start control algorithm is applied at startup, during which the initial output pulses are small and gradually increase until the full pulse width is achieved.

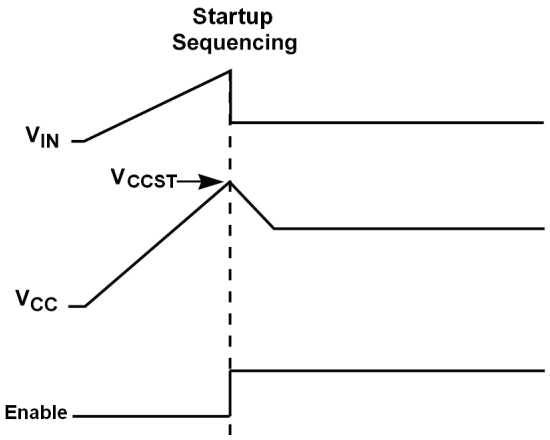
The V_{SENSE} pin connects to the Signal Conditioning block. The Signal Conditioning block provides two inputs to the control block: V_{FB} (Voltage Feed Back) and V_{VMS} (Voltage Valley Mode Switch). V_{FB} provides over-voltage protection and V_{CC} measurement. V_{VMS} is the valley switch detection. V_{FB} is monitored by the control block to determine if the output is over-voltage. When the control block detects an over-voltage condition, it enters a shutdown mode and wait for POR to re-initialize the system. V_{VMS} is monitored by the control block to determine when the power in the flyback MOSFET is at a minimum or in a 'valley'. The control block starts the next cycle at the 'valley' for maximum efficiency and minimum switching EMI.

The SD pin connects to two blocks; a switched current source (I_{SD}) and an analog comparator. These two blocks work together for OTP and optional OVP. For an OTP implementation, the SD pin can be connected to an external NTC component. The current source causes a voltage to be developed at the SD pin which causes the analog comparator's output to be high or low depending upon a 1 V comparator reference. If the voltage across the NTC is less than 1 V, the control block enters a shutdown mode and wait for POR to reinitialize the system.

The I_{SENSE} pin connects to circuitry composed of three blocks: DAC V_{IPK}, I_{PEAK} comparator, and V_{OCP} comparator. These three blocks work together for soft-start control, peak current detection, and over-current protection. The DAC V_{IPK} controls soft-start, minimizing stress associated with system startup. The I_{PEAK} comparator monitors the voltage at the I_{SENSE} pin. The voltage is generated by current flowing through a small external resistor (R_{ISENSE} - not shown). When the I_{SENSE} voltage reaches 1 V, the I_{PEAK} comparator asserts a high to the control block. The control block shuts off the output and waits for V_{VMS} detection; it then starts the next cycle. The V_{OCP} comparator provides primary side over-current protection. When the voltage on I_{SENSE} reaches 1.1 V, the V_{OCP} signal gets asserted. When over-current is detected, the control block enters a shutdown mode and waits for POR to re initialize the system.

The OUTPUT pin connects to the Gate Driver block. The Gate Driver connects to the OUTPUT pin that in turn connects to the flyback MOSFET gate pin (not shown). The OUTPUT pin is a digital control pin that switches between a high level (approximately V_{CC}) and a low level (approximately ground). The duration for high (t_{ON})and low (t_{OFF}) of the Gate Driver is a function of the control block operating upon its inputs: V_{IN},t_{ON}, V_{FB}, V_{VMS}, SD, I_{PEAK}, V_{OCP}, and V_{CC}.

Figure 3. Device Startup Sequence



Constant Current Operation

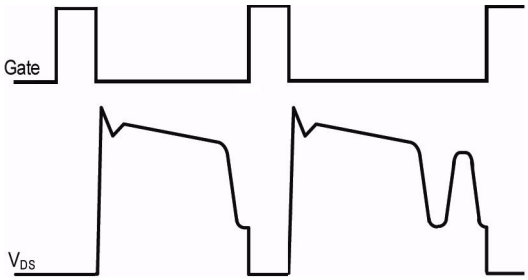
Constant current (CC) mode is the normal operating mode for LED lighting applications. CY8CLEDAC01 operates in CC mode when V_{SENSE} is set below $V_{SENSENOM}$. During this mode, the CY8CLEDAC01 regulates the output current at a constant level regardless of the output voltage. It operates in critical discontinuous conduction mode (CDCM) while in CC mode.

To achieve CC regulation, the CY8CLEDAC01 senses the load current indirectly through the primary current. The primary current is detected by the I_{SENSE} pin through a resistor from the MOSFET source to ground.

Valley Mode Switching

To reduce EMI and switching losses in the MOSFET, the CY8CLEDAC01 employs valley mode switching when operating in CDCM by switching at the lowest MOSFET V_{DS} (see Figure 4). It detects valleys in the MOSFET drain voltage indirectly through the V_{SENSE} pin. This voltage is provided by the auxiliary winding of the flyback transformer and represents a copy of the secondary side characteristics (see Figure 7 on page 6).

Figure 4. Valley Mode Switching



Turning on at the lowest V_{DS} generates lowest dV/dt; thus valley mode switching minimizes switching losses and reduces EMI. To limit the switching frequency range, the CY8CLEDAC01 can skip valleys (second cycle in Figure 4) when the switching frequency becomes too high.

The CY8CLEDAC01 supports valley mode switching in both CC and constant voltage (CV) modes of operation. This feature is superior to other quasi-resonant technologies which only support valley mode switching during constant voltage operation.

Protection Features

The CY8CLEDAC01 has full featured circuit protection not normally available with other primary-side control solutions.

The built-in protection features include OVP, OSCP, PCLP, CSSP, and OTP.

In an event a protection is triggered, V_{CC} discharges below V_{CCUVL} and causes a POR except in case of PCLP. The controller now initiates a new soft start cycle and continues to attempt start-up. It is unable to start up until the fault condition is removed.

Current Sense Resistor Short Protection (CSSP)

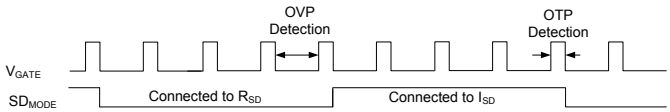
If the I_{SENSE} sense resistor is shorted, there is a potential danger of an over-current condition not being detected. The CY8CLEDAC01 has a separate circuit to detect this fault. This protection mode is triggered if the I_{SENSE} voltage is below 0.15V in CC mode and only at heavy loads in CV mode.

Over-Temperature Protection (OTP) and/or Output Over-Voltage Protection (OVP)

The shutdown (SD) pin along with an external NTC provides over-temperature protection. The SD pin also provides optional over-voltage protection by sensing a scaled auxiliary winding voltage from the flyback transformer using external components. The CY8CLEDAC01 switches between monitoring an

over-temperature fault and an over-voltage fault on the SD pin by using the SD_{MODE} control signal (shown in Figure 2 on page 3). For an over-temperature fault the voltage on the NTC is detected by connecting an internal current source to the pin. For an over-voltage fault the voltage on the SD pin is checked using an internal pulldown resistance R_{SD}. The measurements are made during the last V_{GATE} cycle in the measurement window to allow transients to settle.(shown in Figure 5)

Figure 5. SD Detection



When SD_{MODE} is high and the voltage across the NTC is lower than 1 V during normal operation or 1.2 V during start-up an OTP is triggered. When SD_{MODE} is low and the sensed voltage on the SD pin is higher than 1 V an OVP fault is triggered.

Output Over-Voltage Protection (OVP)

The CY8CLEDAC01 includes a function that protects against an output over-voltage. The output voltage is monitored by the V_{SENSE} pin. The protection is triggered if the voltage at this pin exceeds the over-voltage threshold $V_{SENSEMAX}$.

Peak Current Limit Protection (PCLP)

The I_{SENSE} pin of the CY8CLEDAC01 monitors the primary peak current. This enables cycle-by-cycle peak current control and limiting. When the primary peak current multiplied by the sense resistor value is greater than 1.1 V, an over-current condition is detected and the IC immediately turns off the MOSFET driver. During the next switching cycle, the driver sends out a regular switching pulse and turns off again if the OCP threshold is still reached. Normal switching resumes if the fault is removed and the OCP threshold is not reached.

Output Short Circuit Protection (OSCP)

The CY8CLEDAC01 includes a function that protects against an output short circuit. The output voltage is monitored by the V_{SENSE} pin. The protection is triggered if the voltage at this pin is below 0.22V.

Note When the V_{SENSE} is at this level, the controller is by default operating in CC mode and hence an over current condition cannot happen.

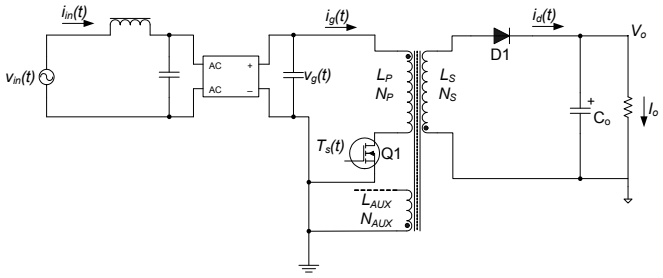
Single Point Fault Protection

The CY8CLEDAC01 detect a short on any of the following pins I_{SENSE}, V_{SENSE}, V_{CC}, OUTPUT, and SD. Therefore, any single point fault is protected against.

Understanding Primary Feedback

Figure 6 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_P. The rectifying diode D1 is reverse biased and the load current I_O is supplied by the secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

Figure 6. Simplified Flyback Converter



When operating in CC mode, to tightly regulate output current, information about the load current needs to be accurately sensed. To achieve CC regulation, this information can be derived indirectly by sensing the primary current.

When operating in CV mode, to tightly regulate output voltage, information about the output voltage and load current needs to be accurately sensed. In the DCM flyback converter, this information can be read through the auxiliary winding.

During the Q1 on time, the load current is supplied from the output filter capacitor C_O. The voltage across L_P is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

Equation 1

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_P}$$

At the end of on time, the current has ramped up to:

Equation 2

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_P}$$

This current represents a stored energy of:

Equation 3

$$E_g = \frac{L_P}{2} \times i_{g\_peak}(t)^2$$

When Q1 turns off, $i_g(t)$ in L_P forces a reversal of polarities on all windings. Ignoring the commutation time caused by the leakage inductance L_{KP} at the instant of turn-off, the primary current transfers to the secondary at a peak amplitude of:

Equation 4

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t)$$

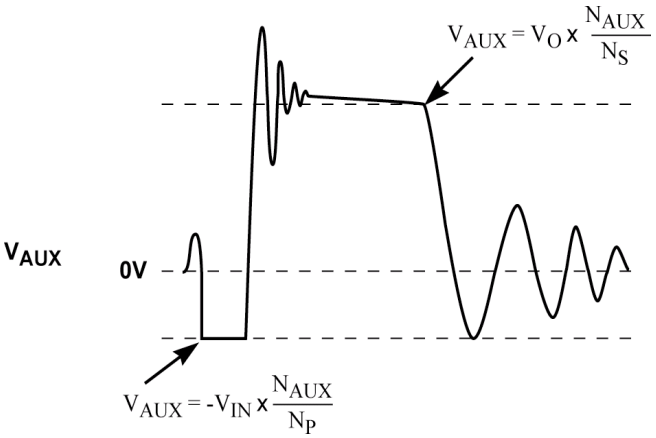
Assuming the secondary winding is master and the auxiliary winding is slave, the auxiliary voltage is given by:

Equation 5

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V)$$

and reflects the output voltage as shown in Figure 7.

Figure 7. Auxiliary Voltage Waveforms



The voltage at the load differs from the secondary voltage by a diode drop and IR losses. The diode drop is a function of current, as are IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV. Further, if the voltage can be read when the secondary current is small; for example, at the knee of the auxiliary waveform (see Figure 7), then ΔV is also small. With the CY8CLEDAC01, ΔV can be ignored.

The real time waveform analyzer in the CY8CLEDAC01 reads the auxiliary waveform information cycle by cycle. The part then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage and is used to regulate the output voltage.

Constant Voltage Operation

The CY8CLEDAC01 also features a CV mode. It operates in CV mode when V_{SENSE} is set between $V_{SENSENOM}$ and $V_{SENSEMAX}$. After soft start is completed, the digital control block measures the output conditions. It determines output power levels and adjusts the control system according to a light load or a heavy load. It uses CDCM or pulse width modulation (PWM) at high output power levels and switches to pulse frequency modulation (PFM) at light loads to minimize power dissipation. The PWM switching frequency is between 30 kHz and 130 kHz, depending on the line and load conditions.

Dynamic Load Transient

There are two components that compose the voltage drop during a load transient event.

$V_{DROP(sense)}$ is the drop in voltage before the V_{SENSE} signal is able to show a significant drop in output voltage. This is determined by V_{min} or the reference voltage at which a load transient is detected. The smaller the V_{min} is, the smaller is the drop in voltage.

Equation 6

$$V_{DROP(sense)} = \left(V_{SENSE(nom)} - V_{SENSE(\min)}\right) \times \frac{V_{OUT(design)}}{V_{SENSE(nom)}}$$

Remember that a smaller V_{min} is less tolerant of noise and can lead to signal distortion in V_{SENSE}.

The final drop in voltage is due to the time from when V_{SENSE} drops V_{min} to when the next V_{SENSE} signal appears. In the worst case condition this is how much voltage drops during the longest switching period.

Equation 7

$$V_{DROP(IC)} = \frac{I_{OUT} \times T_{P(NoLoad)}}{C_{OUT}}$$

A larger output capacitance in this case greatly reduces the $V_{DROP(IC)}$.

Variable Frequency Operation

An internal circuit checks for the falling edge of V_{SENSE} on every switching cycle. If the falling edge of V_{SENSE} is not detected, the off-time is extended until the falling edge of V_{SENSE} is detected. The maximum allowed transformer reset time for the CY8CLEDAC01 is 75 µs.

Internal Loop Compensation

The CY8CLEDAC01 incorporates an internal digital error amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20 dB of gain margin.

PFM Mode at Light Load

The CY8CLEDAC01 normally operates in a fixed frequency PWM or Critical Discontinuous Conduction Mode when I_{OUT} is greater than approximately 10 percent of the specified maximum load current. As the output load I_{OUT} is reduced, the on-time t_{ON} is decreased. The moment the load current drops below 10 percent of nominal, the controller transitions to pulse frequency modulation (PFM) mode. Thereafter, the on-time is modulated by the line voltage and the off-time is modulated by the load current. The device automatically returns to PWM mode when the load current increases.

Pin Information

Figure 8. Pin Diagram - 8-Pin SOIC CY8CLEDAC01

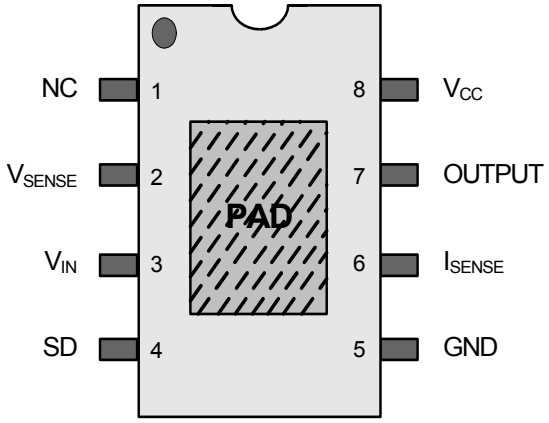


Table 1. Pin Description - 8-Pin SOIC CY8CLEDAC01

Pin No.	Name	Type	Description
1	NC	-	No connection
2	V_{SENSE}	Analog Input	Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.
3	V_{IN}	Analog Input	Sense signal input from the rectified line voltage. V_{IN} is used for line regulation. The input line voltage is scaled down using a resistor network, and is used for input under-voltage and over-voltage protection. This pin also provides the supply current to the IC during startup.
4	SD	Analog Input	External shutdown control. This pin should be pulled down to GND using a 20kΩ resistor if shutdown control is not required.
5	GND	Ground	Ground
6	I_{SENSE}	Analog Input	Primary current sense. Used for cycle by cycle peak current control.
7	OUTPUT	Output	Gate drive for external MOSFET switch
8	V_{CC}	Power Input	Power supply for the controller during normal operation. The controller starts up when V_{CC} reaches 12V (typical) and shuts down when the V_{CC} voltage is below 6V (typical). A decoupling capacitor should be connected between the V_{CC} pin and GND.
–	PAD	Exposed Pad	Connect exposed pad electrically to GND

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLEDAC01, of the PowerPSoC device family. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/powerpsoc. Specifications are valid for -40 °C ≤ T_A ≤ 85 °C and T_J ≤ 125 °C, except where noted.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. Not all user guidelines are production tested

Symbol	Description	Min	Typ	Max	Units	Notes
V_{CC}	DC supply voltage range	–0.3	–	18	V	pin 8, I_{CC} = 20 mA max
I_{CC}	DC supply current at V_{CC} pin	–	–	20	mA	pin 8
	Output pin voltage	–0.3	–	18	V	pin 7
	V_{SENSE} pin voltage	–0.7	–	4.0	V	pin 2, I_{SENSE} ≤ 10 mA
	V_{IN} pin voltage	–0.3	–	18	V	pin 3
	I_{SENSE} pin voltage	–0.3	–	4.0	V	pin 6
	SD pin voltage	–0.3	–	18	V	pin 4
P_D	Power Dissipation	–	–	526	mW	T_A ≤ 25 °C
$T_{J,max}$	Maximum Junction Temperature	–	–	125	°C	
T_{STG}	Storage Temperature	–65	–	150	°C	
T_{LEAD}	Lead Temperature	–	–	260	°C	During IR reflow for ≤ 15 seconds
θ_{JA}	Thermal Resistance Junction-to-ambient	–	–	160	°C/W	
V_{ESD}	ESD Voltage Rating	–	–	2000	V	as per JEDEC JESD22-A114
I_{LU}	Latch Up Current	–100	–	100	mA	as per JEDEC JESD78

Electrical Characteristics

V_{CC}=12V; –40 °C ≤ T_A ≤ 85 °C unless otherwise specified[1]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{IN} Section (pin 3)						
$V_{INSTLOW}$	Startup low voltage threshold	335	369	406	mV	T_A= 25 °C positive edge
I_{INST}	Startup current	–	10	15	µA	V_{IN} = 10V, C_{Vcc}=10 µF
Z_{IN}	Input impedance	–	5	–	kΩ	After startup
V_{SENSE} Section (pin 2)						
I_{BVS}	Input leakage current	–	–	1	µA	VSENSE = 2V
$V_{SENSENOM}$	Nominal voltage threshold	1.523	1.538	1.553	V	T_A = 25 °C negative edge
$V_{SENSEMAX}$	Output OVP threshold	1.790	1.846	1.900	V	T_A = 25 °C negative edge
OUTPUT Section (pin 7)						
$R_{DS(ON)LO}$	Output low level ON-Resistance	–	40	–	Ω	I_{SINK} = 5 mA
$R_{DS(ON)-HP}$	Output high level ON-Resistance	–	102	–	Ω	I_{SOURCE} = 5 mA
t_R	Rise time[2]	–	200	300	ns	T_A= 25 °C; CL = 330 pF; 10 percent to 90 percent
t_F	Fall time[2]	–	40	60	ns	T_A= 25 °C; CL=330 pF; 10 percent to 90 percent
F_{SWMAX}	Maximum switching frequency[3]	–	130	140	kHz	Any combination of line and loads
V_{CC} Section (pin 8)						
V_{CCMAX}	Maximum operating voltage	–	–	16	V	
V_{CCST}	Startup threshold	10.8	12	13.2	V	V_{CC} rising
V_{CCUVL}	Under-voltage lockout threshold	5.5	6.0	6.6	V	V_{CC} falling
I_{CC}	Operating current	–	3.5	–	mA	C_L= 330 pF; V_{SENSE} = 1.5 V
I_{SENSE} Section (pin 6)						
V_{PEAK}	Peak limit threshold		1.1		V	
V_{RSNS}	I_{SENSE} short protection reference	–	0.15	–	V	
V_{REGTH}	CC regulation threshold limit	–	1.0	–	V	
SD Section (pin 4)						
V_{SDTH}	Shutdown threshold	0.95	1.0	1.05	V	
V_{SDTHST}	Shutdown threshold in startup	–	1.2	–	V	
I_{BVSD}	Input leakage current	–	–	1.0	µA	V_{SD} = 1.0 V
R_{SD}	Pull-down resistance	7.916	8.333	8.750	kΩ	
I_{SD}	Pull-up current source	96	107	118	µA	

Notes
1. Adjust V_{CC} above the startup threshold before setting at 12 V.
2. These parameters are not 100 percent tested, guaranteed by design and characterization.
3. Operating frequency varies based on the line and load conditions, see Functional Description on page 3 for more details.

Typical Performance Characteristics

Figure 9. V_{CC} Supply Current versus V_{CC}

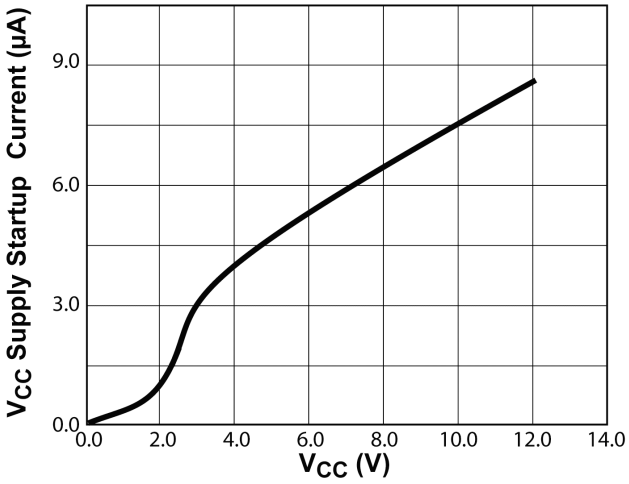


Figure 10. Switching Frequency Percent Change versus Temperature

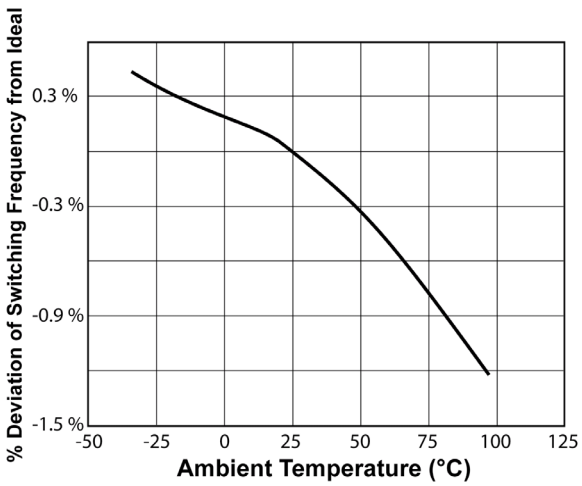


Figure 11. Startup Threshold versus Temperature

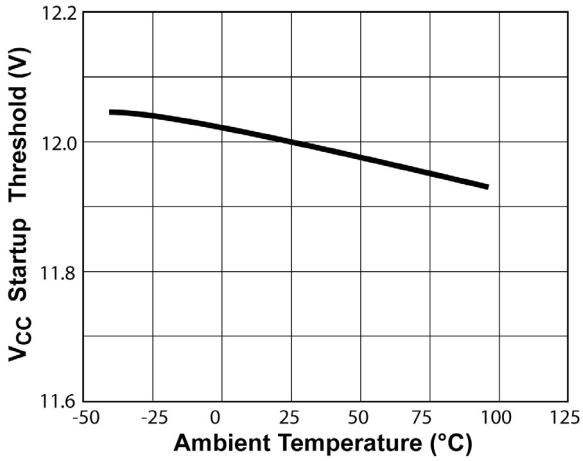


Figure 12. Internal Reference versus Temperature

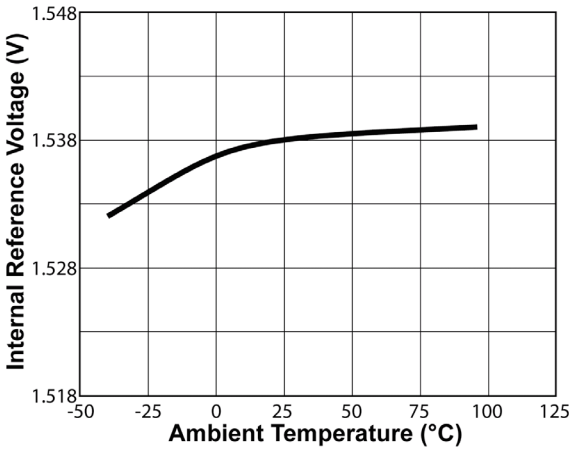
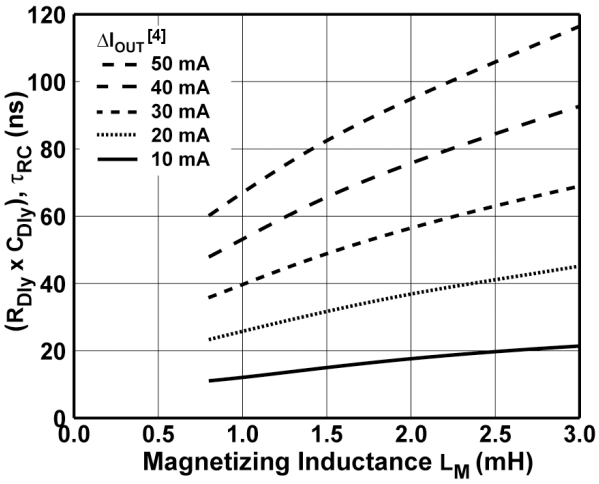


Figure 13. T_{ON} Compensation Chart

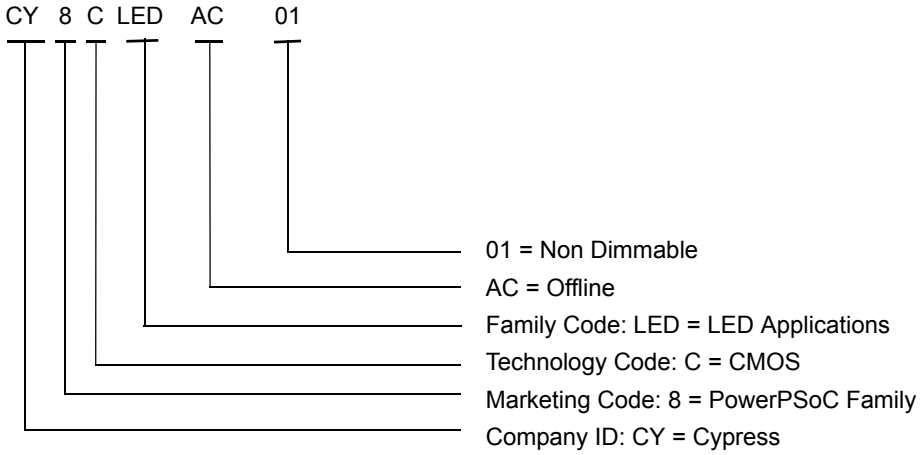


Note
4. ΔI_{OUT} refers to the difference in constant current limit between 264 VAC and 90 VAC when no R_{DLY} and C_{DLY} are applied.

Ordering Information

Ordering Code	No. of Pins	Package	Temperature Range
CY8CLEDAC01	8	SOIC	–40 °C to 85 °C

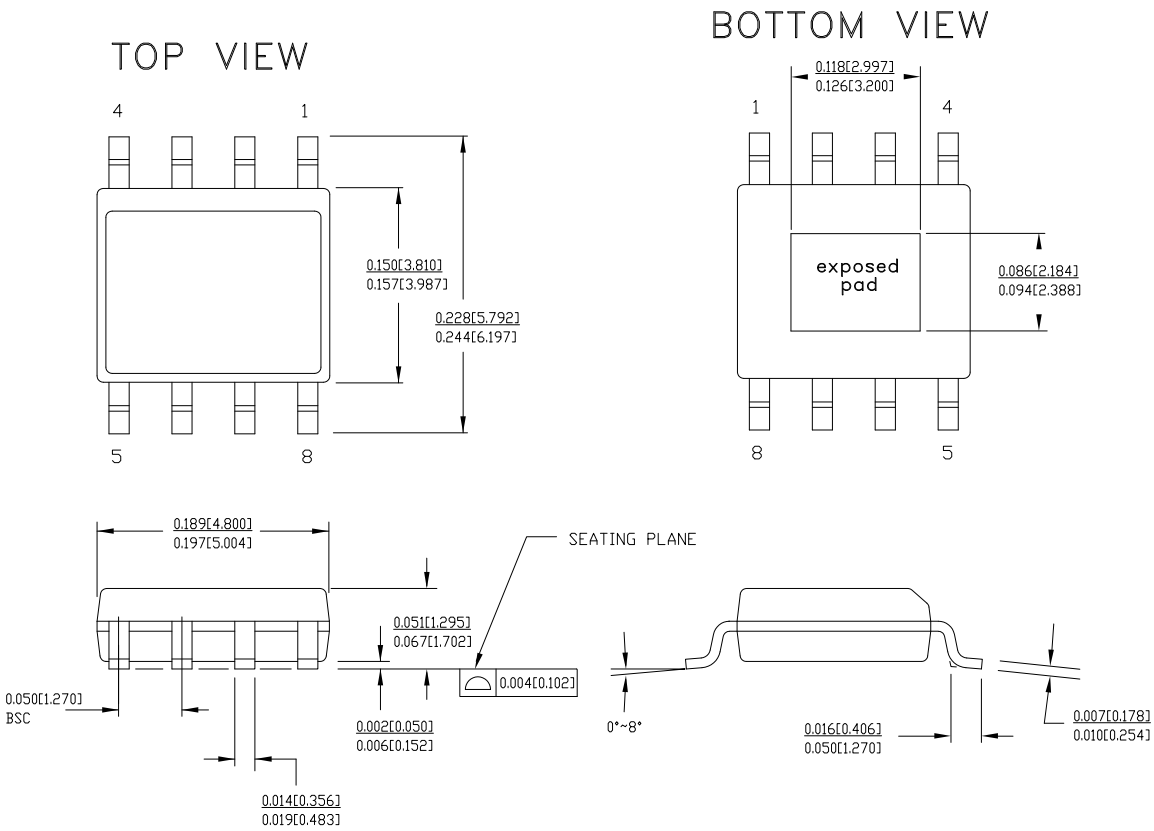
Ordering Code Definitions



Packaging Information

Physical Package Dimensions

Figure 14. 8-Pin Small Outline (SOIC) Package



1. DIMENSIONS IN INCHES[MM]
2. REFERENCE JEDEC MS-012F
3. PACKAGE WEIGHT 0.07 gm

001-54263 *A

Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
CDCM	critical discontinuous conduction mode
CSSP	current-sense resistor short protection
CV	constant voltage
OSCP	output short circuit protection
OTP	over-temperature protection
OVP	output over-voltage protection
PCLP	Peak current limit protection
PFM	pulse frequency modulation
PWM	pulse width modulation

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degrees Celsius	kbit	1024 bits	mA	milliampere
dB	decibels	kHz	kilohertz	ms	millisecond
Hz	Hertz	kΩ	kilohms	mV	millivolts
pp	peak-to-peak	MHz	megahertz	mA	milliwatts
σ	sigma:one standard deviation	MΩ	megaohms	nA	nanoamperes
V	volts	µA	microamperes	ns	nanoseconds
Ω	ohms	µF	microfarads	nV	nanovolts
KB	1024 bytes	µH	microhenrys	pA	picoamperes
ppm	parts per million	µs	microseconds	pF	picofarads
sps	samples per second	µV	microvolts	ps	picoseconds
W	watts	µVrms	microvolts root-mean-square	fF	femtofarads
A	amperes	µW	microwatts		

Document History Page

Document Title: CY8CLEDAC01 AC/DC Digital Current-Mode Controller for LED Lighting Document Number: 001-54122				
Revision	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2721319	KJV/AESA	06/19/2009	New data sheet
*A	2829351	KJV/PYRS	12/16/2009	Added Contents. Updated text in Features, Description, and Functional Description sections. Updated Electrical Specifications
*B	2901104	KJV/VED	03/29/2010	Release to web.
*C	3071772	KJV	10/26/2010	Updated "Pin Information" on page 7. Updated "Packaging Information" on page 13. Updated Template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturers' representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive
Clocks & Buffers
Interface
Lighting & Power Control
Memory
Optical & Image Sensing
PSoC
Touch Sensing
USB Controllers
Wireless/RF

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5