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## Product Portfolio

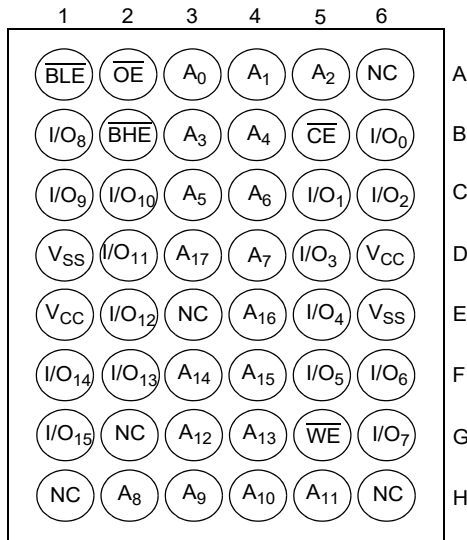
| Product       | Range        | V <sub>CC</sub> Range (V) |                    |                      | Speed (ns) | Power Dissipation              |     |                    |     |                               |     |
|---------------|--------------|---------------------------|--------------------|----------------------|------------|--------------------------------|-----|--------------------|-----|-------------------------------|-----|
|               |              |                           |                    |                      |            | Operating I <sub>CC</sub> (mA) |     |                    |     | Standby I <sub>SB2</sub> (μA) |     |
|               |              | f = 1 MHz                 |                    | f = f <sub>max</sub> |            |                                |     |                    |     |                               |     |
|               |              | Min                       | Typ <sup>[2]</sup> | Max                  |            | Typ <sup>[2]</sup>             | Max | Typ <sup>[2]</sup> | Max | Typ <sup>[2]</sup>            | Max |
| CY62147EV30LL | Automotive-A | 2.2                       | 3.0                | 3.6                  | 45 ns      | 2                              | 2.5 | 15                 | 20  | 1                             | 7   |
|               | Automotive-E | 2.2                       | 3.0                | 3.6                  | 55 ns      | 2                              | 3   | 15                 | 25  | 1                             | 20  |

### Note

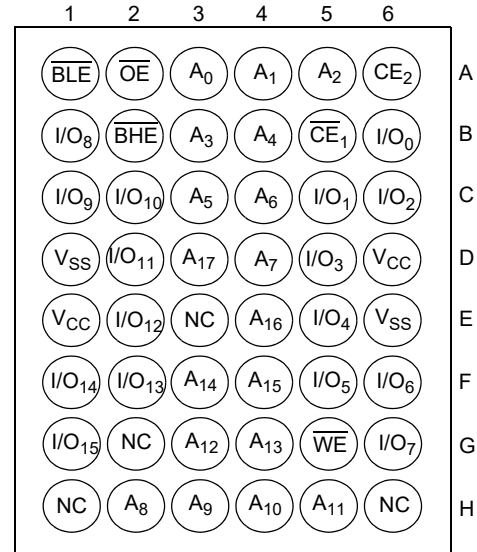
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Pin Configurations

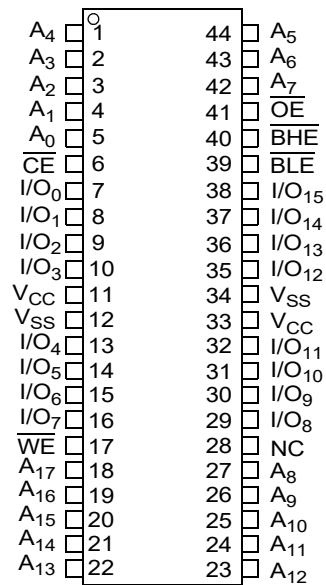
**Figure 1. 48-Ball VFBGA Pinout (Single Chip Enable)** <sup>[3, 4]</sup>



**Figure 2. 48-Ball VFBGA Pinout (Dual Chip Enable)** <sup>[3, 4]</sup>



**Figure 3. 44-Pin TSOP II Pinout** <sup>[3]</sup>



### Notes

3. NC pins are not connected on the die.
4. Pins H1, G2, and H6 in the BGA package are address expansion pins for 8Mb, 16Mb, and 32Mb, respectively.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to + 150 °C

Ambient temperature with power applied ..... -55 °C to + 125 °C

Supply voltage to ground potential ..... -0.3 V to + 3.9 V ( $V_{CCmax} + 0.3$  V)

DC voltage applied to outputs in High Z state <sup>[5, 6]</sup> ..... -0.3 V to 3.9 V ( $V_{CCmax} + 0.3$  V)

DC input voltage <sup>[5, 6]</sup> ..... -0.3 V to 3.9 V ( $V_{CCmax} + 0.3$  V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... >2001 V

Latch-up current ..... >200 mA

## Operating Range

| Device        | Range        | Ambient Temperature | $V_{CC}$ <sup>[7]</sup> |
|---------------|--------------|---------------------|-------------------------|
| CY62147EV30LL | Automotive-A | -40 °C to +85 °C    | 2.2 V to 3.6 V          |
|               | Automotive-E | -40 °C to +125 °C   |                         |

## Electrical Characteristics

Over the Operating Range

| Parameter                | Description                                   | Test Conditions                                                                                                                                                                            | 45 ns (Automotive-A) |                    |                | 55 ns (Automotive-E) |                    |                | Unit |
|--------------------------|-----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------------------|----------------|----------------------|--------------------|----------------|------|
|                          |                                               |                                                                                                                                                                                            | Min                  | Typ <sup>[8]</sup> | Max            | Min                  | Typ <sup>[8]</sup> | Max            |      |
| $V_{OH}$                 | Output HIGH voltage                           | $I_{OH} = -0.1$ mA                                                                                                                                                                         | 2.0                  | —                  | —              | 2.0                  | —                  | —              | V    |
|                          |                                               | $I_{OH} = -1.0$ mA, $V_{CC} \geq 2.70$ V                                                                                                                                                   | 2.4                  | —                  | —              | 2.4                  | —                  | —              | V    |
| $V_{OL}$                 | Output LOW voltage                            | $I_{OL} = 0.1$ mA                                                                                                                                                                          | —                    | —                  | 0.4            | —                    | —                  | 0.4            | V    |
|                          |                                               | $I_{OL} = 2.1$ mA, $V_{CC} = 2.70$ V                                                                                                                                                       | —                    | —                  | 0.4            | —                    | —                  | 0.4            | V    |
| $V_{IH}$                 | Input HIGH voltage                            | $V_{CC} = 2.2$ V to 2.7 V                                                                                                                                                                  | 1.8                  | —                  | $V_{CC} + 0.3$ | 1.8                  | —                  | $V_{CC} + 0.3$ | V    |
|                          |                                               | $V_{CC} = 2.7$ V to 3.6 V                                                                                                                                                                  | 2.2                  | —                  | $V_{CC} + 0.3$ | 2.2                  | —                  | $V_{CC} + 0.3$ | V    |
| $V_{IL}$                 | Input LOW voltage                             | $V_{CC} = 2.2$ V to 2.7 V                                                                                                                                                                  | -0.3                 | —                  | 0.6            | -0.3                 | —                  | 0.6            | V    |
|                          |                                               | $V_{CC} = 2.7$ V to 3.6 V                                                                                                                                                                  | -0.3                 | —                  | 0.8            | -0.3                 | —                  | 0.8            | V    |
| $I_{IX}$                 | Input leakage current                         | $GND \leq V_I \leq V_{CC}$                                                                                                                                                                 | -1                   | —                  | +1             | -4                   | —                  | +4             | μA   |
| $I_{OZ}$                 | Output leakage current                        | $GND \leq V_O \leq V_{CC}$ , output disabled                                                                                                                                               | -1                   | —                  | +1             | -4                   | —                  | +4             | μA   |
| $I_{CC}$                 | $V_{CC}$ operating supply current             | $f = f_{max} = 1/t_{RC}$ $V_{CC} = V_{CC(max)}$                                                                                                                                            | —                    | 15                 | 20             | —                    | 15                 | 25             | mA   |
|                          |                                               | $f = 1$ MHz $I_{OUT} = 0$ mA CMOS levels                                                                                                                                                   | —                    | 2                  | 2.5            | —                    | 2                  | 3              |      |
| $I_{SB1}$                | Automatic CE power-down current – CMOS inputs | $\overline{CE} \geq V_{CC} - 0.2$ V<br>$V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V,<br>$f = f_{max}$ (address and data only),<br>$f = 0$ (OE, BHE, BLE and WE),<br>$V_{CC} = 3.60$ V | —                    | 1                  | 7              | —                    | 1                  | 20             | μA   |
| $I_{SB2}$ <sup>[9]</sup> | Automatic CE power-down current – CMOS inputs | $\overline{CE} \geq V_{CC} - 0.2$ V,<br>$V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V,<br>$f = 0$ , $V_{CC} = 3.60$ V                                                                | —                    | 1                  | 7              | —                    | 1                  | 20             | μA   |

### Notes

- $V_{IL(min)}$  = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75$  V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to  $V_{CC(min)}$  and 200 μs wait time after  $V_{CC}$  stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C.
- Chip enable ( $\overline{CE}$ ) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the  $I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.

## Capacitance

For all packages.

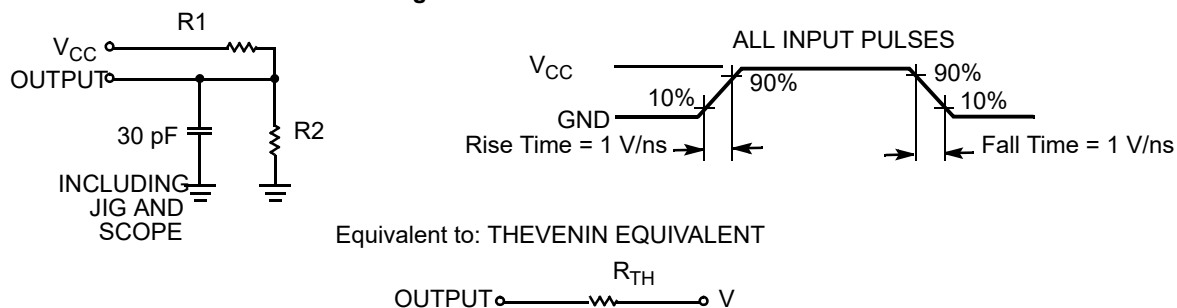
| Parameter <sup>[10]</sup> | Description        | Test Conditions                                                           | Max | Unit |
|---------------------------|--------------------|---------------------------------------------------------------------------|-----|------|
| C <sub>IN</sub>           | Input capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub> | 10  | pF   |
| C <sub>OUT</sub>          | Output capacitance |                                                                           | 10  | pF   |

## Thermal Resistance

| Parameter <sup>[10]</sup> | Description                              | Test Conditions                                                         | VFBGA Package | TSOP II Package | Unit |
|---------------------------|------------------------------------------|-------------------------------------------------------------------------|---------------|-----------------|------|
| Θ <sub>JA</sub>           | Thermal resistance (junction to ambient) | Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 42.10         | 55.52           | °C/W |
| Θ <sub>JC</sub>           | Thermal resistance (junction to case)    |                                                                         | 23.45         | 16.03           | °C/W |

## AC Test Load and Waveforms

Figure 4. AC Test Load and Waveforms



| Parameters      | 2.50 V | 3.0 V | Unit |
|-----------------|--------|-------|------|
| R1              | 16667  | 1103  | Ω    |
| R2              | 15385  | 1554  | Ω    |
| R <sub>TH</sub> | 8000   | 645   | Ω    |
| V <sub>TH</sub> | 1.20   | 1.75  | V    |

### Note

10. Tested initially and after any design or process changes that may affect these parameters.

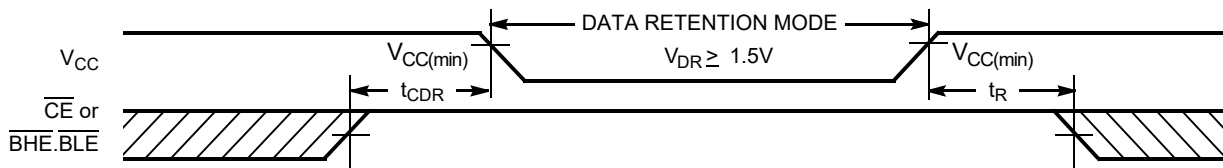
## Data Retention Characteristics

Over the Operating Range

| Parameter         | Description                          | Conditions                                                                                                                                        |                  | Min | Typ <sup>[11]</sup> | Max | Unit          |
|-------------------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|------------------|-----|---------------------|-----|---------------|
| $V_{DR}$          | $V_{CC}$ for data retention          |                                                                                                                                                   |                  | 1.5 | –                   | –   | V             |
| $I_{CCDR}^{[12]}$ | Data retention current               | $V_{CC} = 1.5\text{ V}$ ,<br>$\overline{CE} \geq V_{CC} - 0.2\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{ V}$ or<br>$V_{IN} \leq 0.2\text{ V}$ | Automotive-A     | –   | 0.8                 | 7   | $\mu\text{A}$ |
|                   |                                      |                                                                                                                                                   | Automotive-E     | –   | –                   | 12  |               |
| $t_{CDR}^{[13]}$  | Chip deselect to data retention time |                                                                                                                                                   |                  | 0   | –                   | –   | ns            |
| $t_R^{[14]}$      | Operation recovery time              |                                                                                                                                                   | CY62147EV30LL-45 | 45  | –                   | –   | ns            |
|                   |                                      |                                                                                                                                                   | CY62147EV30LL-55 | 55  | –                   | –   |               |

## Data Retention Waveform

Figure 5. Data Retention Waveform<sup>[15, 16]</sup>



### Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
12. Chip enable ( $\overline{CE}$ ) and byte enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) need to be tied to CMOS levels to meet the  $I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .
15. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device,  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $\overline{CE}_2$  such that when  $\overline{CE}_1$  is LOW and  $\overline{CE}_2$  is HIGH,  $\overline{CE}$  is LOW. For all other cases  $\overline{CE}$  is HIGH.
16.  $\overline{BHE.BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range

| Parameter <sup>[17, 18]</sup> | Description                                             | 45 ns (Automotive-A) |     | 55 ns (Automotive-E) |     | Unit |
|-------------------------------|---------------------------------------------------------|----------------------|-----|----------------------|-----|------|
|                               |                                                         | Min                  | Max | Min                  | Max |      |
| Read Cycle                    |                                                         |                      |     |                      |     |      |
| t <sub>RC</sub>               | Read cycle time                                         | 45                   | –   | 55                   | –   | ns   |
| t <sub>AA</sub>               | Address to data valid                                   | –                    | 45  | –                    | 55  | ns   |
| t <sub>OHA</sub>              | Data hold from address change                           | 10                   | –   | 10                   | –   | ns   |
| t <sub>ACE</sub>              | $\overline{CE}$ LOW to data valid                       | –                    | 45  | –                    | 55  | ns   |
| t <sub>DOE</sub>              | $\overline{OE}$ LOW to data valid                       | –                    | 22  | –                    | 25  | ns   |
| t <sub>LZOE</sub>             | $\overline{OE}$ LOW to Low Z <sup>[19]</sup>            | 5                    | –   | 5                    | –   | ns   |
| t <sub>HZOE</sub>             | $\overline{OE}$ HIGH to High Z <sup>[19, 20]</sup>      | –                    | 18  | –                    | 20  | ns   |
| t <sub>LZCE</sub>             | $\overline{CE}$ LOW to Low Z <sup>[19]</sup>            | 10                   | –   | 10                   | –   | ns   |
| t <sub>HZCE</sub>             | $\overline{CE}$ HIGH to High Z <sup>[19, 20]</sup>      | –                    | 18  | –                    | 20  | ns   |
| t <sub>PU</sub>               | $\overline{CE}$ LOW to power-up                         | 0                    | –   | 0                    | –   | ns   |
| t <sub>PD</sub>               | $\overline{CE}$ HIGH to power-down                      | –                    | 45  | –                    | 55  | ns   |
| t <sub>DBE</sub>              | $\overline{BLE/BHE}$ LOW to data valid                  | –                    | 45  | –                    | 55  | ns   |
| t <sub>LZBE</sub>             | $\overline{BLE/BHE}$ LOW to Low Z <sup>[19]</sup>       | 10                   | –   | 10                   | –   | ns   |
| t <sub>HZBE</sub>             | $\overline{BLE/BHE}$ HIGH to High Z <sup>[19, 20]</sup> | –                    | 18  | –                    | 20  | ns   |
| Write Cycle <sup>[21]</sup>   |                                                         |                      |     |                      |     |      |
| t <sub>WC</sub>               | Write cycle time                                        | 45                   | –   | 55                   | –   | ns   |
| t <sub>SCE</sub>              | $\overline{CE}$ LOW to write end                        | 35                   | –   | 40                   | –   | ns   |
| t <sub>AW</sub>               | Address setup to write end                              | 35                   | –   | 40                   | –   | ns   |
| t <sub>HA</sub>               | Address hold from write end                             | 0                    | –   | 0                    | –   | ns   |
| t <sub>SA</sub>               | Address setup to write start                            | 0                    | –   | 0                    | –   | ns   |
| t <sub>PWE</sub>              | $\overline{WE}$ pulse width                             | 35                   | –   | 40                   | –   | ns   |
| t <sub>BW</sub>               | $\overline{BLE/BHE}$ LOW to write end                   | 35                   | –   | 40                   | –   | ns   |
| t <sub>SD</sub>               | Data setup to write end                                 | 25                   | –   | 25                   | –   | ns   |
| t <sub>HD</sub>               | Data hold from write end                                | 0                    | –   | 0                    | –   | ns   |
| t <sub>HZWE</sub>             | $\overline{WE}$ LOW to High Z <sup>[19, 20]</sup>       | –                    | 18  | –                    | 20  | ns   |
| t <sub>LZWE</sub>             | $\overline{WE}$ HIGH to Low Z <sup>[19]</sup>           | 10                   | –   | 10                   | –   | ns   |

### Notes

17. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [Figure 4 on page 6](#).

18. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application note [AN13842](#) for further clarification.

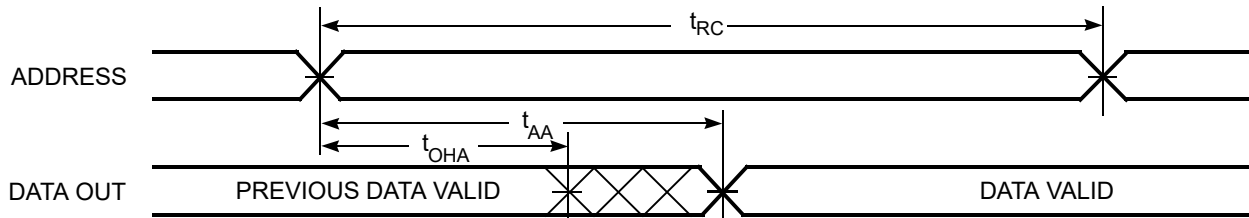
19. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.

20.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.

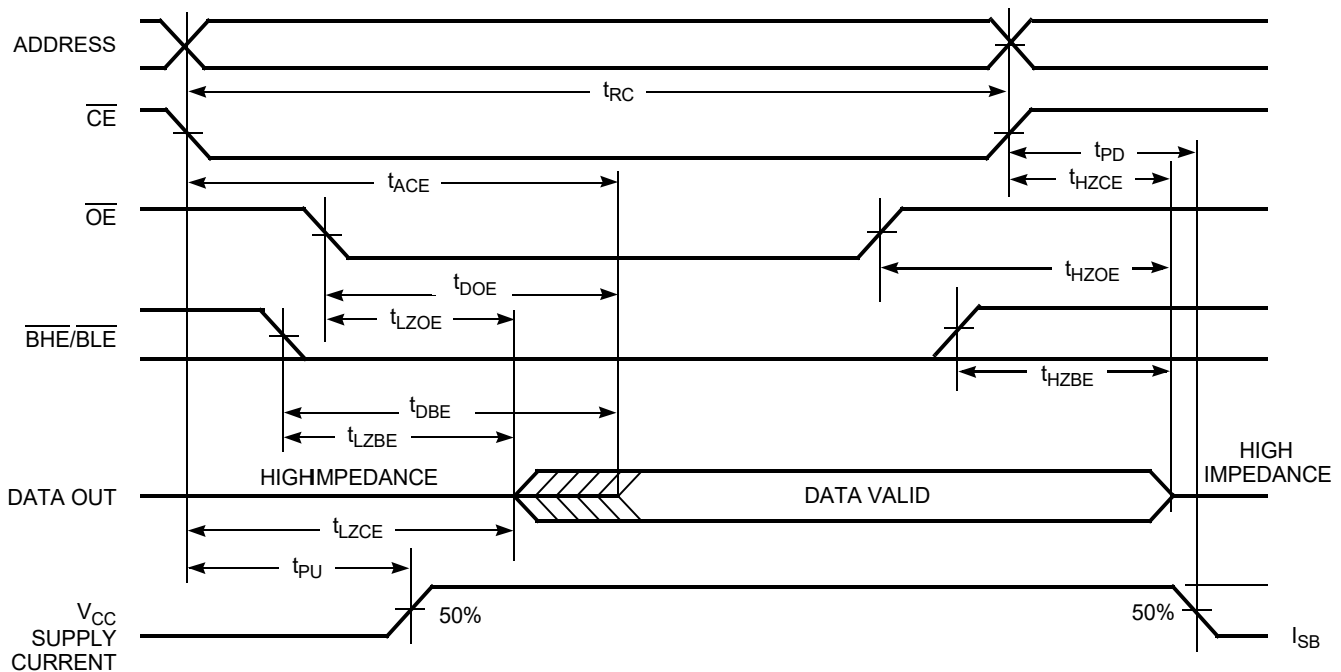
21. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ , BHE, BLE, or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

**Figure 6. Read Cycle No. 1: Address Transition Controlled** [22, 23]



**Figure 7. Read Cycle No. 2:  $\overline{\text{OE}}$  Controlled** [23, 24, 25]



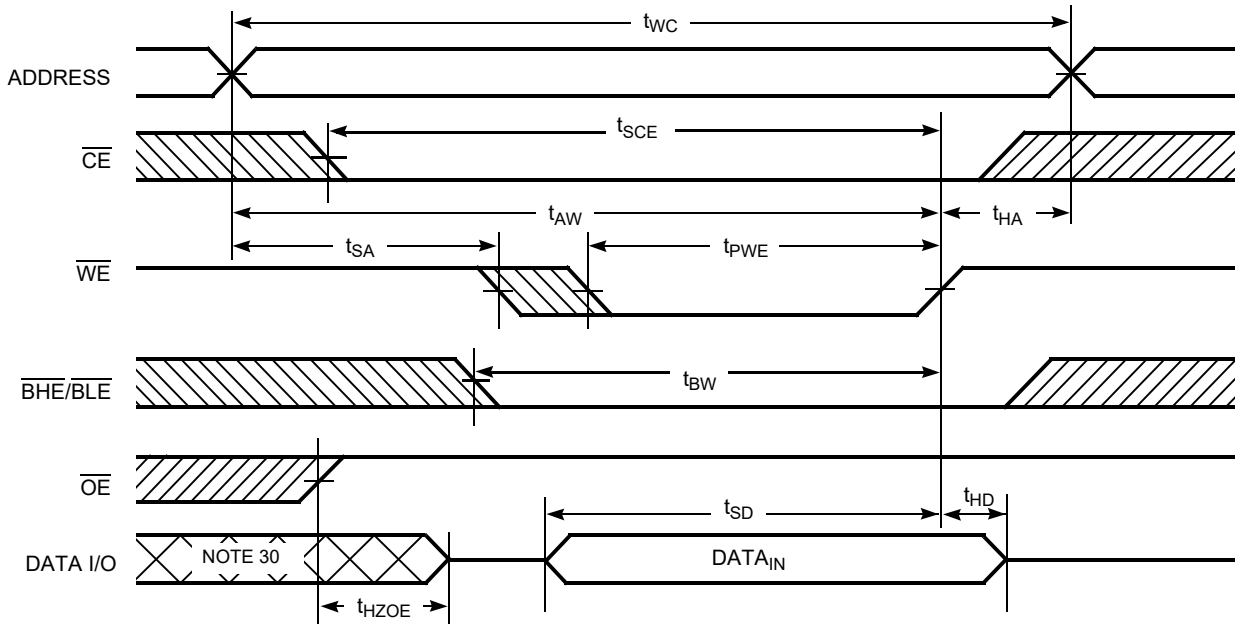
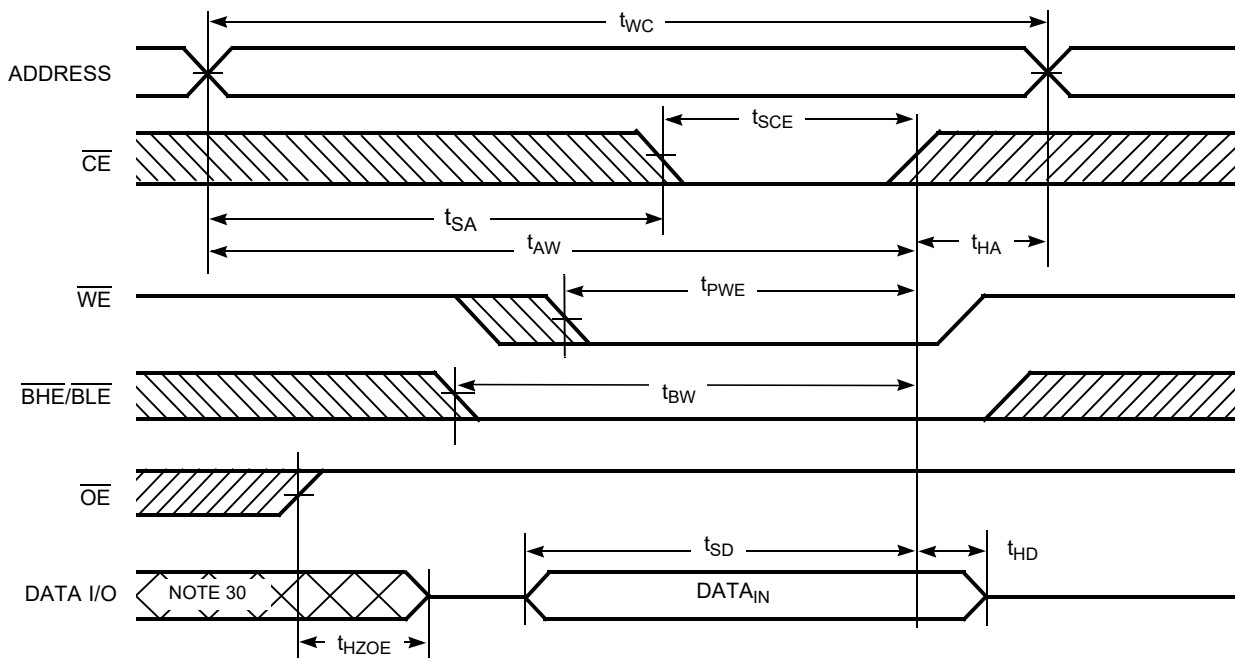
### Notes

22. The device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$ , or both =  $V_{\text{IL}}$ .

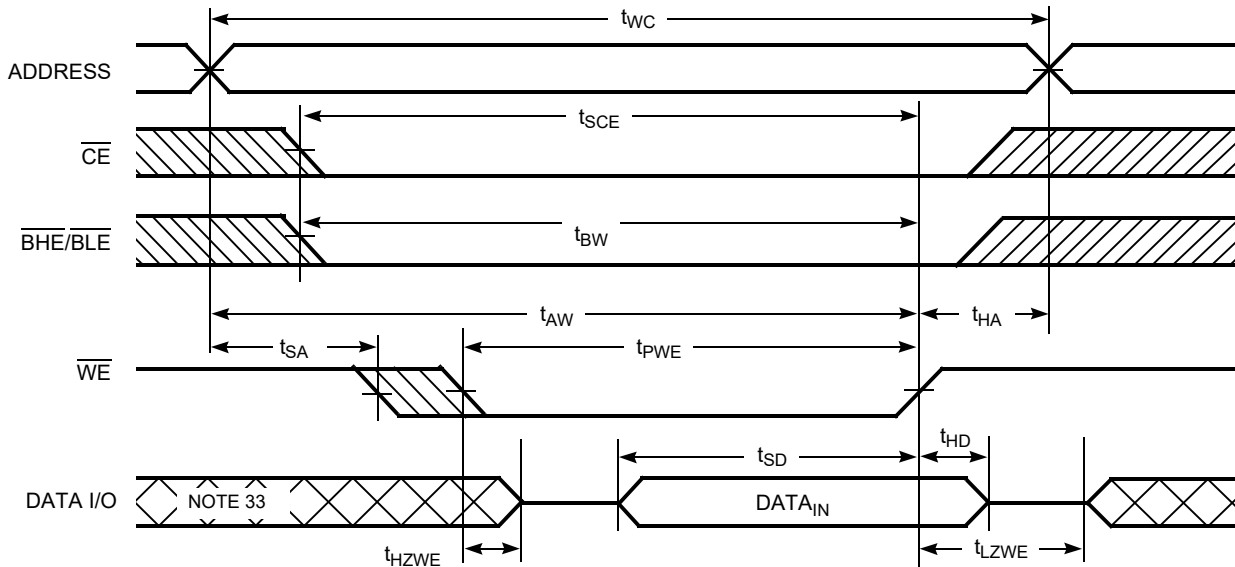
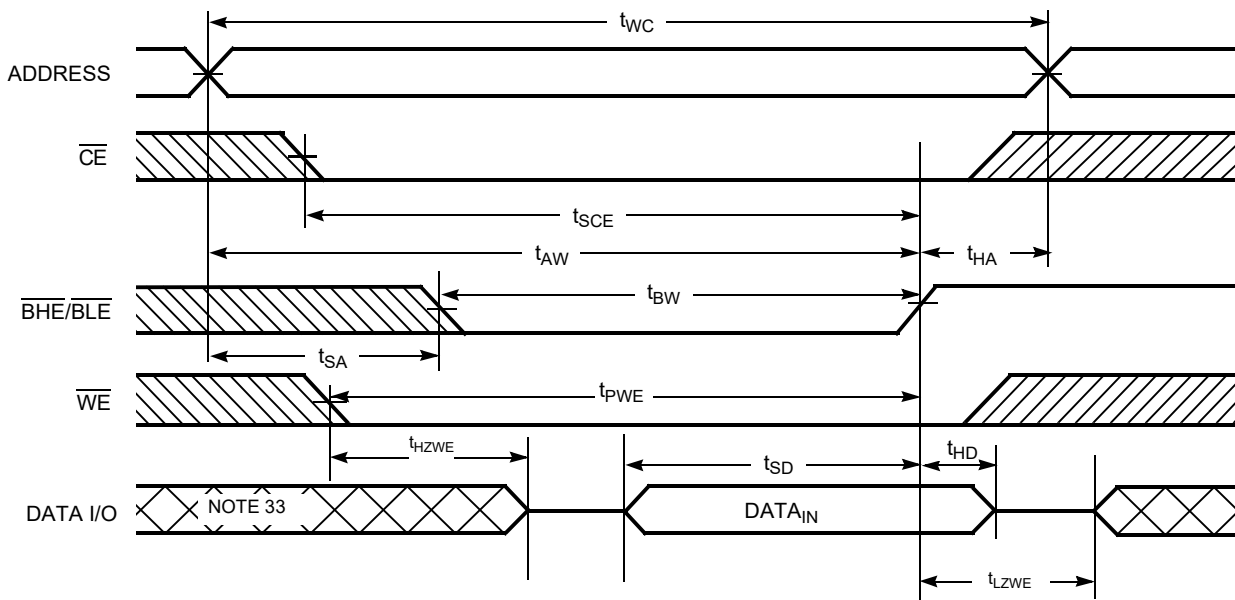
23.  $\overline{\text{WE}}$  is HIGH for read cycle.

24. BGA packaged device is offered in single CE and dual CE options. In this datasheet, for a dual CE device,  $\overline{\text{CE}}$  refers to the internal logical combination of  $\overline{\text{CE}}_1$  and  $\overline{\text{CE}}_2$  such that when  $\overline{\text{CE}}_1$  is LOW and  $\overline{\text{CE}}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW. For all other cases  $\overline{\text{CE}}$  is HIGH.

25. Address valid before or similar to CE and BHE, BLE transition LOW.

**Switching Waveforms (continued)**
**Figure 8. Write Cycle No. 1:  $\overline{\text{WE}}$  Controlled** [26, 27, 28, 29]

**Figure 9. Write Cycle No. 2:  $\overline{\text{CE}}$  Controlled** [26, 27, 28, 29]

**Notes**

26. BGA packaged device is offered in single CE and dual CE options. In this datasheet, for a dual CE device,  $\overline{\text{CE}}$  refers to the internal logical combination of  $\overline{\text{CE}}_1$  and  $\overline{\text{CE}}_2$  such that when  $\overline{\text{CE}}_1$  is LOW and  $\overline{\text{CE}}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW. For all other cases  $\overline{\text{CE}}$  is HIGH.
27. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{IL}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$ , or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
28. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
29. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}} = V_{IH}$ , the output remains in a high impedance state.
30. During this period, the I/Os are in output state. Do not apply input signals.

**Switching Waveforms (continued)**
**Figure 10. Write Cycle No. 3:  $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW [31, 32]**

**Figure 11. Write Cycle No. 4:  $\overline{\text{BHE/BLER}}$  Controlled,  $\overline{\text{OE}}$  LOW [31, 32]**

**Notes**

31. BGA packaged device is offered in single CE and dual CE options. In this datasheet, for a dual CE device,  $\overline{\text{CE}}$  refers to the internal logical combination of  $\overline{\text{CE}}_1$  and  $\overline{\text{CE}}_2$  such that when  $\overline{\text{CE}}_1$  is LOW and  $\overline{\text{CE}}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW. For all other cases  $\overline{\text{CE}}$  is HIGH.

32. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}} = V_{IH}$ , the output remains in a high-impedance state.

33. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

| $\overline{CE}$ [34, 35] | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | I/Os                                                              | Mode                | Power                |
|--------------------------|-----------------|-----------------|------------------|------------------|-------------------------------------------------------------------|---------------------|----------------------|
| H                        | X               | X               | X                | X                | High Z                                                            | Deselect/power-down | Standby ( $I_{SB}$ ) |
| L                        | X               | X               | H                | H                | High Z                                                            | Deselect/power-down | Standby ( $I_{SB}$ ) |
| L                        | H               | L               | L                | L                | Data out ( $I/O_0$ – $I/O_{15}$ )                                 | Read                | Active ( $I_{CC}$ )  |
| L                        | H               | L               | H                | L                | Data out ( $I/O_0$ – $I/O_7$ );<br>$I/O_8$ – $I/O_{15}$ in High Z | Read                | Active ( $I_{CC}$ )  |
| L                        | H               | L               | L                | H                | Data out ( $I/O_8$ – $I/O_{15}$ );<br>$I/O_0$ – $I/O_7$ in High Z | Read                | Active ( $I_{CC}$ )  |
| L                        | H               | H               | L                | L                | High Z                                                            | Output disabled     | Active ( $I_{CC}$ )  |
| L                        | H               | H               | H                | L                | High Z                                                            | Output disabled     | Active ( $I_{CC}$ )  |
| L                        | H               | H               | L                | H                | High Z                                                            | Output disabled     | Active ( $I_{CC}$ )  |
| L                        | L               | X               | L                | L                | Data in ( $I/O_0$ – $I/O_{15}$ )                                  | Write               | Active ( $I_{CC}$ )  |
| L                        | L               | X               | H                | L                | Data in ( $I/O_0$ – $I/O_7$ );<br>$I/O_8$ – $I/O_{15}$ in High Z  | Write               | Active ( $I_{CC}$ )  |
| L                        | L               | X               | L                | H                | Data in ( $I/O_8$ – $I/O_{15}$ );<br>$I/O_0$ – $I/O_7$ in High Z  | Write               | Active ( $I_{CC}$ )  |

### Notes

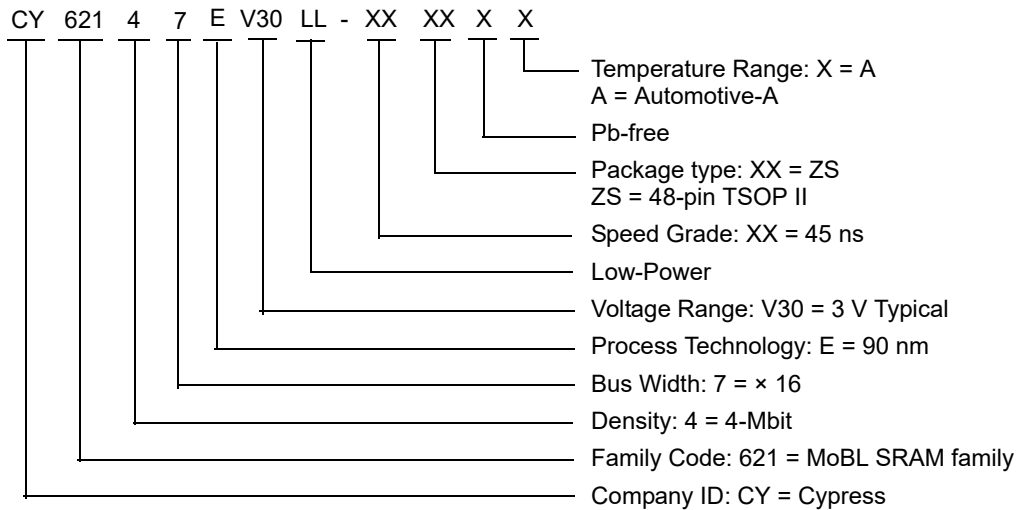
34. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device,  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $\overline{CE}_2$  such that when  $\overline{CE}_1$  is LOW and  $\overline{CE}_2$  is HIGH,  $\overline{CE}$  is LOW. For all other cases  $\overline{CE}$  is HIGH.
35. For the Dual Chip Enable device,  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $\overline{CE}_2$  such that when  $\overline{CE}_1$  is LOW and  $\overline{CE}_2$  is HIGH,  $\overline{CE}$  is LOW. For all other cases  $\overline{CE}$  is HIGH. Intermediate voltage levels is not permitted on any of the Chip Enable pins ( $\overline{CE}$  for the Single Chip Enable device;  $\overline{CE}_1$  and  $\overline{CE}_2$  for the Dual Chip Enable device).

## Ordering Information

| Speed (ns) | Ordering Code        | Package Diagram | Package Type             | Operating Range |
|------------|----------------------|-----------------|--------------------------|-----------------|
| 45         | CY62147EV30LL-45ZSXA | 51-85087        | 44-pin TSOP II (Pb-free) | Automotive-A    |

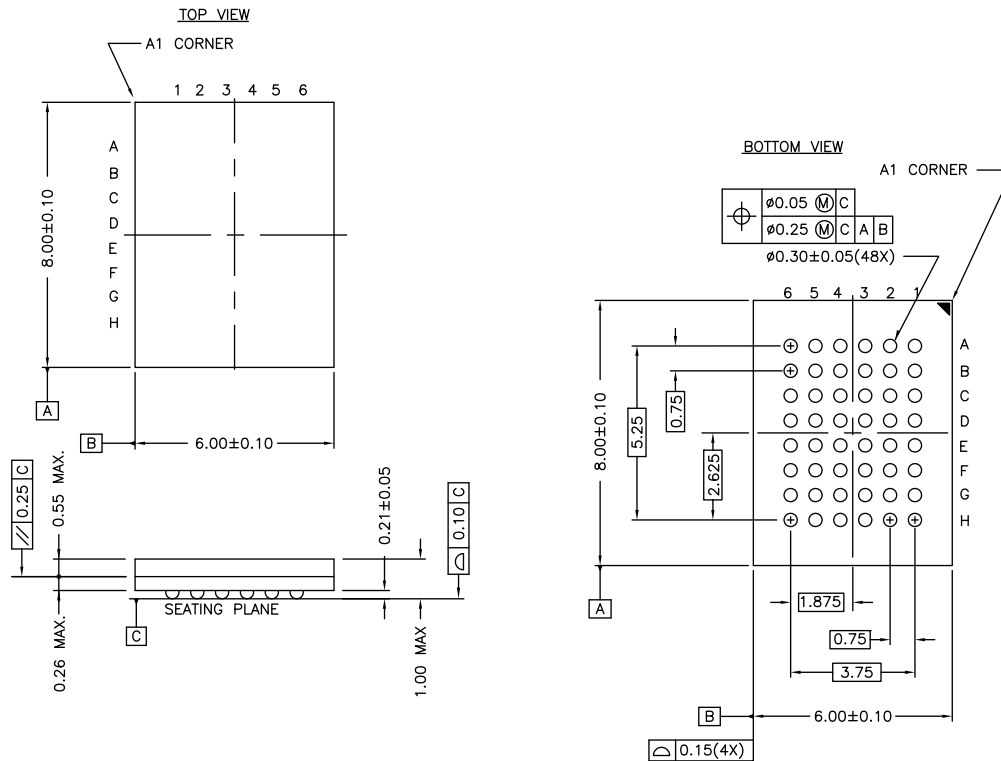
Contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definitions



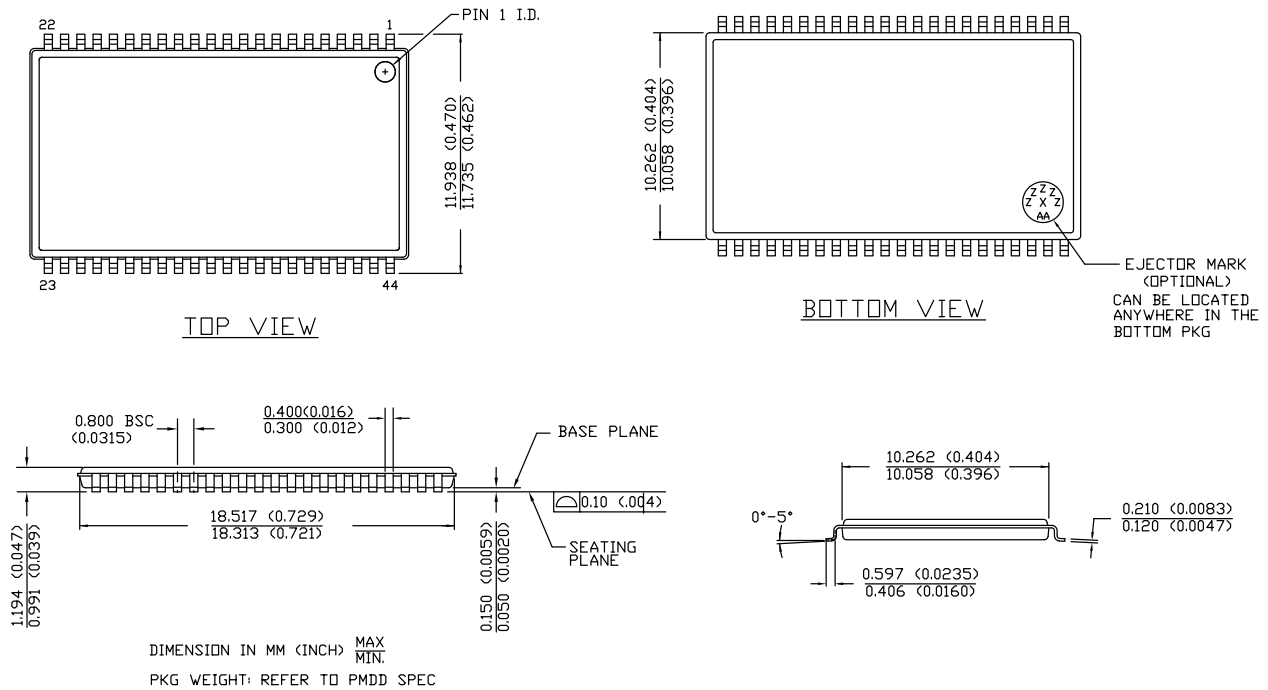
## Package Diagrams

**Figure 12. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150**



NOTE:  
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)  
posted on the Cypress web.

51-85150 \*H

**Package Diagrams (continued)**
**Figure 13. 44-pin TSOP Z44-II Package Outline, 51-85087**


51-85087 \*E

## Acronyms

| Acronym | Description                             |
|---------|-----------------------------------------|
| CMOS    | Complementary Metal Oxide Semiconductor |
| I/O     | Input/Output                            |
| SRAM    | Static Random Access Memory             |
| VFBGA   | Very Fine-Pitch Ball Grid Array         |
| TSOP    | Thin Small Outline Package              |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | megahertz       |
| μA     | microampere     |
| mA     | milliampere     |
| ns     | nanosecond      |
| Ω      | ohm             |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

## Document History Page

| Document Title: CY62147EV30 MoBL <sup>®</sup> Automotive, 4-Mbit (256K × 16) Static RAM<br>Document Number: 001-66256 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                           |
|-----------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                                                  | ECN No. | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                     |
| **                                                                                                                    | 3123973 | RAME            | 01/31/2011      | Created new datasheet for Automotive parts from document number 38-05440 Rev. *I                                                                                                                                                                                                                                                                                          |
| *A                                                                                                                    | 3937956 | MEMJ            | 03/19/2013      | Updated <a href="#">Package Diagrams</a> :<br>spec 51-85150 – Changed revision from *F to *H.<br>spec 51-85087 – Changed revision from *C to *E.<br>Completing Sunset Review.                                                                                                                                                                                             |
| *B                                                                                                                    | 4725832 | PSR             | 04/15/2015      | Updated <a href="#">Functional Description</a> :<br>Removed “For best practice recommendations, refer to the Cypress application note <a href="#">AN1064</a> , <a href="#">SRAM System Guidelines</a> .” at the end.<br>Added “For a complete list of related resources, <a href="#">click here</a> .” at the end.<br>Updated to new template.                            |
| *C                                                                                                                    | 5221444 | VINI            | 04/14/2016      | Updated <a href="#">Thermal Resistance</a> :<br>Updated details in “Test Conditions” column and updated all values in “VFBGA Package” and “TSOP II Package” columns corresponding to $\theta_{JA}$ and $\theta_{JC}$ parameters.<br>Updated to new template.<br>Completing Sunset Review.                                                                                 |
| *D                                                                                                                    | 6049466 | VINI            | 01/29/2018      | Updated <a href="#">Ordering Information</a> :<br>Updated part numbers.<br>Removed Note “This BGA package is offered with single chip enable.” and its reference.<br>Removed Note “This BGA package is offered with dual chip enable.” and its reference.<br>Updated <a href="#">Ordering Code Definitions</a> .<br>Updated to new template.<br>Completing Sunset Review. |

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|-------------------------------|--------------------------------------------------------------------|
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