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Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View) ^[1, 2]

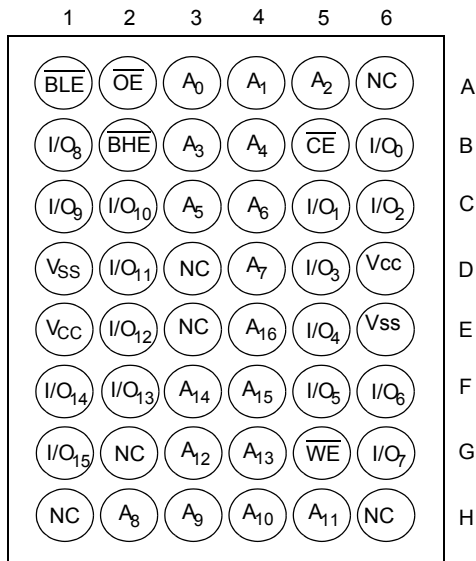
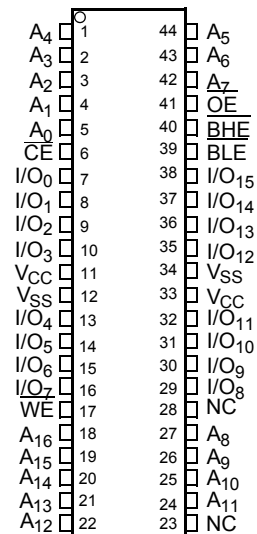


Figure 2. 44-pin TSOP II pinout (Top View) ^[1]



Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
	f = 1 MHz		f = f _{max}							
	Min	Typ ^[3]	Max		Typ ^[3]	Max	Typ ^[3]	Max	Typ ^[3]	Max
CY62137EV30-45LL	2.2 V	3.0 V	3.6 V	45 ns	2	2.5	15	20	1	7

Notes

1. NC pins are not connected on the die.
2. Pins D3, H1, G2, H6 and H3 in the 48-ball VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb and 64 Mb respectively.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature with power applied -55 °C to + 125 °C

Supply voltage to ground potential ^[4, 5] -0.3 V to (V_{CC(MAX)} + 0.3 V)

DC voltage applied to outputs in High Z state ^[4, 5] -0.3 V to (V_{CC(MAX)} + 0.3 V)

DC input voltage ^[4, 5] -0.3 V to (V_{CC(MAX)} + 0.3 V)

Output current into outputs (LOW) 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) > 2001 V

Latch up current > 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[6]
CY62137EV30-45LL	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ ^[7]	Max	
V _{OH}	Output HIGH voltage	I _{OH} = -0.1 mA, V _{CC} = 2.20 V	2.0	—	—	V
		I _{OH} = -1.0 mA, V _{CC} = 2.70 V	2.4	—	—	V
V _{OL}	Output LOW voltage	I _{OL} = 0.1 mA, V _{CC} = 2.20 V	—	—	0.4	V
		I _{OL} = 2.1 mA, V _{CC} = 2.70 V	—	—	0.4	V
V _{IH}	Input HIGH voltage	V _{CC} = 2.2 V to 2.7 V	1.8	—	V _{CC} + 0.3	V
		V _{CC} = 2.7 V to 3.6 V	2.2	—	V _{CC} + 0.3	V
V _{IL}	Input LOW voltage	V _{CC} = 2.2 V to 2.7 V	-0.3	—	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-0.3	—	0.8	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	-1	—	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , Output disabled	-1	—	+1	μA
I _{CC}	V _{CC} Operating supply current	f = f _{max} = 1/t _{RC} , V _{CC} = V _{CCmax}	—	15	20	mA
		f = 1 MHz, I _{OUT} = 0 mA, CMOS levels	—	2.0	2.5	
I _{SB1} ^[8]	Automatic CE power-down current — CMOS inputs	CE ≥ V _{CC} - 0.2 V or (BHE and BLE) ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V, V _{IN} ≤ 0.2 V, f = f _{max} (address and data only), f = 0 (OE and WE), V _{CC} = 3.60 V	—	1	7	μA
I _{SB2} ^[8]	Automatic CE power-down current — CMOS inputs	CE ≥ V _{CC} - 0.2 V or (BHE and BLE) ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0, V _{CC} = 3.60 V	—	1	7	μA

Notes

4. V_{IL(min.)} = -2.0 V for pulse durations less than 20 ns.

5. V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.

6. Full device AC operation assumes a 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.

7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.

8. Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.

Capacitance

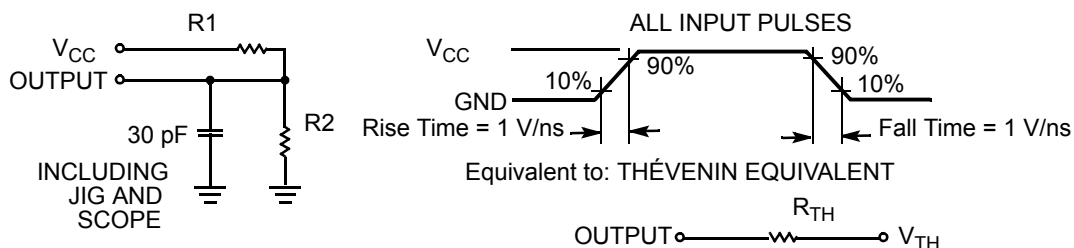
Parameter ^[9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[9]	Description	Test Conditions	48-ball BGA	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3×4.5 inch, four-layer printed circuit board	54	57	$^{\circ}\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		12	17	$^{\circ}\text{C/W}$

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note

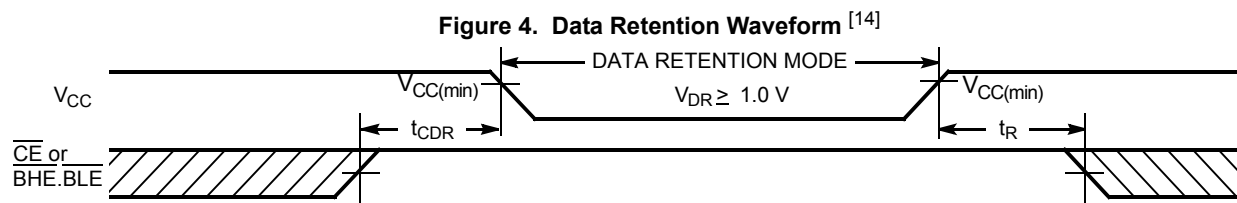
9. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[10]	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	–	V
$I_{CCDR}^{[11]}$	Data retention current	$V_{CC} = 1\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	0.8	3	μA
$t_{CDR}^{[12]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[13]}$	Operation recovery time		45	–	–	ns

Data Retention Waveform



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25\text{ }^\circ\text{C}$.
11. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min.)} \geq 100\text{ }\mu\text{s}$.
14. $\overline{BHE.BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. The chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter ^[15, 16]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	45	–	ns
t _{AA}	Address to data valid	–	45	ns
t _{OHA}	Data hold from address change	10	–	ns
t _{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t _{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[17]	5	–	ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[17, 18]	–	18	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[17]	10	–	ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[17, 18]	–	18	ns
t _{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t _{PD}	$\overline{CE}$ HIGH to power-down	–	45	ns
t _{DBE}	$\overline{BLE/BHE}$ LOW to data valid	–	45	ns
t _{LZBE}	$\overline{BLE/BHE}$ LOW to Low Z ^[17]	5	–	ns
t _{HZBE}	$\overline{BLE/BHE}$ HIGH to High Z ^[17, 18]	–	18	ns
Write Cycle ^[19, 20]				
t _{WC}	Write cycle time	45	–	ns
t _{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t _{AW}	Address setup to write end	35	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	$\overline{WE}$ pulse width	35	–	ns
t _{BW}	$\overline{BLE/BHE}$ LOW to write end	35	–	ns
t _{SD}	Data setup to write end	25	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[17, 18]	–	18	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[17]	10	–	ns

Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in [Figure 3 on page 5](#).
16. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes [AN13842](#) and [AN66311](#). However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
17. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
18. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
20. The minimum pulse width for write cycle 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 5. Read Cycle 1: Address Transition Controlled [21, 22]

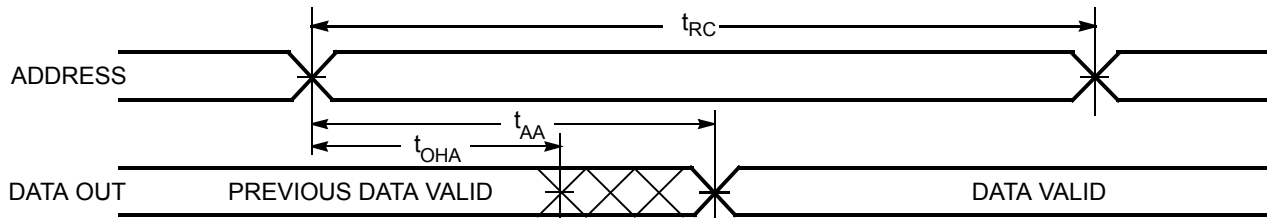
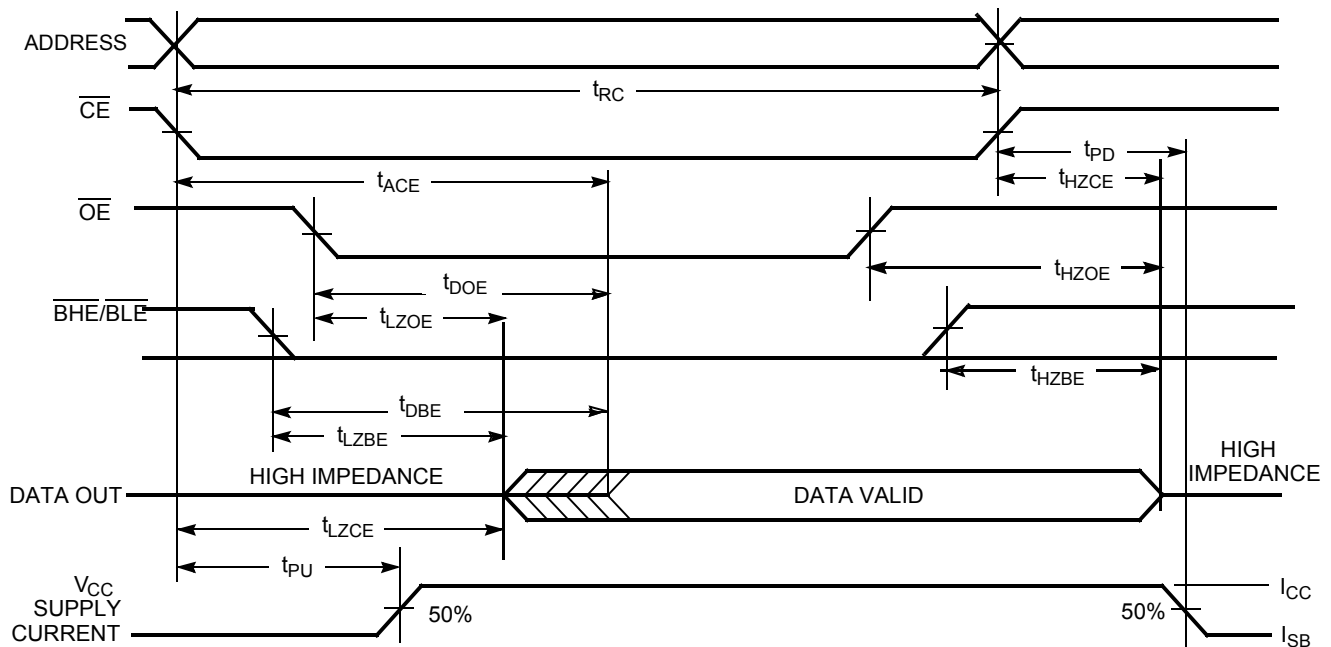


Figure 6. Read Cycle No. 2: $\overline{OE}$ Controlled [22, 23]



Notes

21. The device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and $\overline{BLE} = V_{IL}$.
22. $\overline{WE}$ is HIGH for read cycle.
23. Address valid prior to or coincident with $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1: $\overline{\text{WE}}$ Controlled [24, 25, 26]

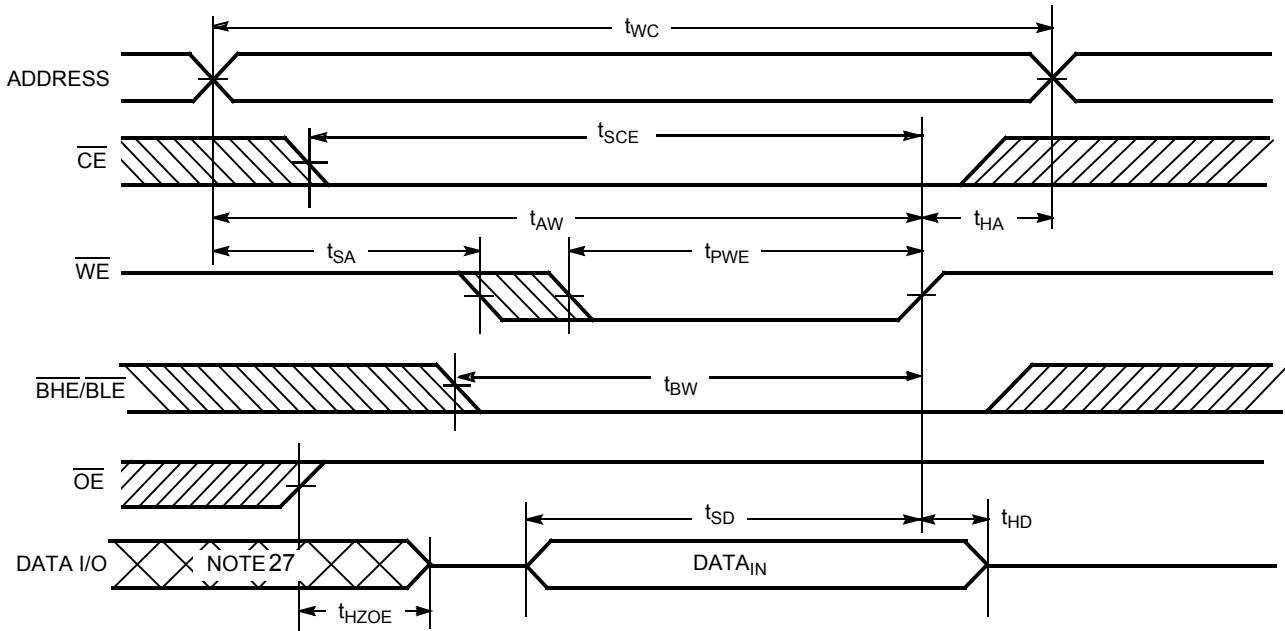
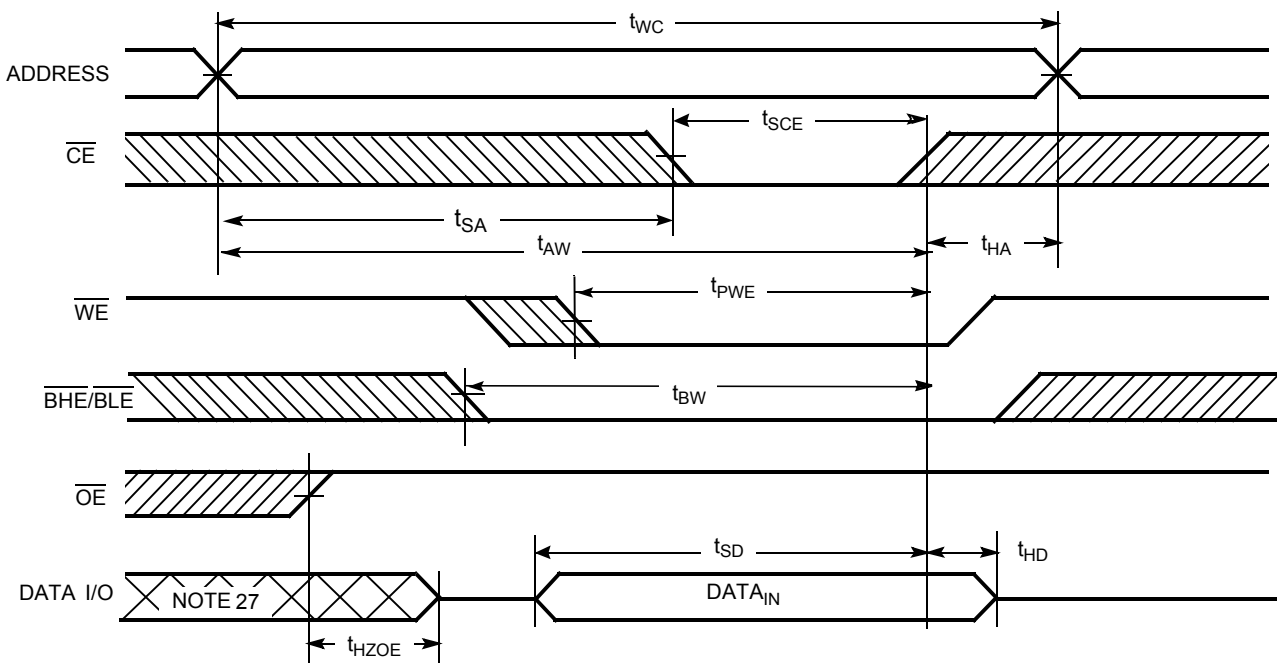


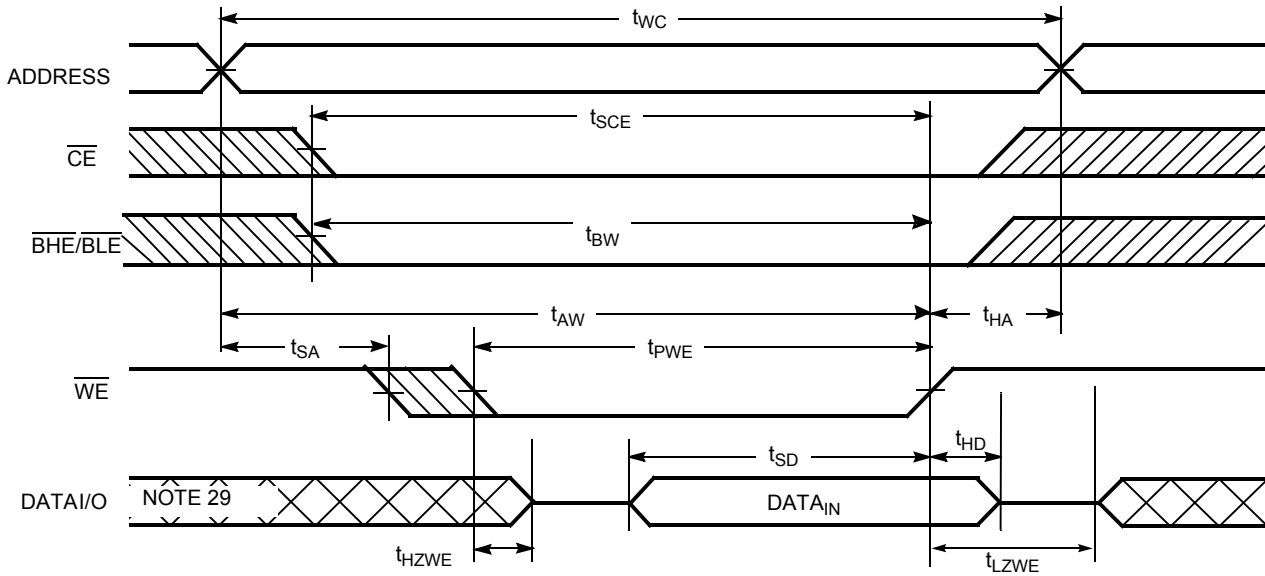
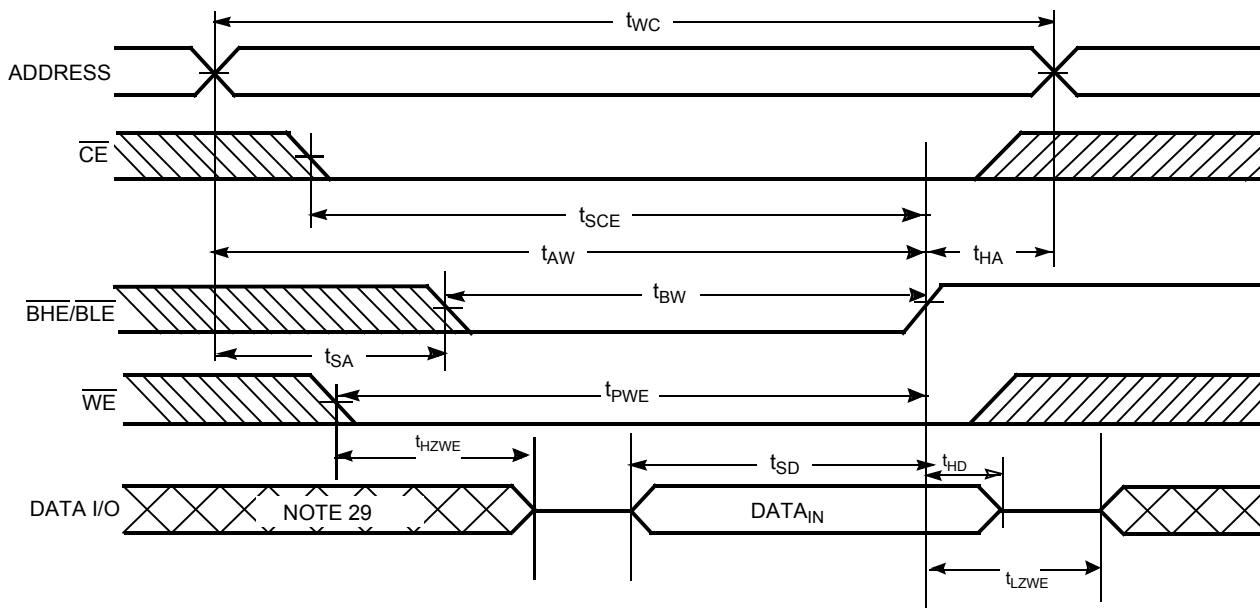
Figure 8. Write Cycle No. 2: $\overline{\text{CE}}$ Controlled [24, 25, 26]



Notes

24. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}}$, $\overline{\text{CE}} = V_{IL}$, $\overline{\text{BHE}}$ and $\overline{\text{BLE}} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
25. Data I/O is high impedance if $\overline{\text{OE}} = V_{IL}$.
26. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}} = V_{IH}$, the output remains in a high impedance state.
27. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3: $\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW ^[28]

Figure 10. Write Cycle No. 4: $\overline{\text{BHE/BLE}}$ Controlled, $\overline{\text{OE}}$ LOW ^[28]

Notes

28. If CE goes HIGH simultaneously with $\overline{\text{WE}} = V_{IH}$, the output remains in a high impedance state.
 29. During this period, the I/Os are in output state and input signals should not be applied.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X ^[30]	X ^[30]	High Z	Deselect/power-down	Standby (I _{SB})
X ^[30]	X	X	H	H	High Z	Deselect/power-down	Standby (I _{SB})
L	H	L	L	L	Data out (I/O ₀ –I/O ₁₅)	Read	Active (I _{CC})
L	H	L	H	L	Data out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Read	Active (I _{CC})
L	H	L	L	H	Data out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Read	Active (I _{CC})
L	H	H	L	L	High Z	Output disabled	Active (I _{CC})
L	H	H	H	L	High Z	Output disabled	Active (I _{CC})
L	H	H	L	H	High Z	Output disabled	Active (I _{CC})
L	L	X	L	L	Data in (I/O ₀ –I/O ₁₅)	Write	Active (I _{CC})
L	L	X	H	L	Data in (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Write	Active (I _{CC})
L	L	X	L	H	Data in (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Write	Active (I _{CC})

Note

30. Chip enable ($\overline{\text{CE}}$) and Byte enables ($\overline{\text{BHE}}$ / $\overline{\text{BLE}}$) must be at fixed CMOS levels (not floating). Intermediate voltage levels on these pins is not permitted.

Ordering Information

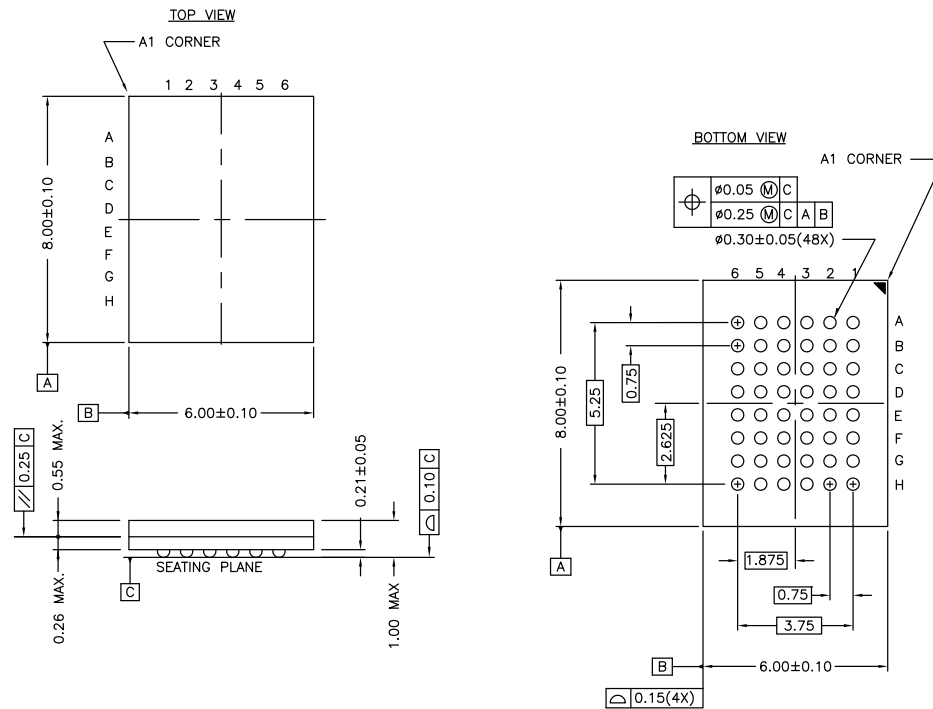
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62137EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
45	CY62137EV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	

Ordering Code Definitions

CY	621	3	7	E	V30	LL	-	45	XX	X	I	
												Temperature Grade: I = Industrial
												Pb-free
												Package Type: XX = BV or ZS
												BV = 48-ball VFBGA
												ZS = 44-pin TSOP II
												Speed Grade: 45 ns
												Low Power
												Voltage Range: V30 = 3 V typical
												Process Technology: E = 90 nm
												Bus Width: 7 = × 16
												Density: 3 = 2-Mbit
												Family Code: 621 = MoBL SRAM family
												Company ID: CY = Cypress

Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150

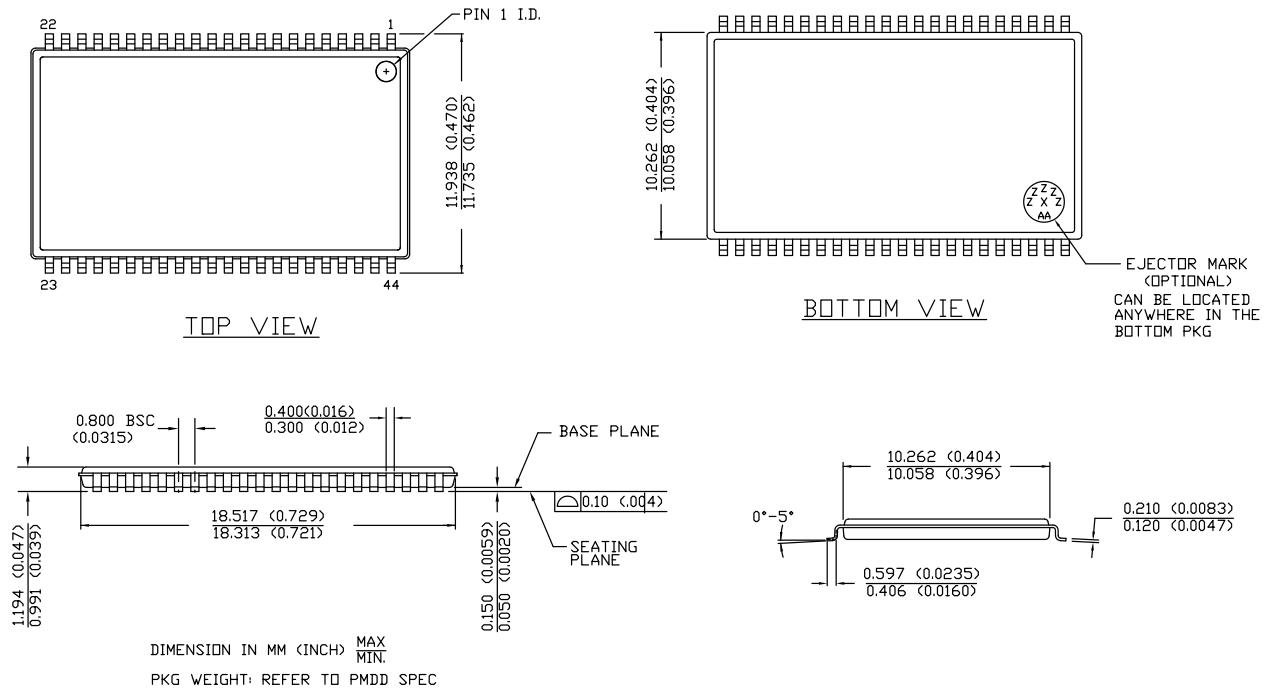


NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)
posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
%	percent
pF	picofarad
Ω	ohm
V	volt
W	watt

Document History Page

Document Title: CY62137EV30 MoBL®, 2-Mbit (128 K × 16) Static RAM Document Number: 38-05443				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	203720	AJU	See ECN	New data sheet
*A	234196	AJU	See ECN	Changed I _{CC} MAX at f=1MHz from 1.7 mA to 2.0 mA Changed I _{CC} TYP from 12 mA (35 ns speed bin) and 10 mA (45 ns speed bin) to 15 mA and 12 mA respectively Changed I _{CC} MAX from 20 mA (35 ns speed bin) and 15 mA (45 ns speed bin) to 25 mA and 20 mA respectively Changed I _{SB1} and I _{SB2} TYP from 0.6 µA to 0.7 µA Changed I _{SB1} and I _{SB2} MAX from 1.5 µA to 2.5 µA Changed I _{CCDR} from 1 µA to 2 µA Fixed typos on TSOP II pinout: Pin 18-22: address lines Pin 23: NC Added Pb-free information
*B	427817	NXR	See ECN	Converted from Advanced Information to Final. Removed 35 ns Speed Bin Removed "L" version Changed ball E3 from DNU to NC. Removed the redundant footnote on DNU. Moved Product Portfolio from Page # 3 to Page #2. Changed I _{CC} (Max) value from 2 mA to 2.5 mA and I _{CC} (Typ) value from 1.5 mA to 2 mA at f=1 MHz Changed I _{CC} (Typ) value from 12 mA to 15 mA at f = f _{max} =1/t _{RC} Changed I _{SB1} and I _{SB2} Typ. values from 0.7 µA to 1 µA and Max. values from 2.5 µA to 7 µA. Changed V _{CC} stabilization time in footnote #7 from 100 µs to 200 µs Changed the AC test load capacitance from 50pF to 30pF on Page# 4 Changed V _{DR} from 1.5V to 1V on Page# 4. Changed I _{CCDR} from 2 µA to 3 µA. Added I _{CCDR} typical value. Corrected t _R in Data Retention Characteristics from 100 µs to t _{RC} ns Changed t _{OHA} , t _{LZCE} and t _{LZWE} from 6 ns to 10 ns Changed t _{LZBE} from 6 ns to 5 ns Changed t _{LZOE} from 3 ns to 5 ns Changed t _{HZOE} , t _{HZCE} , t _{HZBE} and t _{HZWE} from 15 ns to 18 ns Changed t _{SCE} , t _{AW} and t _{BW} from 40 ns to 35 ns Changed t _{PWE} from 30 ns to 35 ns Changed t _{SD} from 20 ns to 25 ns Updated the Ordering Information table and replaced the Package Name column with Package Diagram.
*C	2604685	VKN / PYRS	11/12/08	Added footnote 8 related to I _{SB2} and I _{CCDR} Added footnote 13 related to AC timing parameters
*D	3143896	RAME	01/17/2011	Converted all tablenote to footnotes. Added Ordering Code Definitions . Added Acronyms and Units of Measure . Updated Package Diagrams : spec 51-85150 – Changed revision from *D to *F.
*E	3283711	AJU	06/15/2011	Updated Functional Description : Removed the Note "For best practice recommendations, refer to the Cypress application note "SRAM System Design Guidelines" on http://www.cypress.com website." and its reference. Updated to new template.

Document History Page (continued)

Document Title: CY62137EV30 MoBL®, 2-Mbit (128 K × 16) Static RAM Document Number: 38-05443				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*F	3806123	TAVA	11/08/2012	Updated Data Retention Waveform (Updated Figure 4 (Changed “V _{DR} ≥ 1.5 V” to “V _{DR} ≥ 1.0 V”)). Updated Package Diagrams (spec 51-85150 (Changed revision from *F to *H), spec 51-85087 (Changed revision from *C to *E)).
*G	4101224	VINI	08/21/2013	Updated Switching Characteristics : Updated Note 16. Updated to new template. Completing Sunset Review.
*H	4574264	VINI	11/19/2014	Updated Functional Description : Added “For a complete list of related documentation, click here .” at the end. Updated Maximum Ratings : Referred Notes 4 and 5 In “Supply voltage to ground potential”. Updated Switching Characteristics : Added Note 20 and referred the same note in “Write Cycle”.
*I	5025363	VINI	11/24/2015	Updated Thermal Resistance : Changed value of Θ_{JA} parameter corresponding to 48-ball BGA package from 75 °C/W to 54 °C/W. Changed value of Θ_{JA} parameter corresponding to 44-pin TSOP II package from 77 °C/W to 57 °C/W. Changed value of Θ_{JC} parameter corresponding to 48-ball BGA package from 10 °C/W to 12 °C/W. Changed value of Θ_{JC} parameter corresponding to 44-pin TSOP II package from 13 °C/W to 17 °C/W. Updated to new template. Completing Sunset Review.

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