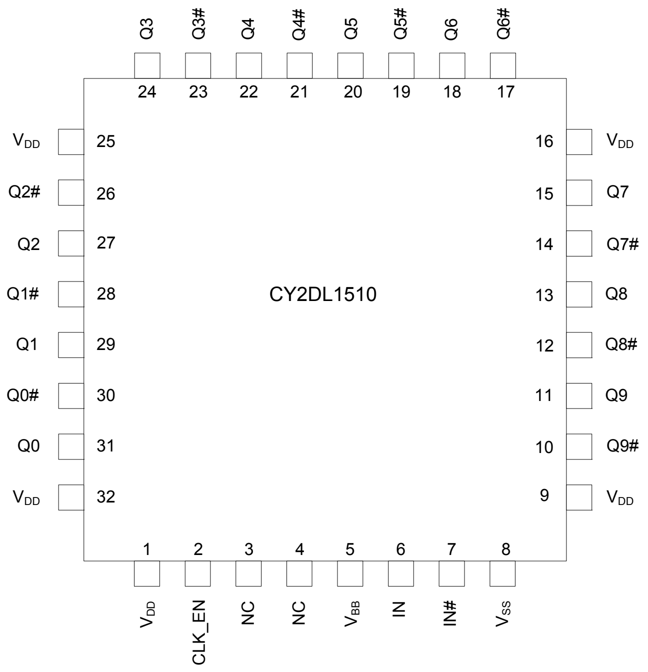
Contents

Pinouts

Figure 1. 32-pin TQFP pinout



Pin Definitions

Pin No.	Pin Name	Pin Type	Description
1, 9, 16, 25, 32	V_{DD}	Power	Power supply
2	CLK_EN	Input	Synchronous clock enable. Low-voltage complementary metal oxide semiconductor (LVCMOS)/low-voltage transistor-transistor-logic (LVTTL). When CLK_EN = Low, Q(0:9) outputs are held low and Q(0:9)# outputs are held high
3, 4	NC		No connection
5	V_{BB}	Output	LVDS reference voltage output
6	IN	Input	LVDS input clock
7	IN#	Input	LVDS complementary input clock
8	V_{SS}	Power	Ground
10, 12, 14, 17, 19, 21, 23, 26, 28, 30	Q(0:9)#	Output	LVDS complementary output clocks
11, 13, 15, 18, 20, 22, 24, 27, 29, 31	Q(0:9)	Output	LVDS output clocks

Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	Non-functional	–0.5	4.6	V
V_{IN}[2]	Input voltage, relative to V_{SS}	Non-functional	–0.5	lesser of 4.0 or V_{DD} + 0.4	V
V_{OUT}[2]	DC output or I/O Voltage, relative to V_{SS}	Non-functional	–0.5	lesser of 4.0 or V_{DD} + 0.4	V
T_S	Storage temperature	Non-functional	–55	150	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	–	V
L_U	Latch up		Meets or exceeds JEDEC Spec JESD78B IC latch up test		
UL–94	Flammability rating	At 1/8 in.	V–0		
MSL	Moisture sensitivity level		3		

Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.5 V supply	2.375	2.625	V
		3.3 V supply	3.135	3.465	V
T_A	Ambient operating temperature	Commercial	0	70	°C
		Industrial	–40	85	°C
t_{PU}	Power ramp time	Power-up time for V_{DD} to reach minimum specified voltage (power ramp must be monotonic.)	0.05	500	ms

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Note

[2] The voltage on any I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

DC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Max	Unit
I_{DD}	Operating supply current	All LVDS outputs terminated with 100 Ω load [3, 4]	–	125	mA
V_{IH1}	Input high Voltage, LVDS input clocks, IN and IN#		–	V_{DD} + 0.3	V
V_{IL1}	Input low voltage, LVDS input clocks, IN and IN#		–0.3	–	V
V_{IH2}	Input high voltage, CLK_EN	V_{DD} = 3.3 V	2.0	V_{DD} + 0.3	V
V_{IL2}	Input low voltage, CLK_EN	V_{DD} = 3.3 V	–0.3	0.8	V
V_{IH3}	Input high voltage, CLK_EN	V_{DD} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL3}	Input low voltage, CLK_EN	V_{DD} = 2.5 V	–0.3	0.7	V
V_{ID}[5]	Input differential amplitude	See Figure 3 on page 7	0.4	0.8	V
V_{ICM}	Input common mode voltage	See Figure 3 on page 7	0.5	V_{DD} – 0.2	V
I_{IH}	Input high current, All inputs	Input = V_{DD} [6]	–	150	µA
I_{IL}	Input low current, All inputs	Input = V_{SS} [6]	–150	–	µA
V_{PP}	LVDS differential output voltage peak to peak, single-ended	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between Q and Q# pairs [3, 7]	250	470	mV
ΔV_{OCM}	Change in V_{OCM} between complementary output states	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between Q and Q# pairs [3, 7]	–	50	mV
V_{BB}	Output reference voltage	0 to 150 µA output current	1.125	1.375	V
R_{TERM}	On-chip differential input termination resistor		80	120	Ω
R_P	Internal pull-up resistance, LVCMOS logic input	CLK_EN pin	60	140	kΩ
C_{IN}	Input capacitance	Measured at 10 MHz per pin	–	3	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	32-pin TQFP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	69	°C/W
θ_{JC}	Thermal resistance (junction to case)		14	°C/W

Notes

3. Refer to Figure 2 on page 7.
4. I_{DD} includes current that is dissipated externally in the output termination resistors.
5. V_{ID} minimum of 400 mV is required to meet all output AC Electrical Specifications. The device is functional with V_{ID} minimum of greater than 200 mV.
6. Positive current flows into the input pin, negative current flows out of the input pin.
7. Refer to Figure 4 on page 7.
8. These parameters are guaranteed by design and are not tested.

AC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{IN}	Input frequency		DC	–	1.5	GHz
F_{OUT}	Output frequency	$F_{OUT} = F_{IN}$	DC	–	1.5	GHz
t_{PD}[11]	Propagation delay input pair to output pair	Input rise/fall time < 1.5 ns (20% to 80%)	–	–	600	ps
t_{ODC}[12]	Output duty cycle	50% duty cycle at input Frequency range up to 1 GHz	48	–	52	%
t_{SK1}[13]	Output-to-output skew	Any output to any output, with same load conditions at DUT	–	–	40	ps
$t_{SK1\ D}$[13]	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	–	–	150	ps
PN_{ADD}	Additive RMS phase noise 156.25 MHz input Rise/fall time < 150 ps (20% to 80%) V_{ID} > 400 mV	Offset = 1 kHz	–	–	–120	dBc/Hz
		Offset = 10 kHz	–	–	–135	dBc/Hz
		Offset = 100 kHz	–	–	–135	dBc/Hz
		Offset = 1 MHz	–	–	–150	dBc/Hz
		Offset = 10 MHz	–	–	–154	dBc/Hz
		Offset = 20 MHz	–	–	–155	dBc/Hz
t_{JIT}[14]	Additive RMS phase jitter (Random)	156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV	–	–	0.11	ps
t_R, t_F[15]	Output rise/fall time, single-ended	50% duty cycle at input, 20% to 80% of full swing (V_{OL} to V_{OH}) Input rise/fall time < 1.5 ns (20% to 80%) Measured at 1 GHz	–	–	300	ps
t_{SOD}	Time from clock edge to outputs disabled	Synchronous clock enable (CLK_EN) switched low	–	–	700	ps
t_{SOE}	Time from clock edge to outputs enabled	Synchronous clock enable (CLK_EN) switched high	–	–	700	ps

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Notes

[9] Refer to Figure 2 on page 7.
[10] Refer to Figure 4 on page 7.
[11] Refer to Figure 5 on page 7.
[12] Refer to Figure 6 on page 7.
[13] Refer to Figure 7 on page 8.
[14] Refer to Figure 8 on page 8.
[15] Refer to Figure 9 on page 8.

Switching Waveforms

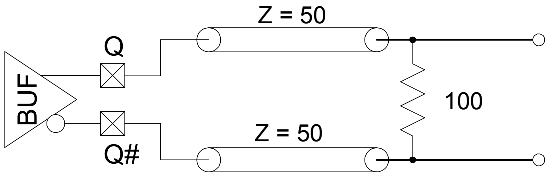


Figure 2. LVDS Output Termination

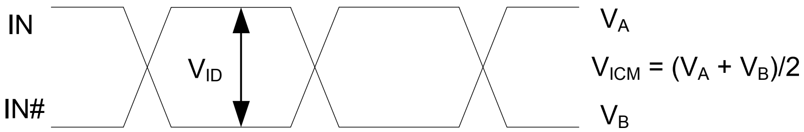


Figure 3. Input Differential and Common Mode Voltages

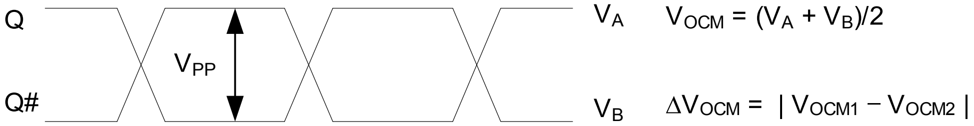


Figure 4. Output Differential and Common Mode Voltages

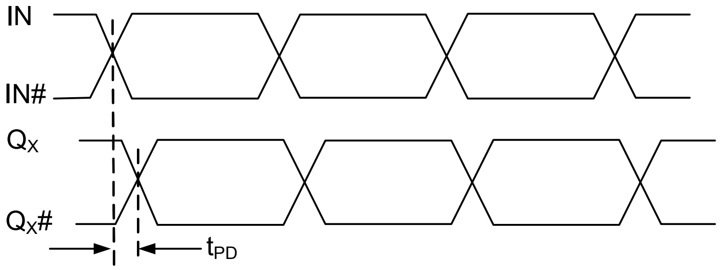


Figure 5. Input to Any Output Pair Propagation Delay

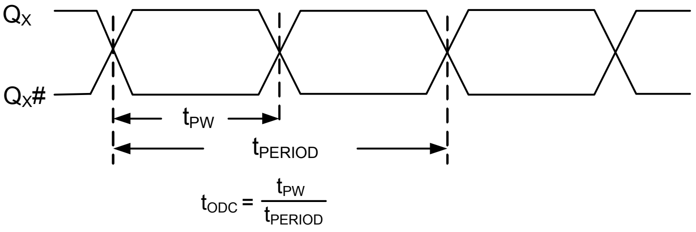


Figure 6. Output Duty Cycle

Switching Waveforms (continued)

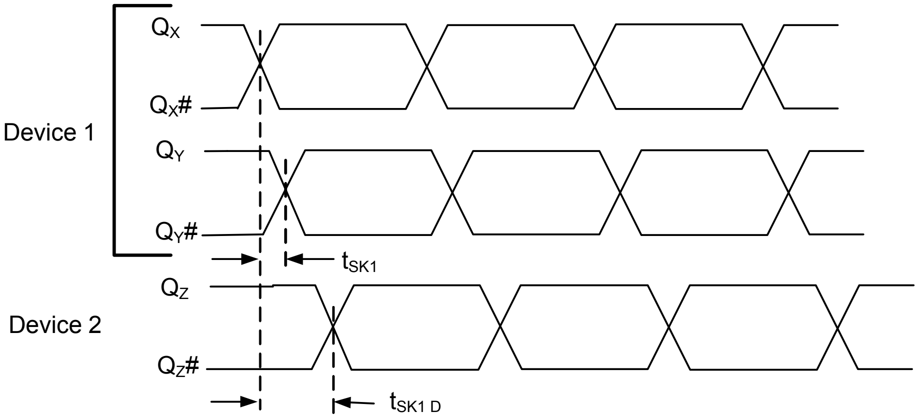
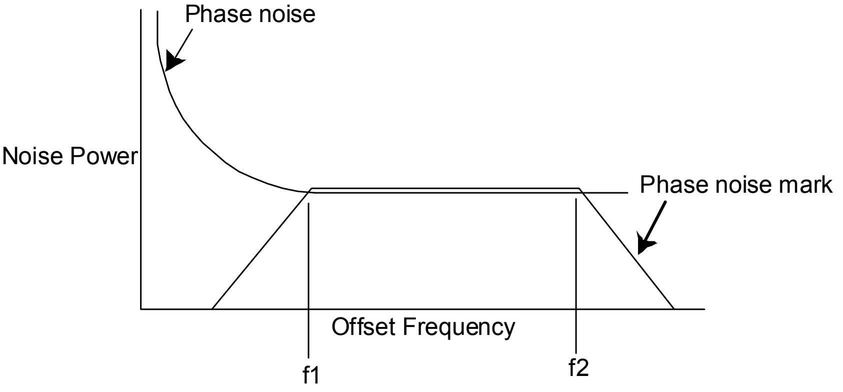


Figure 7. Output-to-output and Device-to-device Skew



$$\text{RMS Jitter} \propto \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

Figure 8. RMS Phase Jitter

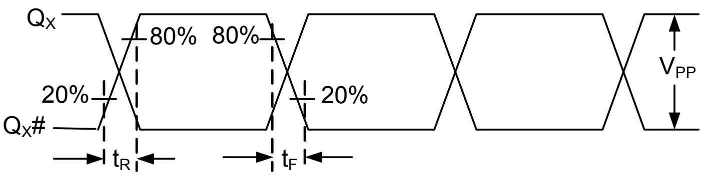


Figure 9. Output Rise/Fall Time

Switching Waveforms (continued)

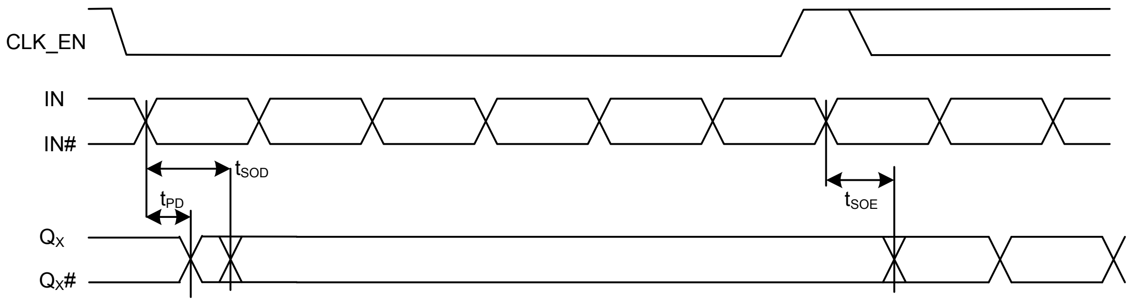
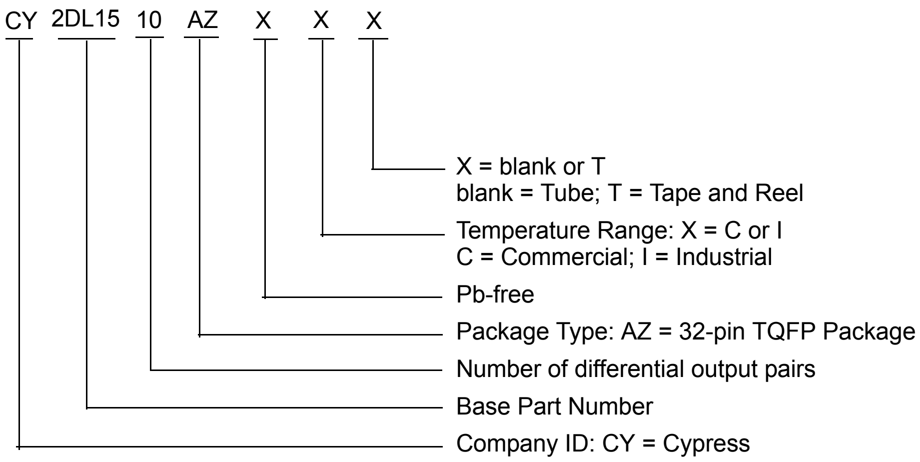


Figure 10. Synchronous Clock Enable Timing

Ordering Information

Part Number	Type	Production Flow
Pb-free		
CY2DL1510AZC	32-pin TQFP	Commercial, 0 °C to 70 °C
CY2DL1510AZCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to 70 °C
CY2DL1510AZI	32-pin TQFP	Industrial, –40 °C to 85 °C
CY2DL1510AZIT	32-pin TQFP – Tape and Reel	Industrial, –40 °C to 85 °C

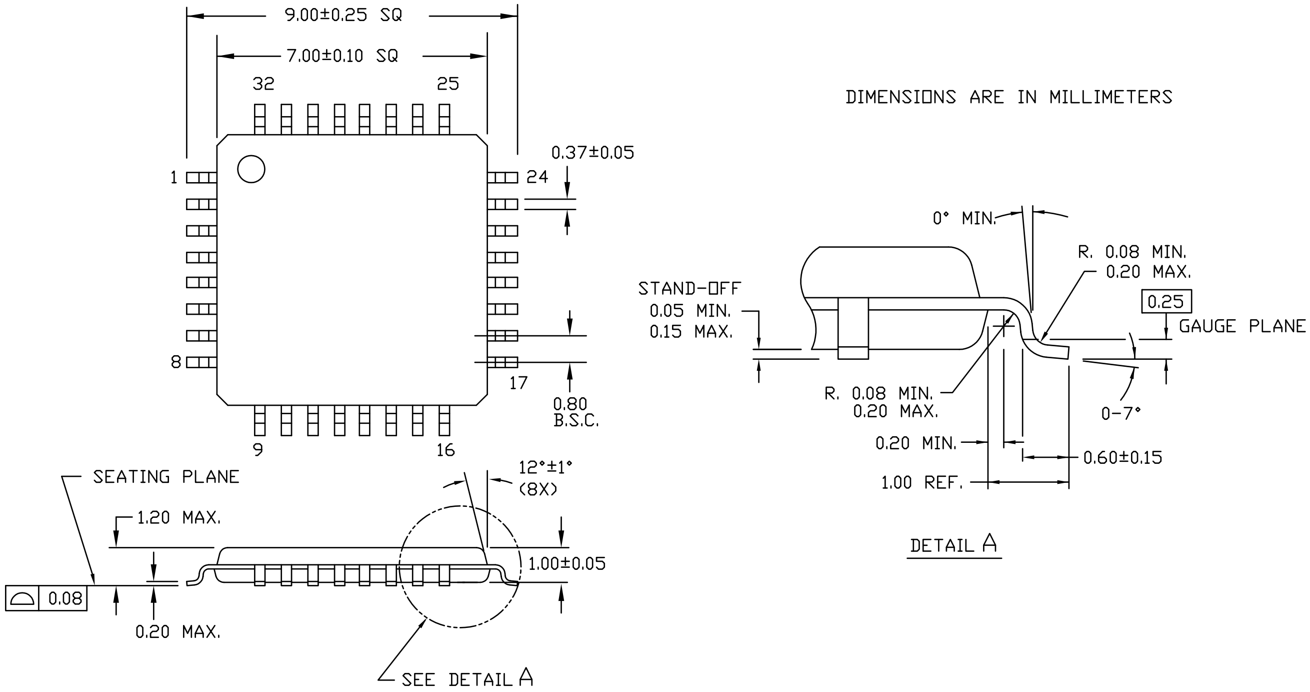
Ordering Code Definitions



X = blank or T
blank = Tube; T = Tape and Reel
Temperature Range: X = C or I
C = Commercial; I = Industrial
Pb-free
Package Type: AZ = 32-pin TQFP Package
Number of differential output pairs
Base Part Number
Company ID: CY = Cypress

Package Diagram

Figure 11. 32-pin TQFP (7 × 7 × 1.0 mm) A 3210 Package Outline, 51-85063



51-85063 *E

Acronyms

Acronym	Description
ESD	Electrostatic Discharge
HBM	Human Body Model
JEDEC	Joint Electron Devices Engineering Council
LVDS	Low-Voltage Differential Signal
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low-Voltage Transistor-Transistor Logic
OE	Output Enable
RMS	Root Mean Square
TQFP	Thin Quad Flat Pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	gigahertz
Hz	hertz
kΩ	kilohm
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2DL1510, 1:10 Differential LVDS Fanout Buffer **Document Number: 001-54863**				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2744225	CXQ / PYRS	08/19/09	New data sheet.
*A	2782891	CXQ	10/09/09	Updated format of Logic Block Diagram on page 1. Added T_{SOD} and T_{SOE} specs (700 ps max) to AC Specs table. Added T_{SETUP} and T_{HOLD} specs (300 ps min) to AC Specs table. Changed equation for RMS jitter in Figure 8 to proportionality. Changed package drawing from 1.4 mm thickness 51-85088 spec to 1.0 mm thickness 51-850063 spec. Added “Synchronous Clock Enable Function” to Features on page 1.
*B	2838916	CXQ	01/05/2010	Changed status from Advance to Preliminary. Changed from 0.34 ps to 0.25 ps maximum additive jitter in “Features” on page 1 and in t_{JIT} in the AC Electrical Specs table on page 5. Added t_{PU} spec to the Operating Conditions table on page 3. Removed V_{OD} and ΔV_{OD} specs from the DC Electrical Specs table on page 4. Added V_{PP} and ΔV_{PP} specs to the AC Electrical Specs table on page 5. V_{PP} min = 250 mV and max = 470 mV; ΔV_{PP} max = 50 mV. Added internal pullup resistance spec for CLK_EN in the DC Electrical Specs table on page 4. Min = 60 kΩ, Max = 140 kΩ. Added a measurement definition for C_{IN} in the DC Electrical Specs table on page 4. Changed letter case and some names of all the timing parameters in the AC Electrical Specs table on page 5 to be consistent with EROS. Lowered all additive phase noise mask specs by 3 dB in the AC Electrical Specs table on page 5. Added condition to t_R and t_F specs in the AC Electrical specs table on page 5 that input rise/fall time must be less than 1.5 ns (20% to 80%). Changed letter case and some names of all the timing parameters in Figures 5, 6, 7, and 9, to be consistent with EROS. Updated Figure 4 with definitions for V_{PP} and ΔV_{PP}.
*C	2885033	CXQ	02/26/2010	Updated 32-Pin TQFP package diagram.
*D	3011766	CXQ	08/20/2010	Changed maximum additive jitter from 0.25 ps to 0.11 ps in “Features” on page 1 and in t_{JIT} in the AC Electrical Specs table on page 5. Changed max t_{PD} spec from 480 ps to 600 ps. Added note 5 to describe I_{IH} and I_{IL} specs. Removed reference to data distribution from “Functional Description”. Changed R_P for differential inputs from 100 kΩ to 150 kΩ in the Logic Block Diagram and from 60 kΩ min / 140 kΩ max to 90 kΩ min / 210 kΩ max in the DC Electrical Specs table. Added V_{ID} max spec of 0.8V in the DC Electrical Specs table. Updated phase noise specs for 1 k/10 k/100 k/1 M/10 M/20 MHz offset to -120/-130/-135/-150/-150/-150dBc/Hz, respectively, in the AC Electrical Specs table. Added “Frequency range up to 1 GHz” condition to t_{ODC} spec. Added Acronyms and Ordering Code Definition.
*E	3017258	CXQ	08/27/2010	Corrected Output Rise/Fall time diagram.

Document History Page (continued)

Document Title: CY2DL1510, 1:10 Differential LVDS Fanout Buffer **Document Number: 001-54863**				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	3100234	CXQ	11/18/2010	Changed V_{IN} and V_{OUT} specs from 4.0V to “lesser of 4.0 or V_{DD} + 0.4” Removed 200mA min LU spec, replaced with “Meets or exceeds JEDEC Spec JESD78B IC Latchup Test” Moved V_{PP} from AC spec table to DC spec table, removed $\Delta V_{PP.}$ Removed R_P spec for differential input clock pins IN_X and IN_X#. Changed C_{IN} condition to “Measured at 10 MHz”. Changed PN_{ADD} specs for 10kHz, 10MHz, and 20MHz offsets. Added “Measured at 1 GHz” to t_R, t_F spec condition. Removed t_S and t_H specs from AC specs table. Changed to CY2DL1510AZ package code in Ordering Information. Added to Z package code in Ordering Code Definition.
*G	3135201	CXQ	01/12/2011	Changed status from Preliminary to Final. Updated Logic Block Diagram (Fixed typo and removed resistors from IN/IN#). Updated Switching Waveforms: Added Figure 10 (to describe T_{SOE} and T_{SOD}).
*H	3090938	CXQ	02/25/2011	Post to external web.
*I	3952187	CINM	04/02/2013	Updated Package Diagram: spec 51-85063 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*J	4586288	CINM	12/04/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*K	5260362	TAVA	05/05/2016	Added Thermal Resistance. Updated Package Diagram: spec 51-85063 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*L	5983414	AESATMP8	12/04/2017	Updated logo and Copyright.

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