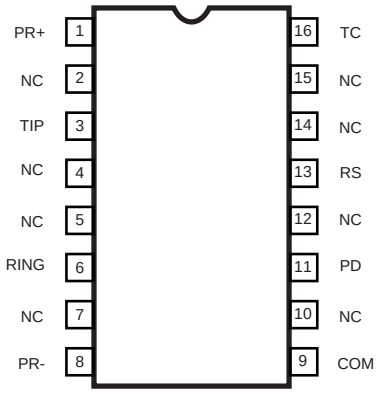
1. Specifications

1.1 Package Pinout



1.2 Pin Description

Pin	Name	Description
1	PR+	Protection resistor positive side
2	NC	No connection
3	TIP	Tip Lead
4	NC	No connection
5	NC	No connection
6	RING	Ring lead
7	NC	No connection
8	PR-	Protection resistor negative side
9	COM	Common
10	NC	No connection
11	PD	Photo-diode (LED input current)
12	NC	No connection
13	RS	Current limiting resistor
14	NC	No connection
15	NC	No connection
16	TC	Timing capacitor

1.3 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Maximum Voltage (T to R, R to T)*	-	300	V
Power dissipation	-	1	W
Operating temperature	-40	+85	°C
Operating relative humidity	5	95	%
Storage temperature	-40	+125	°C

Electrical absolute maximum ratings are at 25°C.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Electrical Characteristics

Unless otherwise specified, minimum and maximum values are guaranteed by production testing requirements. Typical values are characteristic of the device and are the result of engineering evaluations. In addition, typical values are provided for informational purposes only and are not part of the testing requirements.

All electrical specifications are provided for T_A=25°C

1.4.1 DC Characteristics, Normal Operation

For operational templates: (see Figure 2 on page 5) and (see Figure 3 on page 5).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Activate/Non-activate Voltage	Off State	V_{AN}	30.0	35.0	39.0	V
Breakover current	-	I_{BO}	-	0.5	1	mA
DC Voltage drop	Active State, 1 mA ≤ I_{SL} ≤ 20 mA	V_{ON}	-	12.5	15	V
DC leakage current	V_{OFF} = 20 V	I_{LKG}	-	1.5	5	µA
Hold/Release current	Active State	$I_{H/R}$	0.1	0.5	1.0	mA
Minimum on current	V_{ON} < 54 V	I_{MIN1}	20	38	-	mA
	54 V ≤ V_{ON} ≤ 100 V for 2 seconds, source resistance 200 Ω to 4 kΩ	I_{MIN2}	9.0	45	-	mA
	V_{ON} > 100 V	I_{MIN3}	0	0.1	-	mA
Maximum on current	V_{ON} ≤ 70 V	I_{MAX1}	-	38.4	70	mA
	V_{ON} > 70 V	I_{MAX2}	-	-	$\frac{V_{ON}}{1k\Omega}$	mA
Photodiode drive current	Active State	I_{PD}	0.2	0.3	10	mA

1.4.2 AC Characteristics, Normal Operation

For test conditions: (see Figure 4 on page 6).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
AC impedance	200 Hz to 50 kHz	Z_{MT}	10	38	-	kΩ
Linearity distortion	f = 200 Hz to 40 kHz, I_{SL} = 1 mA to 20 mA, V_{APP} ≤ 12 V_{PP}	D	40	70	-	dB

1.4.3 Transition Characteristics, Normal Operation

For activation/deactivation test conditions: (see Figure 5 on page 7).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Activate time	(see Figure 6 on page 7)	t1	3.0	13	50	ms
Deactivate time	(see Figure 7 on page 7)	t2	3.0	-	100	ms

Figure 2. I-V Requirements Template, 0 V to 50 V

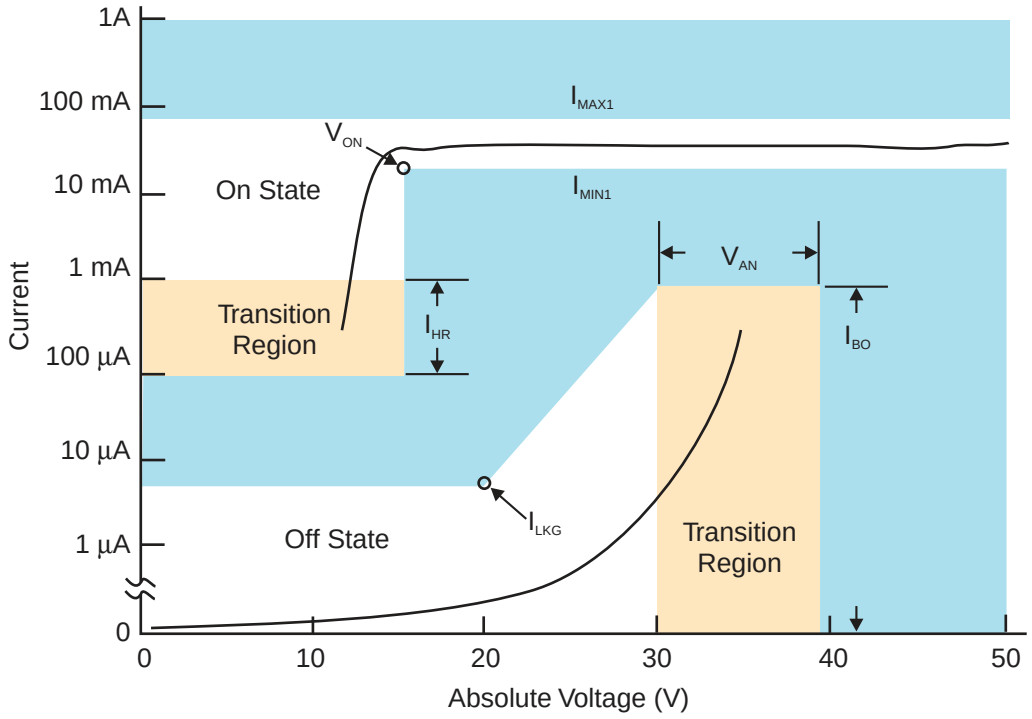


Figure 3. I-V Requirements Template, 0 V to 250 V

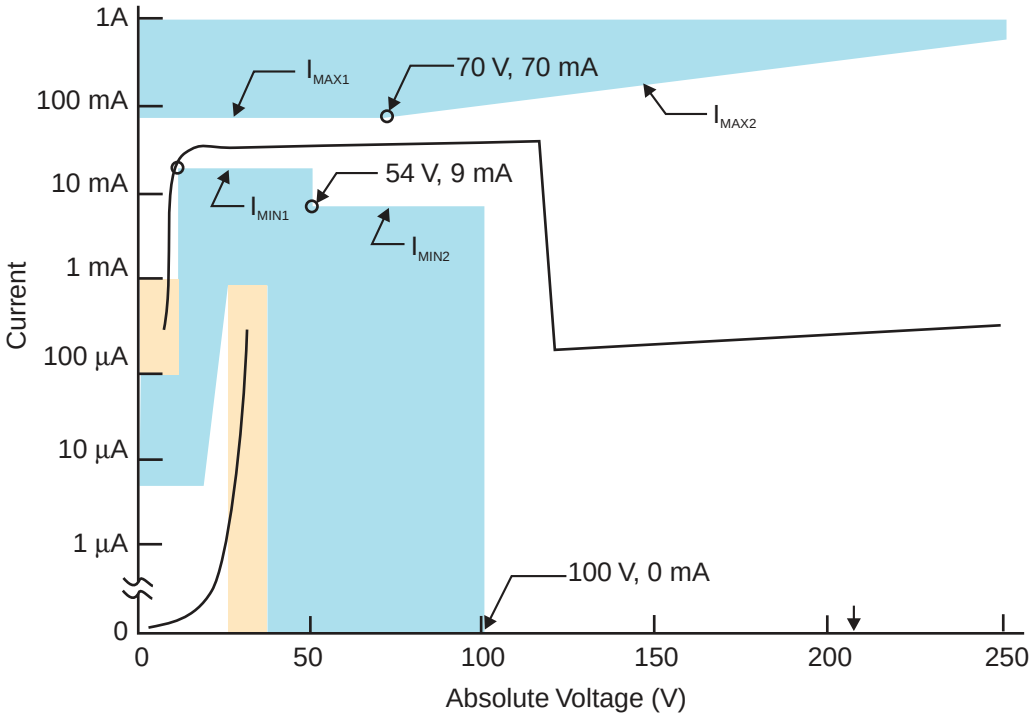
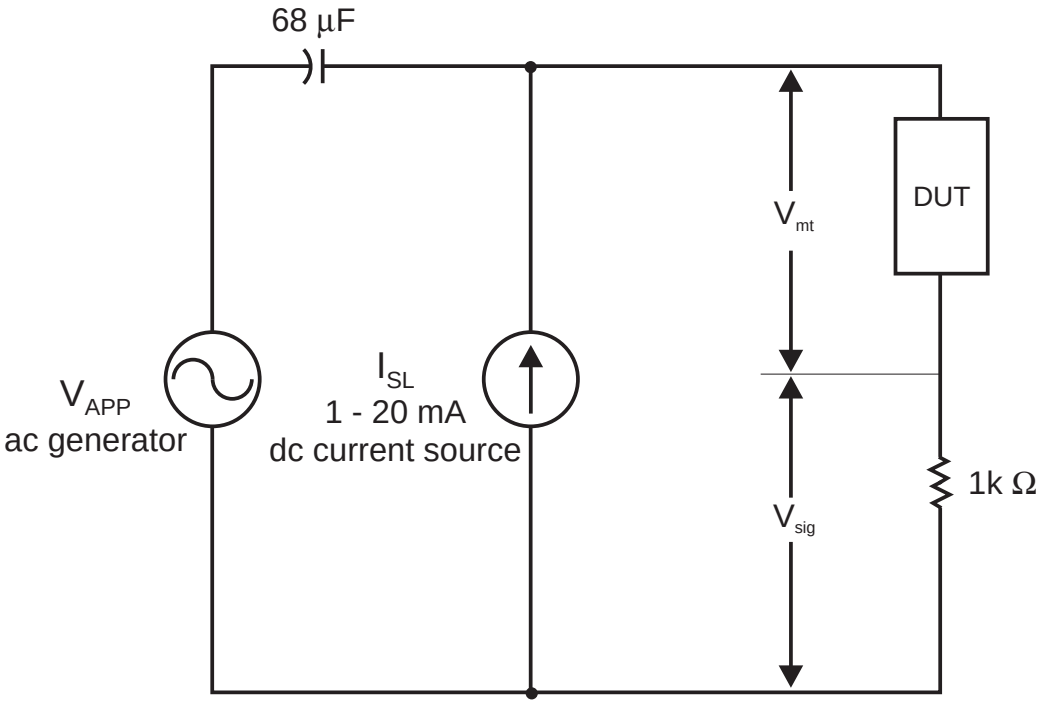


Figure 4. Test Circuit for ac Impedance and Linearity



$$Z_{mt} = \frac{1000 \times V_{mt}}{V_{sig}}$$

$$\text{Linearity} = 20\log\left[\frac{V_{mt}}{V_{sig2ndHarmonic}}\right] + 20\log\left[\frac{1000}{67.5}\right]$$

Figure 5. Test Circuit for Activate and Deactivate Times

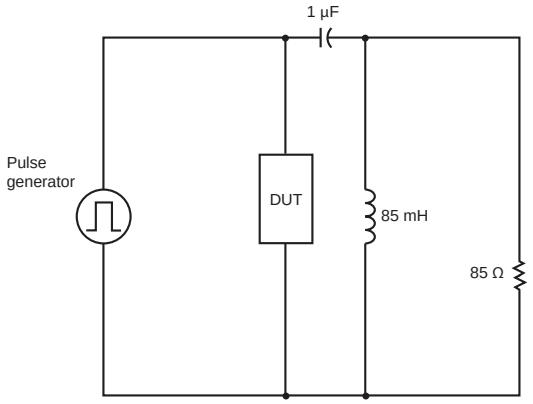


Figure 6. Applied Waveform for Activation Test

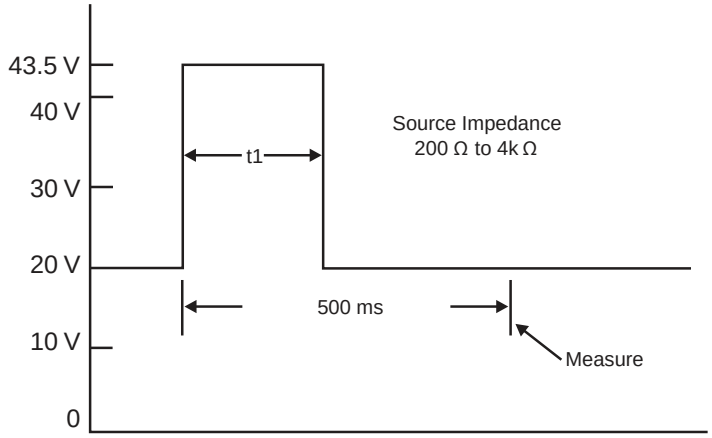
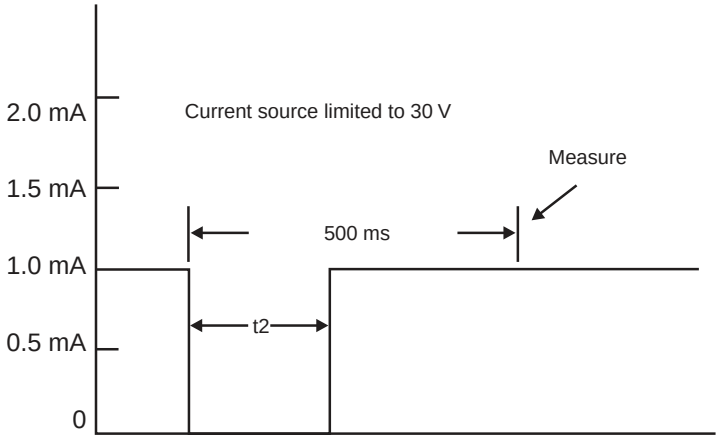


Figure 7. Applied Waveform for Deactivation Test



1.5 Sealing Current Monitor Characteristics

1.5.1 LED Trigger Characteristics

For test conditions: (see Figure 8 on page 8).

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Applied DC battery Voltage	-	-	-43.5	-	-56	V_{DC}
Frequency (pulses per second)	-	-	4	-	8	-
Percent break	-	-	40	-	60	%
Number of pulses	-	-	6	-	10	-
Total Loop Resistance	-	-	200	-	4000	Ω
Required opto-coupler response						
Number of applied pulses per make/break	-	-	-	1	-	-
Pulse width (opto on)	(see Figure 8 on page 8)	T_{ON}	10	-	-	ms
Pulse width (opto off)	(see Figure 8 on page 8)	T_{OFF}	10	-	-	ms

Figure 8. Test Circuit for LED Operation

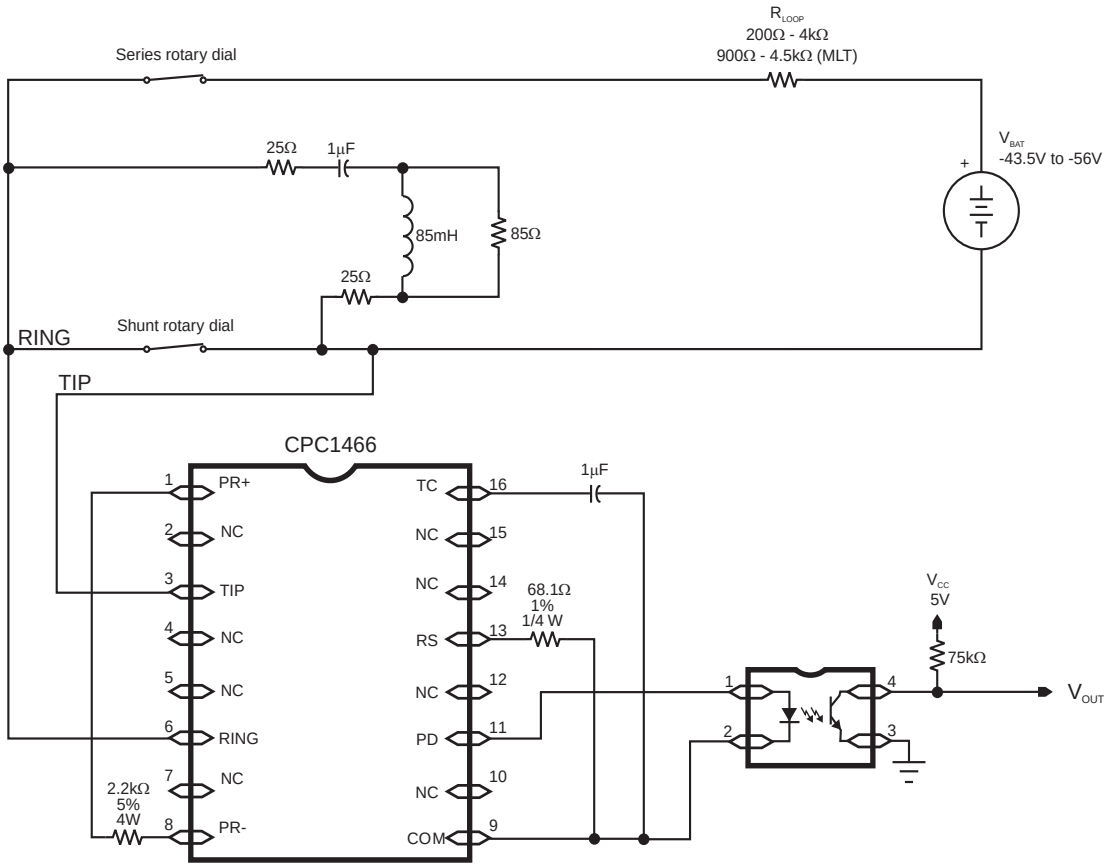
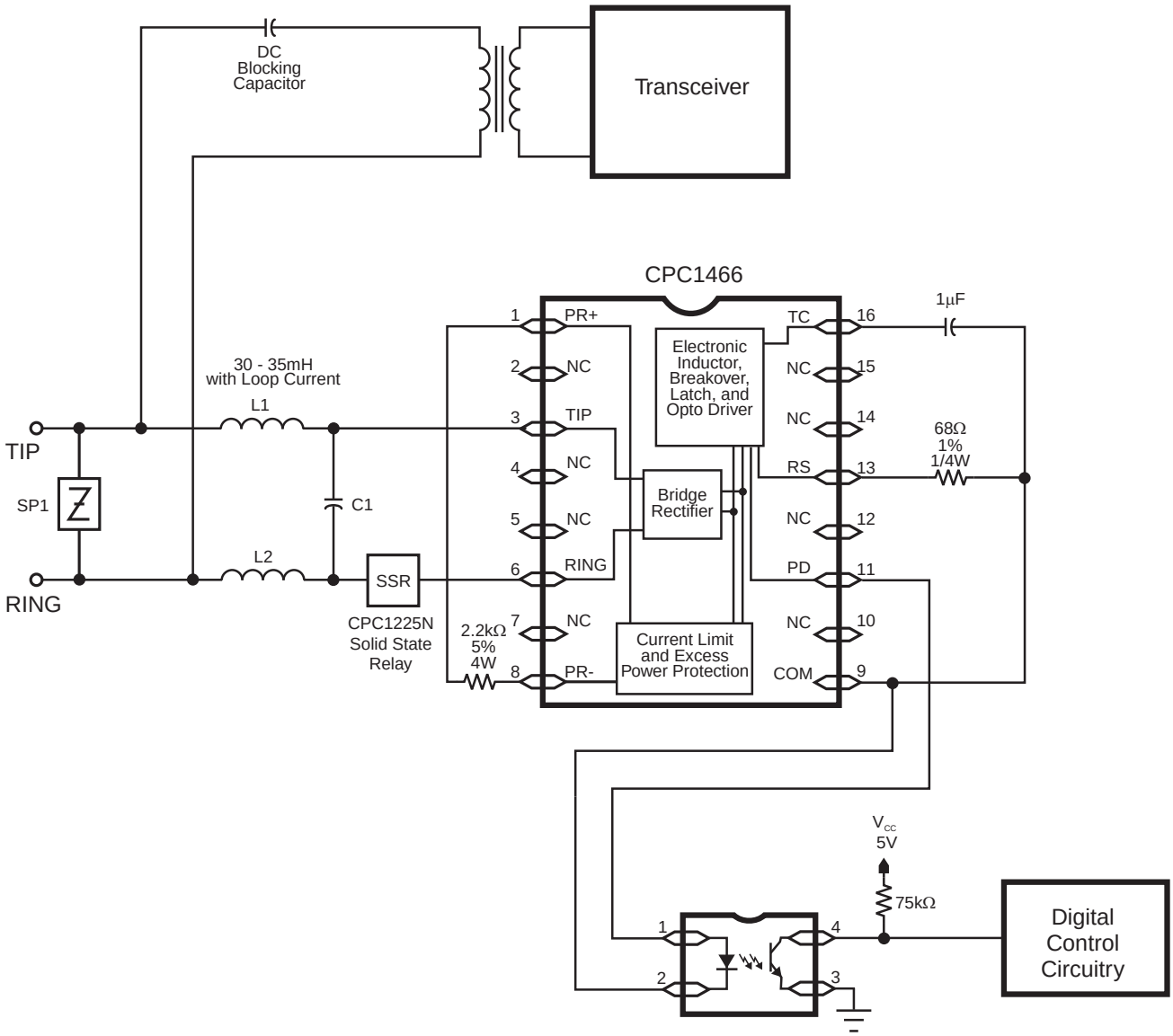


Figure 9. Typical ADSL/VDSL Application Diagram



2. Functional Description

2.1 Introduction

The CPC1466 can be used for a number of DSL designs requiring a DC-hold circuit such as ADSL modem applications. Typical ADSL applications will use a filter circuit design similar to the one shown in **Figure 9, "Typical ADSL/VDSL Application Diagram" on page 9**.

The DC Termination IC performs two fundamental functions in an ADSL modem application; as an electronic inductor providing a low impedance DC termination with a high impedance ac termination and second as part of the sealing current detection system for automated line sensing. This function provides an excellent method to monitor for the presence of sealing current. Generally, loss of sealing current indicates loop loss.

As can be seen in the application circuit in **Figure 9 on page 9**, CPC1466 designs require few external components. For the CPC1466, all that is needed is a circuit protector, two resistors and a capacitor. To ensure DSL signal integrity over a wide variety of conditions a POTS splitter type filter is recommended to isolate the DSL traffic from the termination.

2.2 Surge Protection

Although the CPC1466 self-protects via current limiting, it requires over-voltage surge protection to protect against destructive over-voltage transients. IXYS Integrated Circuits recommends the use of a crowbar-type surge protector to limit the surge voltage seen by the CPC1466 to less than 250 V. The protection device must be able to withstand the surge requirements specified by the appropriate governing agency in regions where the product will be deployed. Littelfuse, Inc. makes suitable surge protectors for most applications. Devices such as Littelfuse's P1800SDL or P2000SDL SIDACtor devices should provide suitable protection.

2.3 Bridge Rectifier

The bridge rectifier in the CPC1466 ensures that the device is polarity-insensitive and provides consistent operational characteristics if the TIP/RING circuit polarity is reversed.

2.4 State Transitions

The DC TIP/RING voltage-current characteristics of the CPC1466 are shown in **Figure 2, "I-V Requirements Template, 0 V to 50 V"**, and in **Figure 3, "I-V Requirements Template, 0 V to 250 V" on page 5**.

Transition timings are illustrated in **Figure 6, "Applied Waveform for Activation Test"**, and in **Figure 7, "Applied Waveform for Deactivation Test"**. The test configuration for these timings is given in **Figure 5, "Test Circuit for Activate and Deactivate Times"**. All timing figures are located on **page 7**.

State transition timings are set by the 1 μF capacitor connected between the TC and COM pins.

2.4.1 Activation - On-State

Application of battery voltage to the loop causes the CPC1466 to conduct whenever the voltage exceeds approximately 35 V. With application of sufficient voltage applied across the TIP/RING terminals, the CPC1466 will initially conduct a nominal 150 μA of sealing current for approximately 20 ms prior to activation. Once activated, the CPC1466 will remain in the on state for as long as the loop current exceeds a nominal 0.5 mA.

The CPC1466 turn-on timing circuit assures device activation will occur within 50 ms of an applied voltage greater than 43.5 V but not within the first 3 ms.

2.4.2 Deactivation - Off-State

While the CPC1466 activation protocol is based on an initial minimum voltage level, deactivation is based on a diminished sealing current level. Deactivation occurs when the nominal sealing current level drops below 0.5 mA with guaranteed deactivation occurring for sealing current levels less than 0.1 mA

The turn-off timing circuit deactivates the sealing current hold circuit when 1 mA of sealing current has been removed for 100 ms but ignores periods of loss up to 3 ms.

2.5 Photo-Diode (PD) Output Behavior

Output from the PD pin provides a minimum of 0.2 mA of photodiode drive current for an optocoupler's LED anytime sealing current exceeds 1 mA.

Because LED current is interrupted whenever loop current is interrupted, the optocoupler provides an excellent means of indicating loop availability for designs with a full time sealing current requirement. In addition, for pulsed sealing current loops, the status from this detector when used in conjuntion with the timing of modem retraining events can be used as an indicator to determine if the sealing current event is clearing line impairments.

2.6 On-State Behavior

2.6.1 Typical Conditions

On-state sealing current levels are determined by the network's power feed circuit and the loop's DC impedance. To compensate for low loop resistance or very high loop voltage, the CPC1466 limits the maximum sealing current to 70 mA.

The CPC1466 manages package power dissipation by shunting excess sealing current through the 2.2 kΩ 4W power resistor located between the PR+ and PR- pins.

2.6.2 Over-Voltage Conditions

Potentials in excess of 100 V applied to the TIP/RING interface will cause the CPC1466 to disable the sealing current hold circuit and enter a standby state with very little current draw. Once the over-voltage condition is removed, the CPC1466 automatically resumes normal operation.

3. Manufacturing Information

3.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
CPC1466M	MSL 3
CPC1466D	MSL 1

3.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

3.3 Reflow Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be (T_C - 5)ºC or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of **J-STD-020** must be observed.

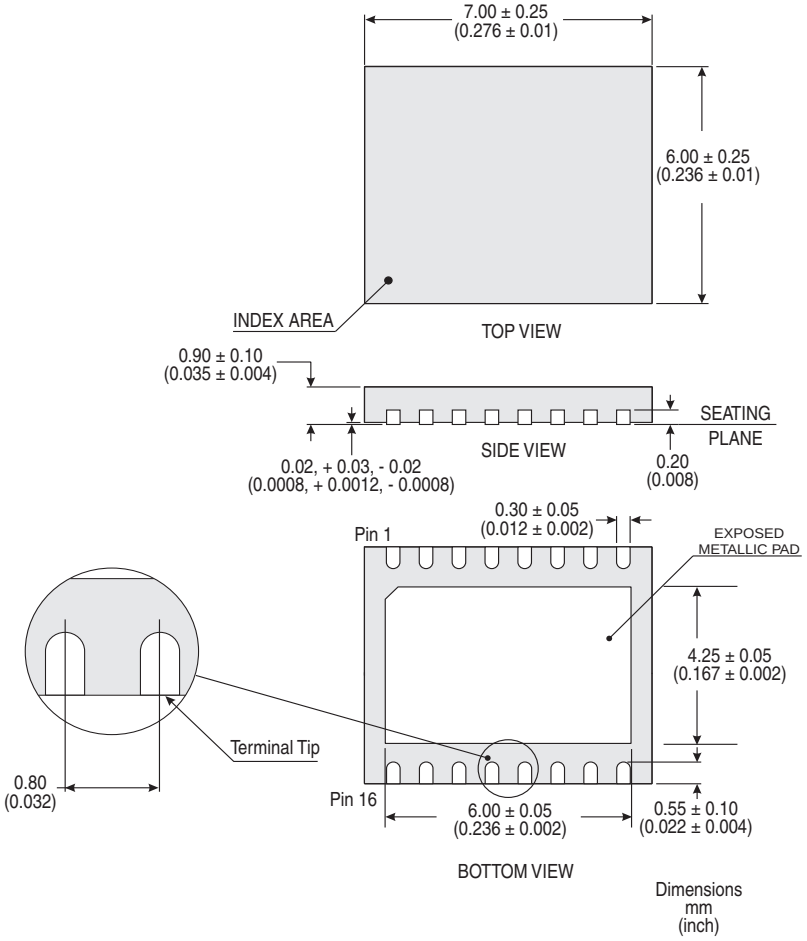
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
CPC1466M / CPC1466D	260°C	30 seconds	3

3.4 Board Wash

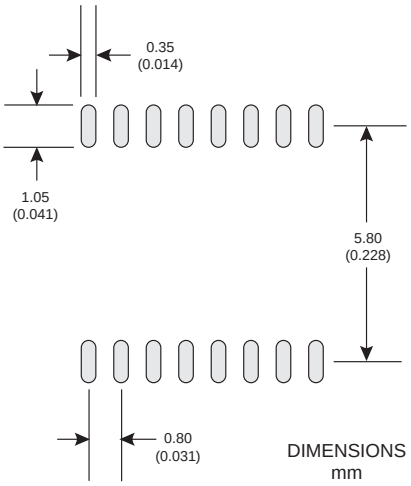
IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

3.5 Mechanical Dimensions

3.5.1 CPC1466M 16-Pin DFN Package

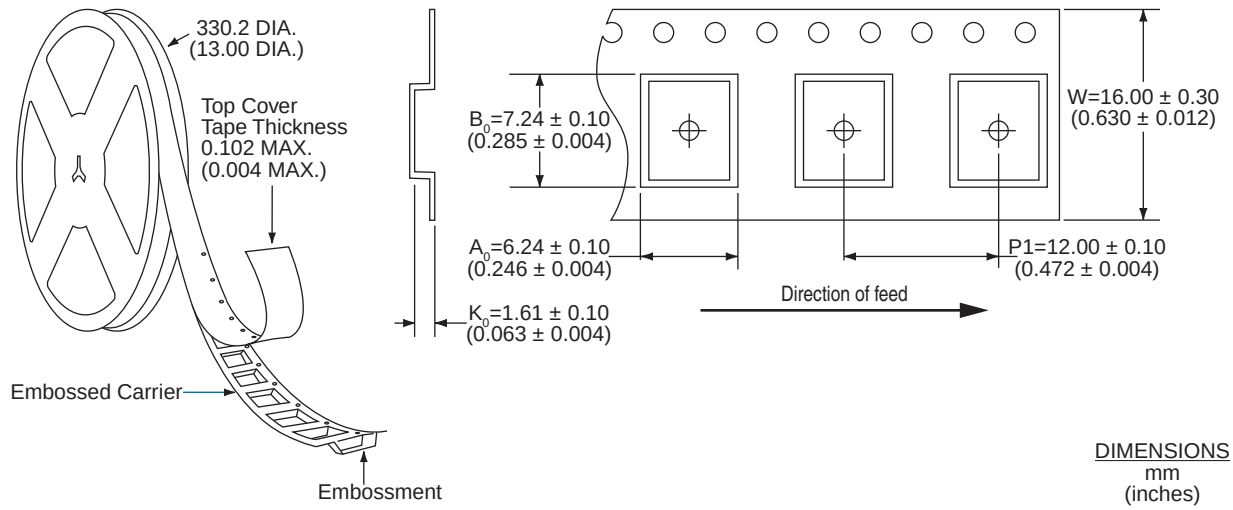


Recommended PCB Land Pattern

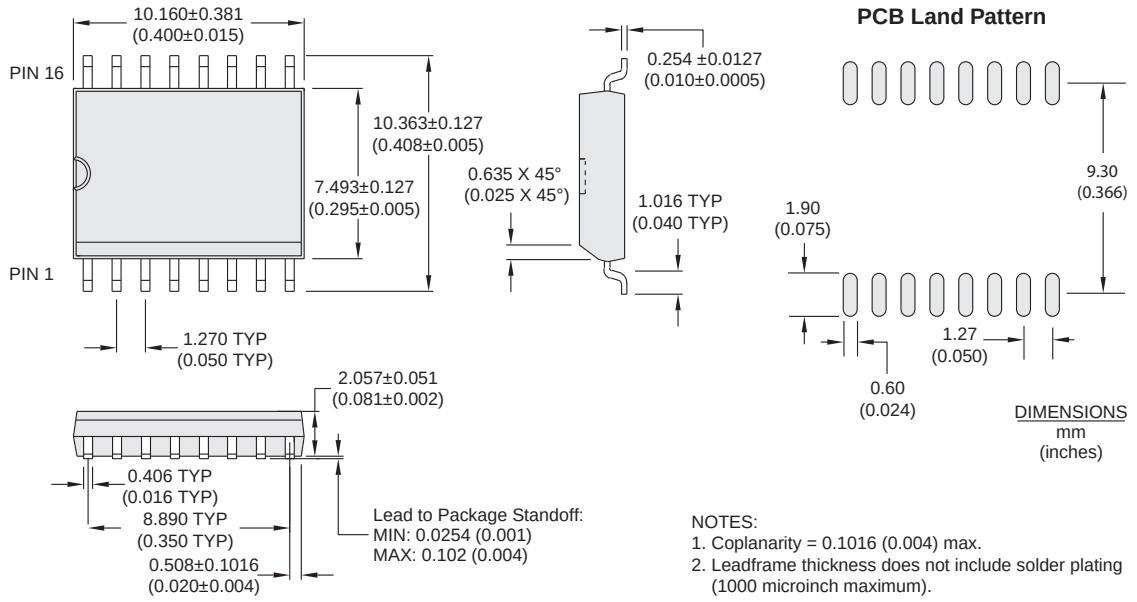


NOTE: Because the metallic pad on the bottom of the DFN package is connected to the substrate of the die, it is recommended that no printed circuit board traces or vias be placed under this area.

3.5.2 CPC1466MTR 16-Pin DFN Tape & Reel

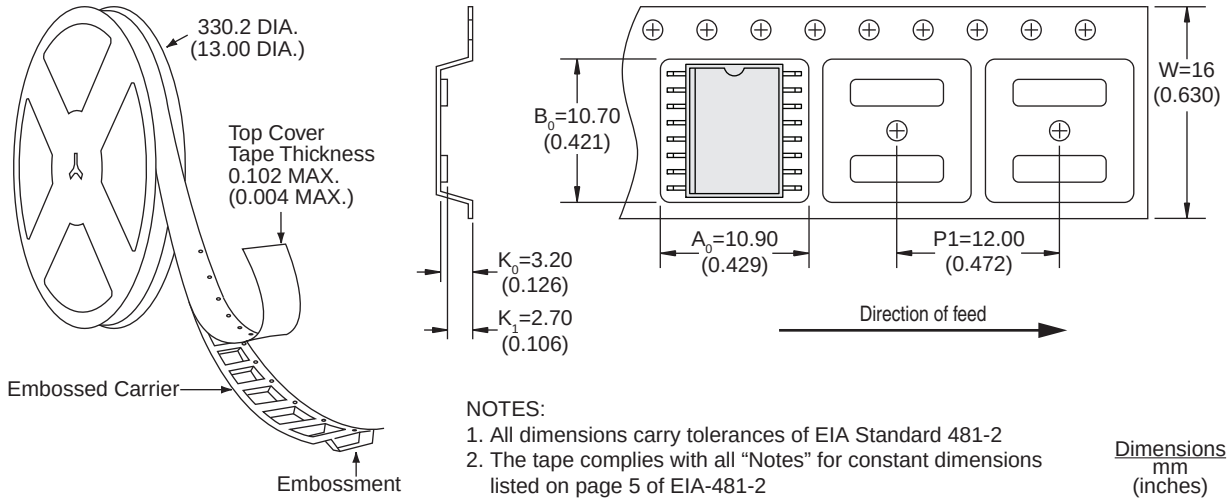


3.5.3 CPC1466D 16-Pin SOIC Package



NOTES:
1. Coplanarity = 0.1016 (0.004) max.
2. Leadframe thickness does not include solder plating (1000 microinch maximum).

3.5.4 CPC1466DTR 16-Pin SOIC Tape & Reel



NOTES:
1. All dimensions carry tolerances of EIA Standard 481-2
2. The tape complies with all "Notes" for constant dimensions listed on page 5 of EIA-481-2

Dimensions
mm
(inches)

For additional information please visit www.ixysic.com

Specifications: DS-CPC1466-R03

8/14/2018