

CMP04—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ $V_+ = 5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{OS}	$R_S = 0\ \Omega$, $R_L = 5.1\text{ k}\Omega$, $V_O = 1.4\text{ V}^1$		0.4	1	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$, $R_L = 5.1\text{ k}\Omega$, $V_O = 1.4\text{ V}$		2	10	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$		25	100	nA
Voltage Gain	A_V	$R_L \geq 15\text{ k}\Omega$, $V_+ = 15\text{ V}^2$	80	200		V/mV
Large Signal Response Time	t_r	$V_{IN} = \text{TTL Logic Swing}$, $V_{REF} = 1.4\text{ V}^3$ $V_{RL} = 5\text{ V}$, $R_L = 5.1\text{ k}\Omega$		300		ns
Small Signal Response Time	t_r	$V_{IN} = 100\text{ mV Step}^3$, 5 mV Overdrive $V_{RL} = 5\text{ V}$, $R_L = 5.1\text{ k}\Omega$		1.3		μs
Input Voltage Range	CMVR	Note 4	0		$V_+ - 1.5$	V
Common-Mode Rejection Ratio	CMRR	Notes 2, 5	80	100		dB
Power Supply Rejection Ratio	PSRR	$V_+ = 5\text{ V to }18\text{ V}^2$	80	100		dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1\text{ V}$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4\text{ mA}$		250	400	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1\text{ V}$, $V_{IN}(+) = 0$, $V_O \leq 1.5\text{ V}$	6	16		mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1\text{ V}$, $V_{IN}(-) = 0$, $V_O = 30\text{ V}$		0.1	100	nA
Supply Current	I_+	$R_L = \infty$, All Comps $V_+ = 30\text{ V}$		0.8	2.0	mA

NOTES

¹At output switch point, $V_O = 1.4\text{ V}$, $R_S = 0\ \Omega$ with V_+ from 5 V , and over the full input common-mode range (0 V to $V_+ - 1.5\text{ V}$).

²Guaranteed by design.

³Sample tested.

⁴The input common-mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $V_+ - 1.5\text{ V}$, but either or both inputs can go to 30 V without damage.

⁵ $R_L \geq 15\text{ k}\Omega$, $V_+ = 15\text{ V}$, $V_{CM} = 1.5\text{ V}$ to 13.5 V .

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	+36 V or $\pm 18\text{ V}$
Differential Input Voltage	36 V dc
Input Voltage	-0.3 V to $+36\text{ V}$
Operating Temperature Range	
CMP04FSZ	-40°C to $+85^\circ\text{C}$
Junction Temperature (T_J)	-65°C to $+150^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Input Current ($V_{IN} < -3.0\text{ V}$)	50 mA
Output Short Circuit to GND	Continuous
Lead Temperature (Soldering, 60 sec)	300°C

Package Type	θ_{JA}^2	θ_{JC}	Unit
14-Lead SOIC	120	36	$^\circ\text{C/W}$

NOTES

¹Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

² θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the CMP04 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ELECTRICAL CHARACTERISTICS (@ $V_+ = 5\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for CMP04FSZ, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	CMP04FSZ ¹ Typ	Max	Unit
Input Offset Voltage	V_{OS}	$R_S = 0\ \Omega$, $R_L = 5.1\text{ k}\Omega$		1	2	mV
		$V_O = 1.4\text{ V}^2$		1	2	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$		4	20	nA
		$R_L = 5.1\text{ k}\Omega$		4	20	nA
		$V_O = 1.4\text{ V}$		4	20	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$		40	200	nA
Voltage Gain	A_V	$R_L \geq 15\text{ k}\Omega$, $V_+ = 15\text{ V}^3$	70	125		V/mV
Large Signal Response Time	t_r	$V_{IN} = \text{TTL Logic Swing}$		300		ns
		$V_{REF} = 1.4\text{ V}^4$		300		ns
		$V_{RL} = 5\text{ V}$, $R_L = 5.1\text{ k}\Omega$		300		ns
Small Signal Response Time	t_r	$V_{IN} = 100\text{ mV Step}^4$		1.3		μs
		5 mV Overdrive		1.3		μs
		$V_{RL} = 5\text{ V}$, $R_L = 5.1\text{ k}\Omega$		1.3		μs
Input Voltage Range	CMVR	Note 5	0		$V_+ - 1.5$	V
Common-Mode Rejection Ratio	CMRR	Notes 1, 3	60	100		dB
Power Supply Rejection Ratio	PSRR	$V_+ = 5\text{ V}$ to 18 V	80	100		dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1\text{ V}$, $V_{IN}(+) = 0$,		250	700	mV
		$I_{SINK} \leq 4\text{ mA}$		250	700	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1\text{ V}$,	5	16		mA
		$V_{IN}(+) = 0$, $V_O \leq 1.5\text{ V}$	5	16		mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1\text{ V}$,		0.1	200	nA
		$V_{IN}(-) = 0$, $V_O = 30\text{ V}$		0.1	200	nA
Supply Current	I_+	$R_L = \infty$, All Comps		1.2	3.0	mA
		$V_+ = 30\text{ V}$		1.2	3.0	mA

NOTES

¹ $R_L \geq 15\text{ k}\Omega$, $V_+ = 15\text{ V}$, $V_{CM} = 1.5\text{ V}$ to 13.5 V .²At output switch point, $V_O = 1.4\text{ V}$, $R_S = 0\ \Omega$ with V_+ from 5 V ; and over the full input common-mode range (0 V to $V_+ - 1.5\text{ V}$).³Guaranteed by design.⁴Sample tested.⁵The input common-mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $V_+ - 1.5\text{ V}$, but either or both inputs can go to $+30\text{ V}$ without damage.

Specifications subject to change without notice.

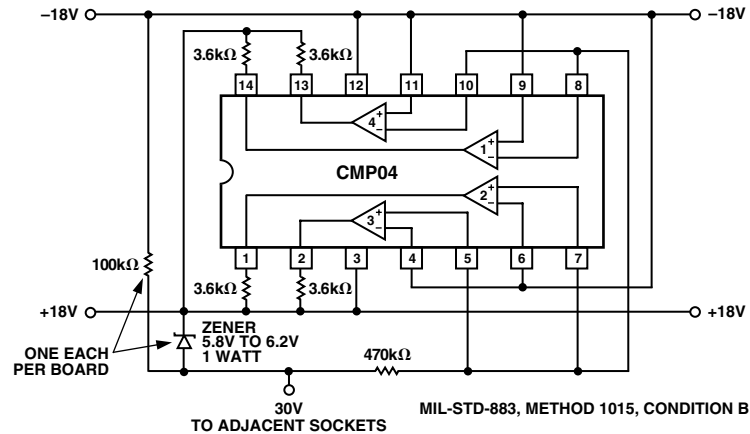
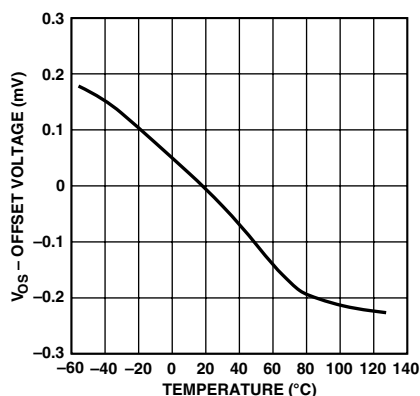
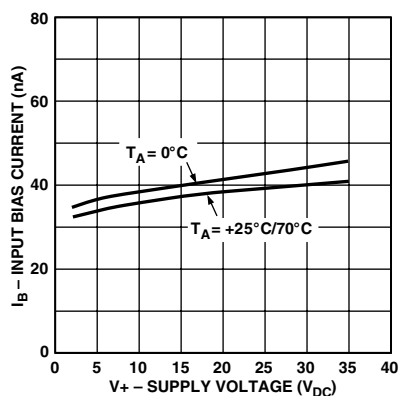


Figure 3. Burn-In Circuit

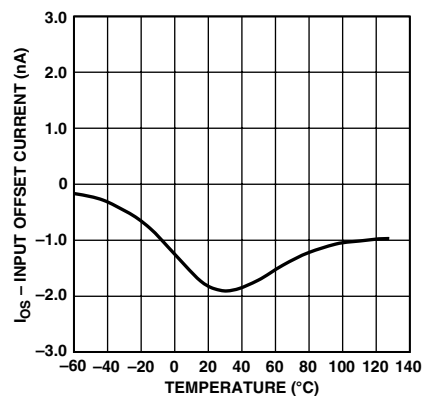
CMP04—Typical Performance Characteristics



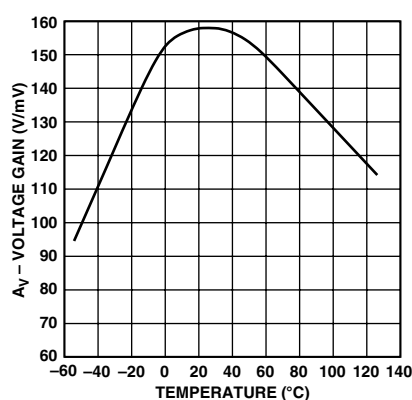
TPC 1. Offset Voltage vs. Temperature



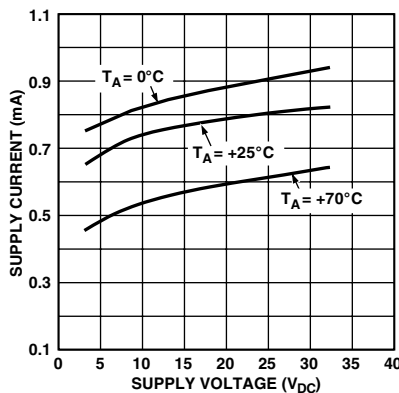
TPC 2. Input Bias Current vs. V_+ and Temperature



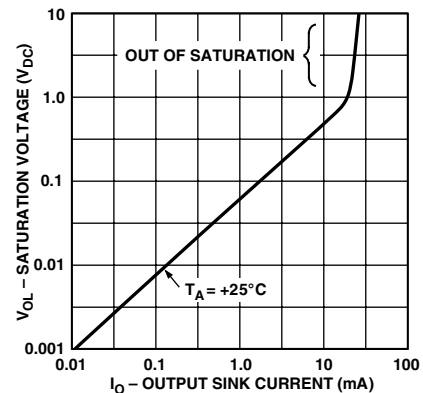
TPC 3. Input Offset Current vs. Temperature



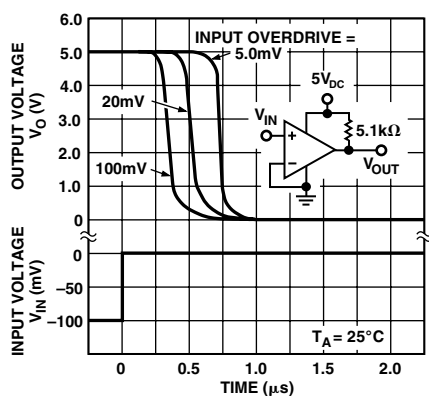
TPC 4. Voltage Gain vs. Temperature



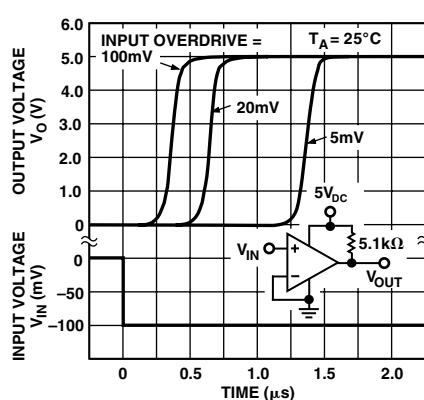
TPC 5. Supply Current vs. Supply Voltage



TPC 6. Output Voltage vs. Output Current and Temperature



TPC 7. Response Time for Various Input Overdrives—Negative Transition



TPC 8. Response Time for Various Input Overdrives—Positive Transition

TYPICAL APPLICATIONS

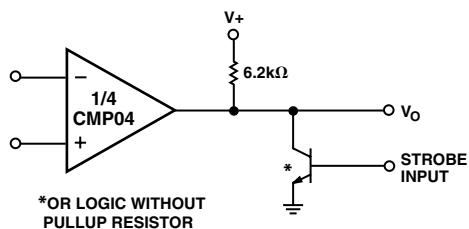


Figure 4. Output Strobging

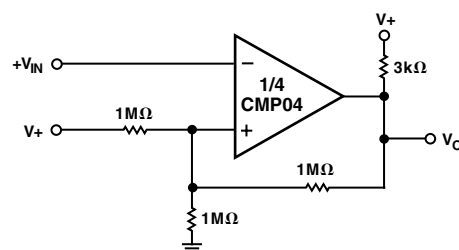


Figure 7. Inverting Comparator with Hysteresis

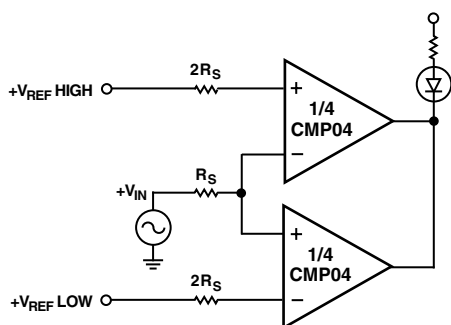


Figure 5. Limit Comparator

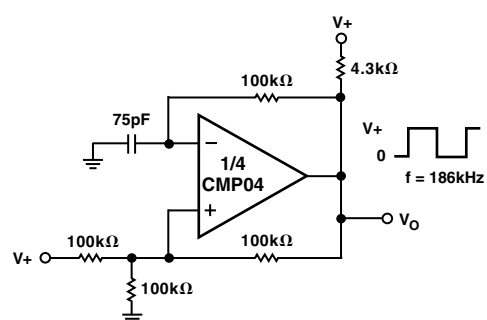


Figure 8. Square Wave Oscillator

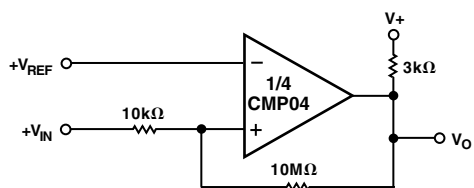


Figure 6. Noninverting Comparator with Hysteresis

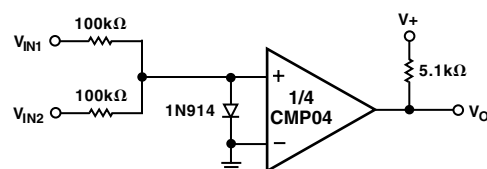


Figure 9. Comparing Input Voltages of Opposite Polarity

CMP04

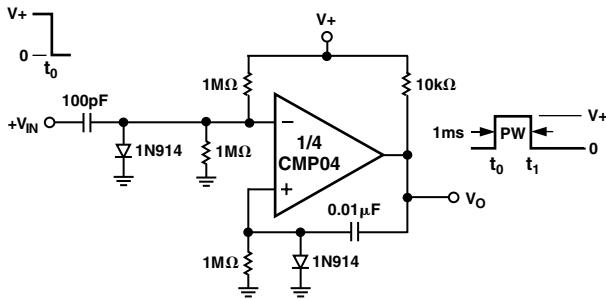


Figure 10. One-Shot Multivibrator

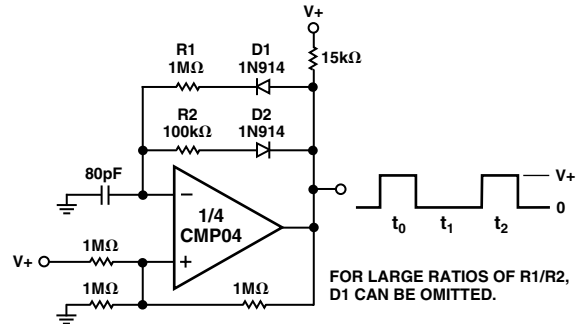


Figure 12. Pulse Generator

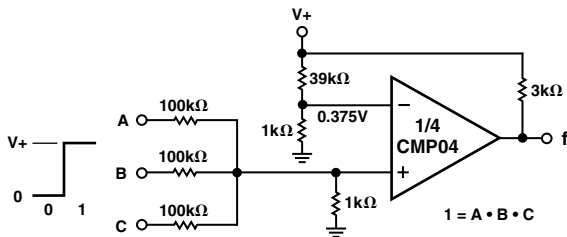


Figure 11. AND Gate

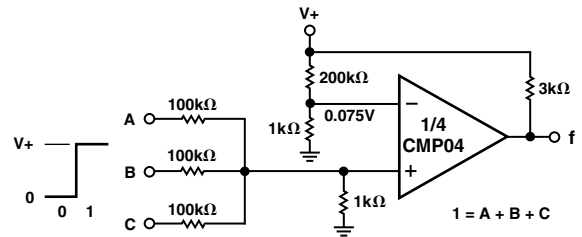


Figure 13. OR Gate

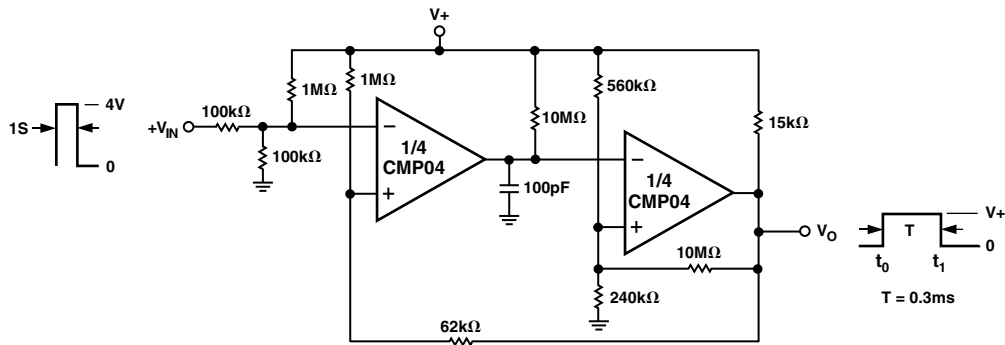
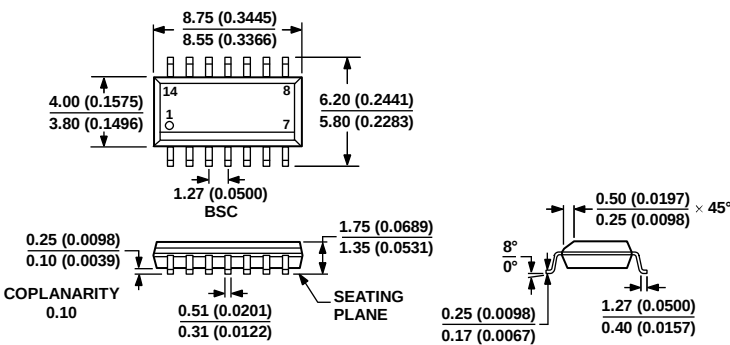


Figure 14. One-Shot Multivibrator with Input Lockout



OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 16. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model ¹	T _A = 25°C, V _{OS}	Temperature Range	Package Description	Package Option
CMP04FSZ	1 mV	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
CMP04FSZ-REEL	1 mV	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14

¹ Z = RoHS Compliant Part.

REVISION HISTORY

10/2018—Rev. D to Rev. E

Changed CMP04FS and CMP04F to CMP04FSZ Throughout
Updated Outline Dimensions.....8
Moved Ordering Guide8
Changes to Ordering Guide.....8

3/2003—REV. C to REV. D

Renumbered TPCs and Figures..... Global
Deletion of 14-Lead Cerdip and 14-Lead PDIP
Information Global

Changes to Features	1
Changes to Pin Connections	1
Changes to Absolute Maximum Ratings.....	2
Changes to Ordering Guide	2
Changes to Electrical Characteristics.....	3
Removal of Dice Characteristics, Wafer Test Limits, and Typical Electrical Characteristics Sections	4
Changes to TPCs 2, 5, and 6	4
Updated Outline Dimensions.....	8