

CD4538BC Dual Precision Monostable

General Description

The CD4538BC is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are internally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active LOW and prevent triggering while active. Precise control of output pulse-width has been achieved using linear CMOS techniques. The pulse duration and accuracy are determined by external components R_X and C_X . The device does not allow the timing capacitor to discharge through the timing pin on power-down condition. For this reason, no external protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

Features

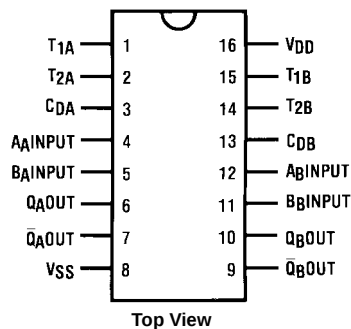
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: $0.45 V_{CC}$ (typ.)
- Low power TTL compatibility:
Fan out of 2 driving 74L or 1 driving 74LS
- New formula:
 $PW_{OUT} = RC$ (PW in seconds, R in Ohms, C in Farads)
- $\pm 1.0\%$ pulse-width variation from part to part (typ.)
- Wide pulse-width range: $1 \mu s$ to ∞
- Separate latched reset inputs
- Symmetrical output sink and source capability
- Low standby current: 5 nA (typ.) @ $5 V_{DC}$
- Pin compatible to CD4528BC

Ordering Code:

Order Number	Package Number	Package Description
CD4538BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4538BCWM	M16B	16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
CD4538BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

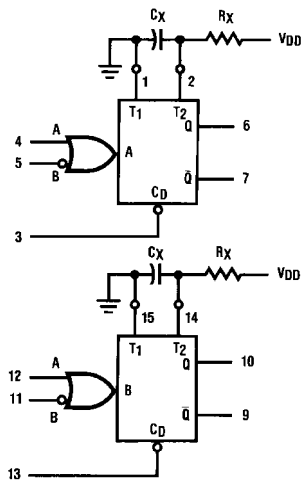


Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⌋	⌋
H	↑	H	⌋	⌋

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⌋ = One HIGH Level Pulse
⌋ = One LOW Level Pulse
X = Irrelevant

Block Diagram



R_X and C_X are External Components

V_{DD} = Pin 16

V_{SS} = Pin 8

Logic Diagram

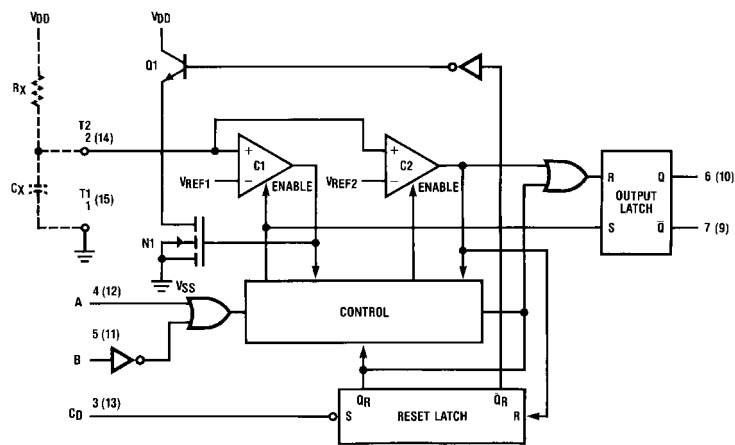


FIGURE 1.

Theory of Operation

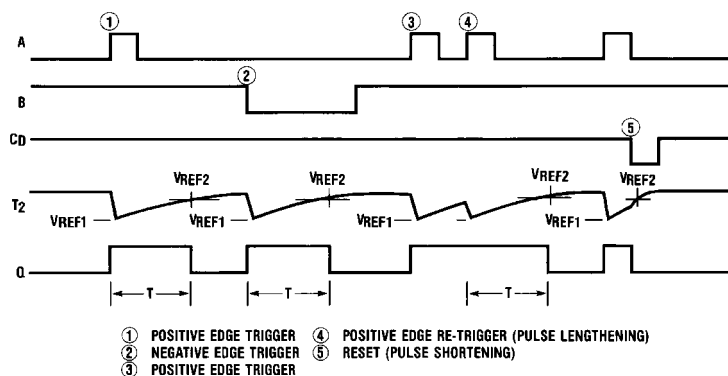


FIGURE 2.

Trigger Operation

The block diagram of the CD4538BC is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and Figure 2, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD} . When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_D are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1⁽¹⁾. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X , toward V_{DD} . When the voltage across C_X equals V_{REF2} , comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from V_{DD} to V_{SS} (while input A is at V_{SS} and input C_D is at V_{DD})⁽²⁾.

It should be noted that in the quiescent state C_X is fully charged to V_{DD} , causing the current through resistor R_X to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the CD4538BC is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X , R_X , or the duty cycle of the input waveform.

Retrigger Operation

The CD4538BC is retriggered if a valid trigger occurs⁽³⁾ followed by another valid trigger⁽⁴⁾ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V_{REF1} , but has not yet reached V_{REF2} , will cause an increase in output pulse width T. When a valid retrigger is initiated⁽⁴⁾, the voltage at T2 will again drop to V_{REF1} before progressing along the RC charging curve toward V_{DD} . The Q output will remain high until time T, after the last valid retrigger.

Reset Operation

The CD4538BC may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on C_D sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor Q1⁽⁵⁾. When the voltage on the capacitor reaches V_{REF2} , the reset latch will clear and then be ready to accept another pulse. If the C_D input is held low, any trigger inputs that occur will be inhibited and the Q and $\bar{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

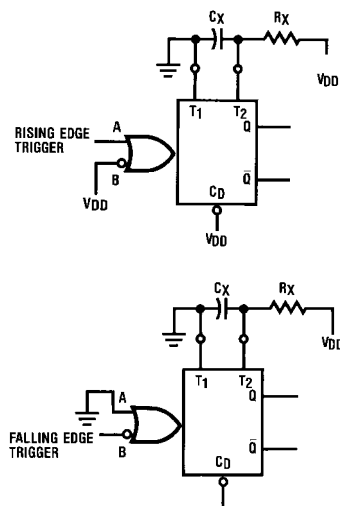


FIGURE 3. Retriggerable Monostables Circuitry

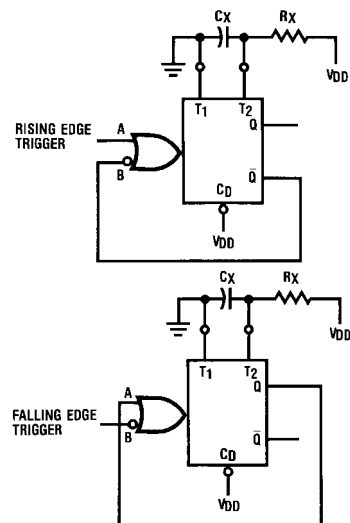


FIGURE 4. Non-Retriggerable Monostables Circuitry

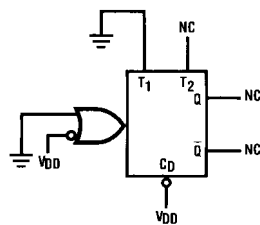


FIGURE 5. Connection of Unused Sections

Absolute Maximum Ratings(Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	-0.5 to +18 V_{DC}
Input Voltage (V_{IN})	-0.5V to $V_{DD} + 0.5 V_{DC}$
Storage Temperature Range (T_S)	-65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating**Conditions** (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to $V_{DD} V_{DC}$
Operating Temperature Range (T_A)	-55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$ $V_{IH} = V_{DD}$ $V_{DD} = 10V$ $V_{IL} = V_{SS}$ $V_{DD} = 15V$ All Outputs Open		20 40 80		0.005 0.010 0.015	5 10 20		150 300 600	μA
V_{OL}	LOW Level Output Voltage	$V_{DD} = 5V$ $ I_{OL} < 1 \mu A$ $V_{DD} = 10V$ $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$ $V_{DD} = 15V$		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	V
V_{OH}	HIGH Level Output Voltage	$V_{DD} = 5V$ $ I_{OL} < 1 \mu A$ $V_{DD} = 10V$ $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$ $V_{DD} = 15V$	4.95 9.95 14.95		4.95 9.95 14.95	5 10 15		4.95 9.95 14.95		V
V_{IL}	LOW Level Input Voltage	$ I_{OL} < 1 \mu A$ $V_{DD} = 5V$, $V_O = 0.5V$ or 4.5V $V_{DD} = 10V$, $V_O = 1.0V$ or 9.0V $V_{DD} = 15V$, $V_O = 1.5V$ or 13.5V		1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	V
V_{IH}	HIGH Level Input Voltage	$ I_{OL} < 1 \mu A$ $V_{DD} = 5V$, $V_O = 0.5V$ or 4.5V $V_{DD} = 10V$, $V_O = 1.0V$ or 9.0V $V_{DD} = 15V$, $V_O = 1.5V$ or 13.5V	3.5 7.0 11.0		3.5 7.0 11.0	2.75 5.50 8.25		3.5 7.0 11.0		V
I_{OL}	LOW Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$ $V_{IH} = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$ $V_{IL} = V_{SS}$ $V_D = 15V$, $V_O = 1.5V$	0.64 1.6 4.2		0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4		mA
I_{OH}	HIGH Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$ $V_{IL} = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$ $V_D = 15V$, $V_O = 13.5V$	-0.6 -1.6 -4.2		-0.51 -1.3 -3.4	-0.88 -2.25 -8.8		-0.36 -0.9 -2.4		mA
I_{IN}	Input Current, Pin 2 or 14	$V_{DD} = 15V$, $V_{IN} = 0V$ or 15V		± 0.02		$\pm 10^{-5}$	± 0.05		± 0.5	μA
I_{IN}	Input Current Other Inputs	$V_{DD} = 15V$, $V_{IN} = 0V$ or 15V		± 0.1		$\pm 10^{-5}$	± 0.1		± 1.0	μA

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 4) $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, and $t_r = t_f = 20\text{ ns}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TLH}, t_{THL}	Output Transition Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 50 40	200 100 80	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Trigger Operation— A or B to Q or $\bar{Q}$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ Reset Operation— C_D to Q or $\bar{Q}$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		300 150 100 250 125 95	600 300 220 500 250 190	ns ns
t_{WL}, t_{WH}	Minimum Input Pulse Width A, B, or C_D	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		35 30 25	70 60 50	ns
t_{RR}	Minimum Retrigger Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		0 0 0	0 0 0	ns
C_{IN}	Input Capacitance	Pin 2 or 14 Other Inputs		10 5	7.5	pF
PW_{OUT}	Output Pulse Width (Q or $\bar{Q}$) (Note: For Typical Distribution, see Figure 6)	$R_X = 100\text{ k}\Omega$ $V_{DD} = 5\text{V}$ $C_X = 0.002\text{ }\mu\text{F}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ $R_X = 100\text{ k}\Omega$ $V_{DD} = 5\text{V}$ $C_X = 0.1\text{ }\mu\text{F}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ $R_X = 100\text{ k}\Omega$ $V_{DD} = 5\text{V}$ $C_X = 10.0\text{ }\mu\text{F}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	208 211 216 8.83 9.02 9.20 0.87 0.89 0.91	226 230 235 9.60 9.80 10.00 0.95 0.97 0.99	244 248 254 10.37 10.59 10.80 1.03 1.05 1.07	μs ms s
Pulse Width Match between Circuits in the Same Package $C_X = 0.1\text{ }\mu\text{F}$, $R_X = 100\text{ k}\Omega$		$R_X = 100\text{ k}\Omega$ $V_{DD} = 5\text{V}$ $C_X = 0.1\text{ }\mu\text{F}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		± 1 ± 1 ± 1		%
Operating Conditions						
R_X	External Timing Resistance		5.0		(Note 5)	k Ω
C_X	External Timing Capacitance		0		No Limit	pF

Note 4: AC parameters are guaranteed by DC correlated testing.**Note 5:** The maximum usable resistance R_X is a function of the leakage of the Capacitor C_X , leakage of the CD4538BC, and leakage due to board layout, surface resistance, etc.

Typical Applications

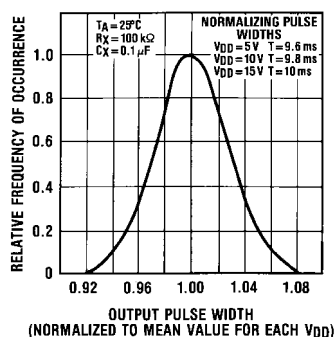


FIGURE 6. Typical Normalized Distribution of Units for Output Pulse Width

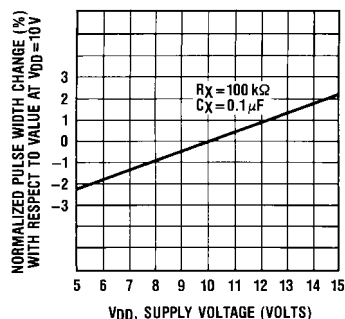


FIGURE 7. Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}

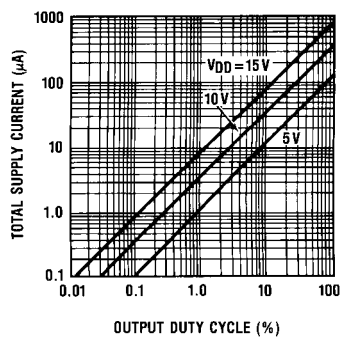


FIGURE 8. Typical Total Supply Current Versus Output Duty Cycle, $R_X = 100\text{ k}\Omega$, $C_L = 50\text{ pF}$, $C_X = 100\text{ pF}$, One Monostable Switching Only

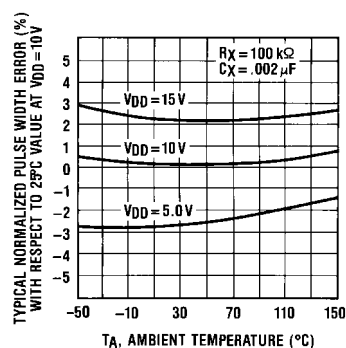


FIGURE 9. Typical Pulse Width Error Versus Temperature

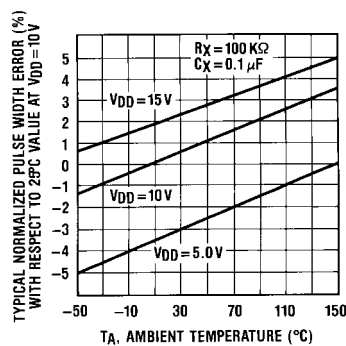


FIGURE 10. Typical Pulse Width Error Versus Temperature

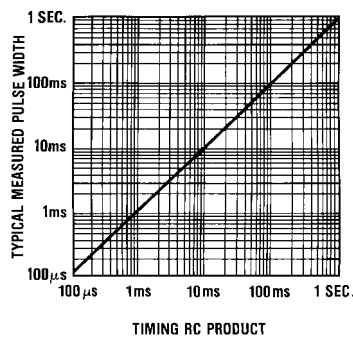


FIGURE 11. Typical Pulse Width Versus Timing RC Product

Test Circuits and Waveforms

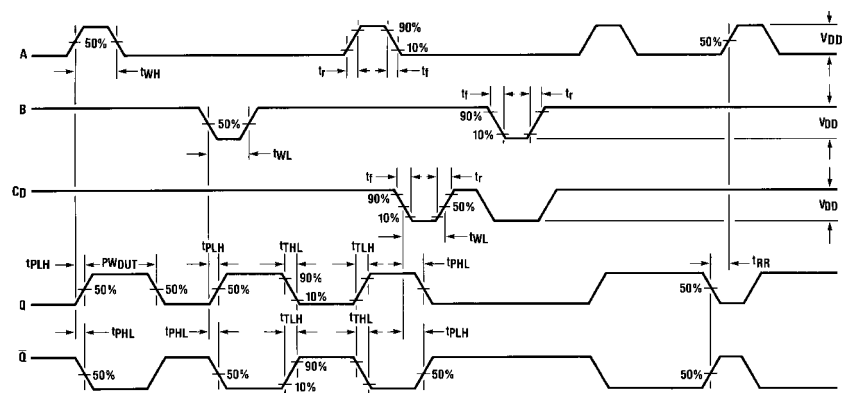
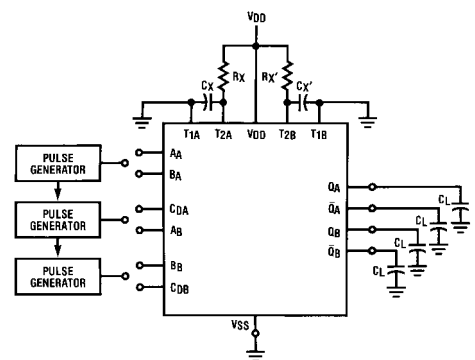


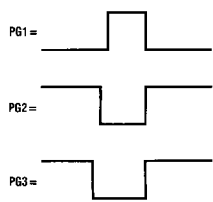
FIGURE 12. Switching Test Waveforms



*C_L = 50 pF

Input Connections

Characteristics	CD	A	B
t _{PLH} , t _{PHL} , t _{TLH} , t _{THL} PW _{OUT} , t _{WH} , t _{WL}	V _{DD}	PG1	V _{DD}
t _{PLH} , t _{PHL} , t _{TLH} , t _{THL} PW _{OUT} , t _{WH} , t _{WL}	V _{DD}	V _{SS}	PG2
t _{PLH(R)} , t _{PHL(R)} , t _{WH} , t _{WL}	PG3	PG1	PG2

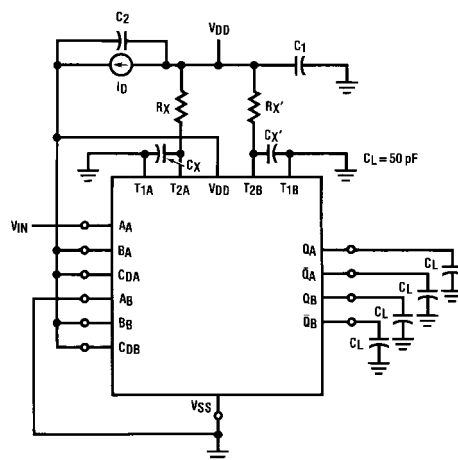


*Includes capacitance of probes, wiring, and fixture parasitic

Note: Switching test waveforms for PG1, PG2, PG3 are shown in Figure 12.

FIGURE 13. Switching Test Circuit

Test Circuits and Waveforms (Continued)



$$R_X = R_{X'} = 100 \text{ k}\Omega$$

$$C_X = C_{X'} = 100 \text{ pF}$$

$$C_1 = C_2 = 0.1 \text{ }\mu\text{F}$$

Duty Cycle = 50%

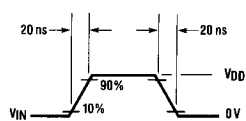
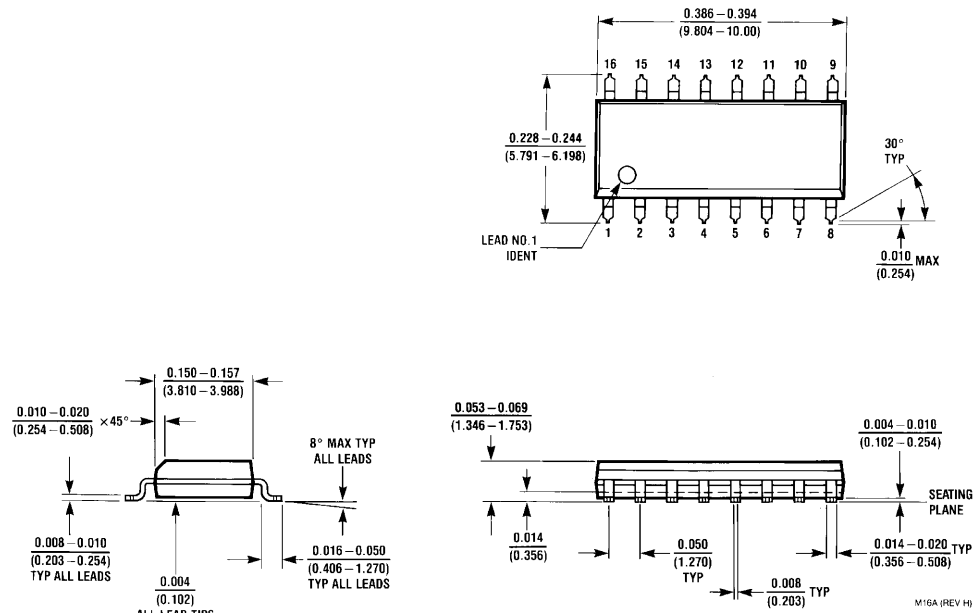
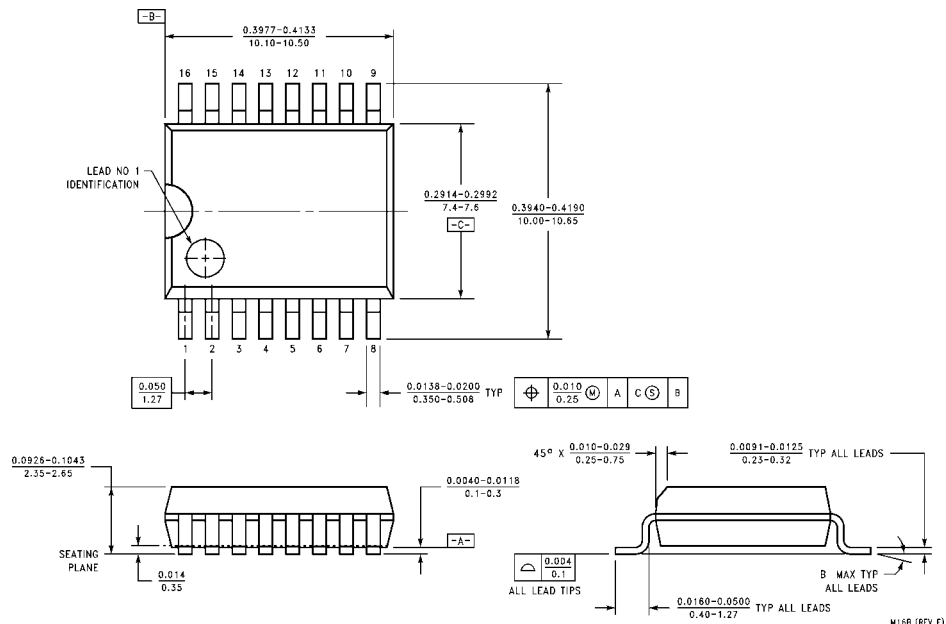


FIGURE 14. Power Dissipation Test Circuit and Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

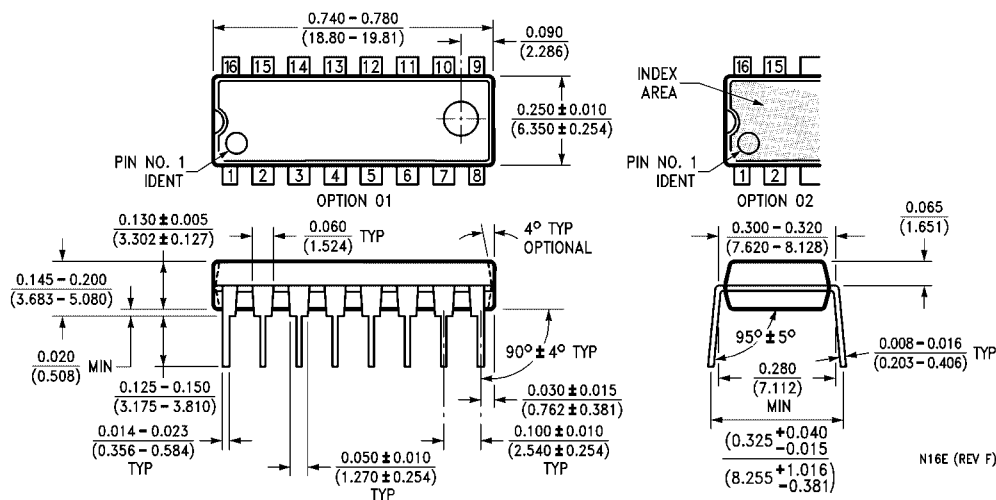


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A



16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M16B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative