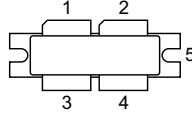
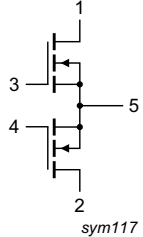
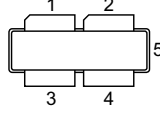
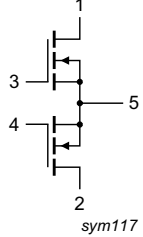


2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF888E (SOT539A)			
1	drain1 (peak)		
2	drain2 (main)		
3	gate1 (peak)		
4	gate2 (main)		
5	source [1]		
BLF888ES (SOT539B)			
1	drain1 (peak)		
2	drain2 (main)		
3	gate1 (peak)		
4	gate2 (main)		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF888E	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF888ES	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS(amp)main}$	main amplifier drain-source voltage		-	104	V
$V_{DS(amp)peak}$	peak amplifier drain-source voltage		-	120	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		-0.5	+11	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-6	+11	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	^[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 90\text{ }^{\circ}\text{C}$; $V_{DS} = 50\text{ V}$; $I_{DS} = 3\text{ A}$ (main); $I_{DS} = 0\text{ A}$ (peak) [1]	0.29	K/W
		$T_{case} = 90\text{ }^{\circ}\text{C}$; $V_{DS} = 50\text{ V}$; $P_L = 150\text{ W}$; $PAR = 8\text{ dB}$ [2]	0.19	K/W

[1] Measured under DC test conditions, with peak section off.

[2] Measured in an ultra-wide Doherty application, using DVB-T (8k OFDM) signal, PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^{\circ}\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 2.4\text{ mA}$	104	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 240\text{ mA}$	1.25	1.75	2.25	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	38	-	A
I_{GSS}	gate leakage current	$V_{GS} = 10\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 8.5\text{ A}$	-	120	-	$\text{m}\Omega$
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 3.6\text{ mA}$	125	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 360\text{ mA}$	1.33	1.83	2.33	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	57	-	A
I_{GSS}	gate leakage current	$V_{GS} = 10\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 12.6\text{ A}$	-	90	-	$\text{m}\Omega$

Table 7. AC characteristics

$T_j = 25\text{ }^{\circ}\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	210	-	pF
C_{oss}	output capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	67	-	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	1.35	-	pF

Table 7. AC characteristics ...continued
 $T_j = 25\text{ }^{\circ}\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Peak device						
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	315	-	pF
C_{oss}	output capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	105	-	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	1.5	-	pF

Table 8. RF characteristics
RF characteristics in Ampleon production test circuit, $T_{case} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DVB-T (8k OFDM), Doherty operation						
V_{DS}	drain-source voltage		-	50	-	V
I_{Dq}	quiescent drain current	peak section: $V_{GS} = 1.3\text{ V}$ below $V_{GS(th)}$ (peak)	-	600	-	mA
$P_{L(AV)}$	average output power	$f = 550\text{ MHz}$	-	150	-	W
G_p	power gain	$f = 550\text{ MHz}$	15.8	17	-	dB
η_D	drain efficiency	$f = 550\text{ MHz}$	48	52	-	%
PAR	peak-to-average ratio	$f = 550\text{ MHz}$	7.2	7.8	-	dB

7. Test information

7.1 Ruggedness in Doherty operation

The BLF888E and BLF888ES are capable of withstanding a load mismatch corresponding to $VSWR \geq 40 : 1$ through all phases under the following conditions: $V_{DS} = 50\text{ V}$; $f = 550\text{ MHz}$ at rated load power.

7.2 Test circuit

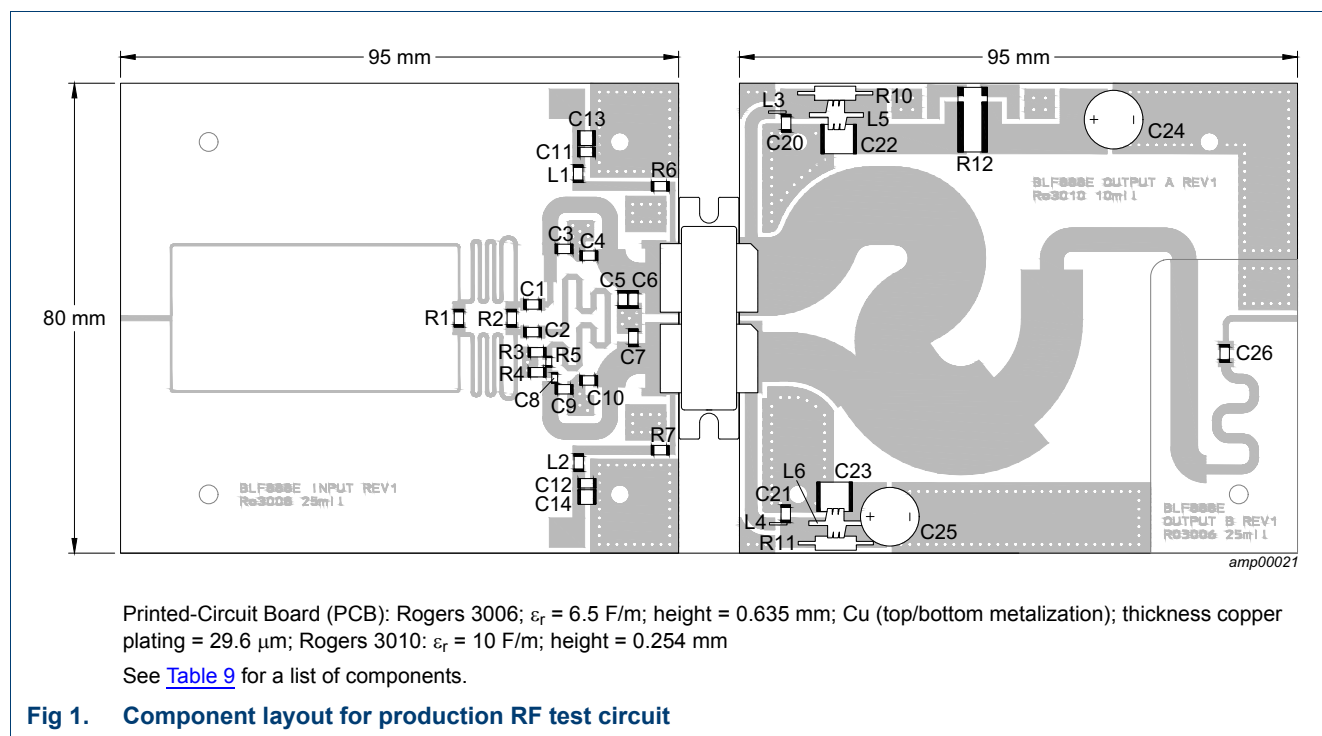


Table 9. List of components

For test circuit see [Figure 1](#).

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	51 pF	[1] ATC 100B
C3	multilayer ceramic chip capacitor	11 pF	[1] ATC 100B
C4	multilayer ceramic chip capacitor	13 pF	[1] ATC 100B
C5, C6	multilayer ceramic chip capacitor	24 pF	[1] ATC 100B
C7	multilayer ceramic chip capacitor	33 pF	[1] ATC 100B
C8	multilayer ceramic chip capacitor	51 pF	[2] ATC 100A
C9	multilayer ceramic chip capacitor	12 pF	[1] ATC 100B
C10	multilayer ceramic chip capacitor	20 pF	[1] ATC 100B
C11, C12	multilayer ceramic chip capacitor	43 pF	[1] ATC 100B
C13, C14	multilayer ceramic chip capacitor	4.7 μF	
C20, C21	electrolytic capacitor	100 pF	[1] ATC 100B
C22, C23	multilayer ceramic chip capacitor	4.7 μF , 100 V	
C25, C25	electrolytic capacitor	470 μF , 63 V	
C26	multilayer ceramic chip capacitor	47 pF	[1] ATC 100B
L1, L2	inductor	10 nH	Coilcraft
L3, L4	inductor	0.5 turn, D = 2 mm, d = 1mm	
L5, L6	inductor	1 turn, D = 5 mm, d = 1mm	
R1	chip resistor	90 Ω	

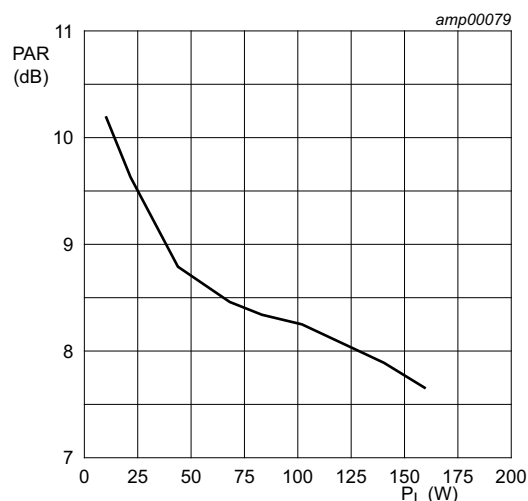
Table 9. List of components ...continued
For test circuit see [Figure 1](#).

Component	Description	Value	Remarks
R2	chip resistor	265 Ω	
R3, R4	chip resistor	360 Ω	
R5	chip resistor	15 Ω	
R6	chip resistor	75 Ω	
R7	chip resistor	5 Ω	
R10, R11	wire resistor	1 Ω	
R12	shunt resistor	0.01 Ω	

- [1] American Technical Ceramics type 100B or capacitor of same quality
[2] American Technical Ceramics type 100A or capacitor of same quality

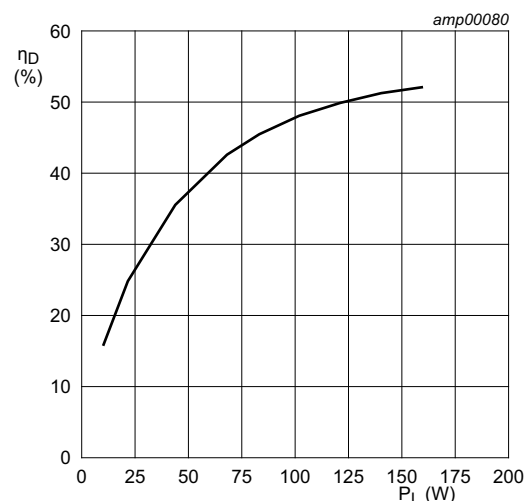
7.3 Graphical data

7.3.1 DVB-T in production test circuit



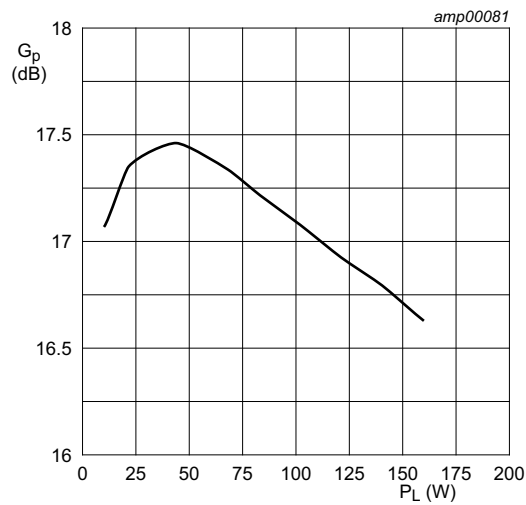
$V_{DS} = 50$ V; $I_{DQ} = 600$ mA; measured in a Doherty production test circuit at 550 MHz.

Fig 2. Peak-to-average power ratio as a function of output power; typical values



$V_{DS} = 50$ V; $I_{DQ} = 600$ mA; measured in a Doherty production test circuit at 550 MHz.

Fig 3. Drain efficiency as a function of output power; typical values



$V_{DS} = 50$ V; $I_{DQ} = 600$ mA; measured in a Doherty production test circuit at 550 MHz.

Fig 4. Power gain as a function of output power; typical values

8. Package outline

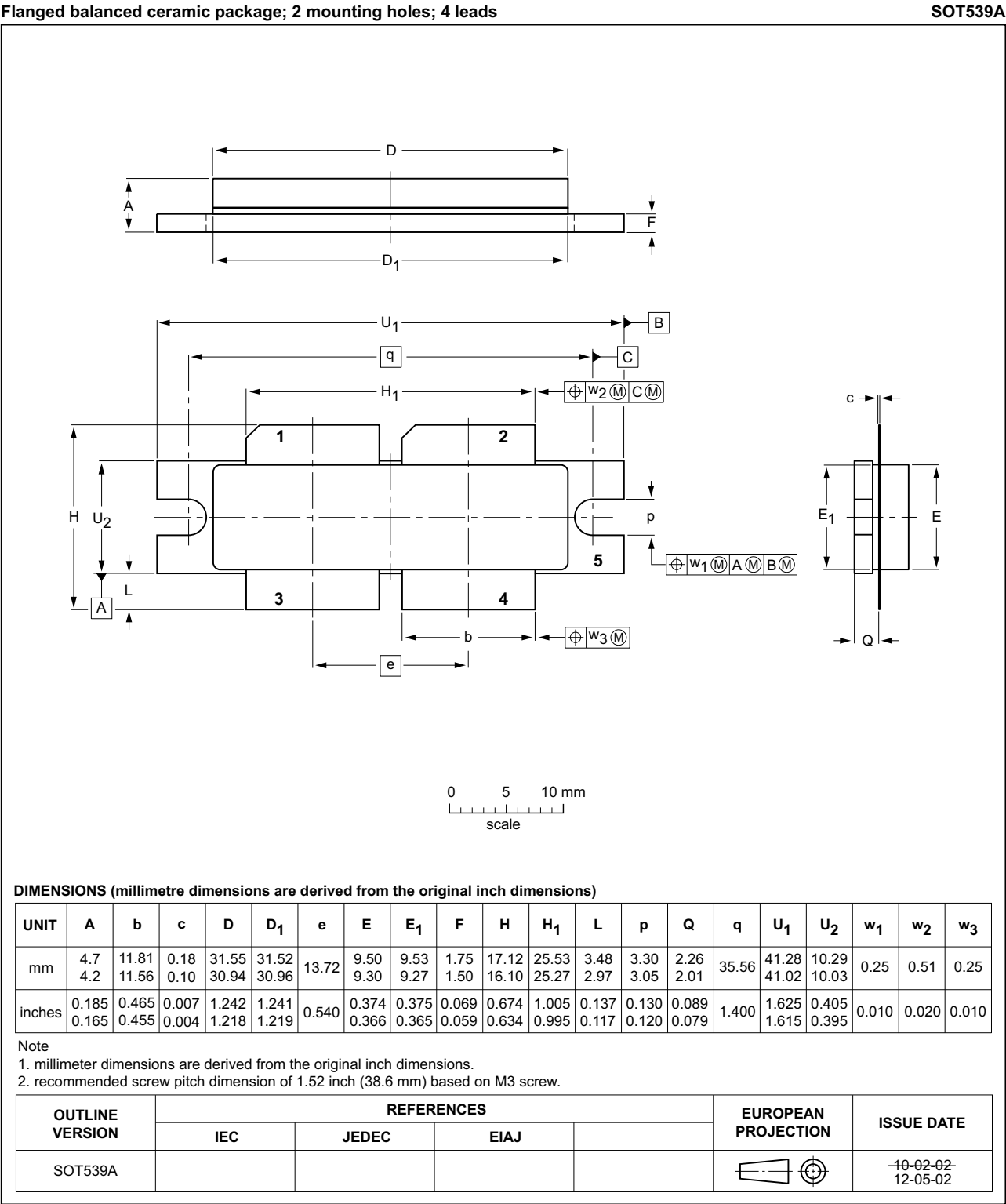
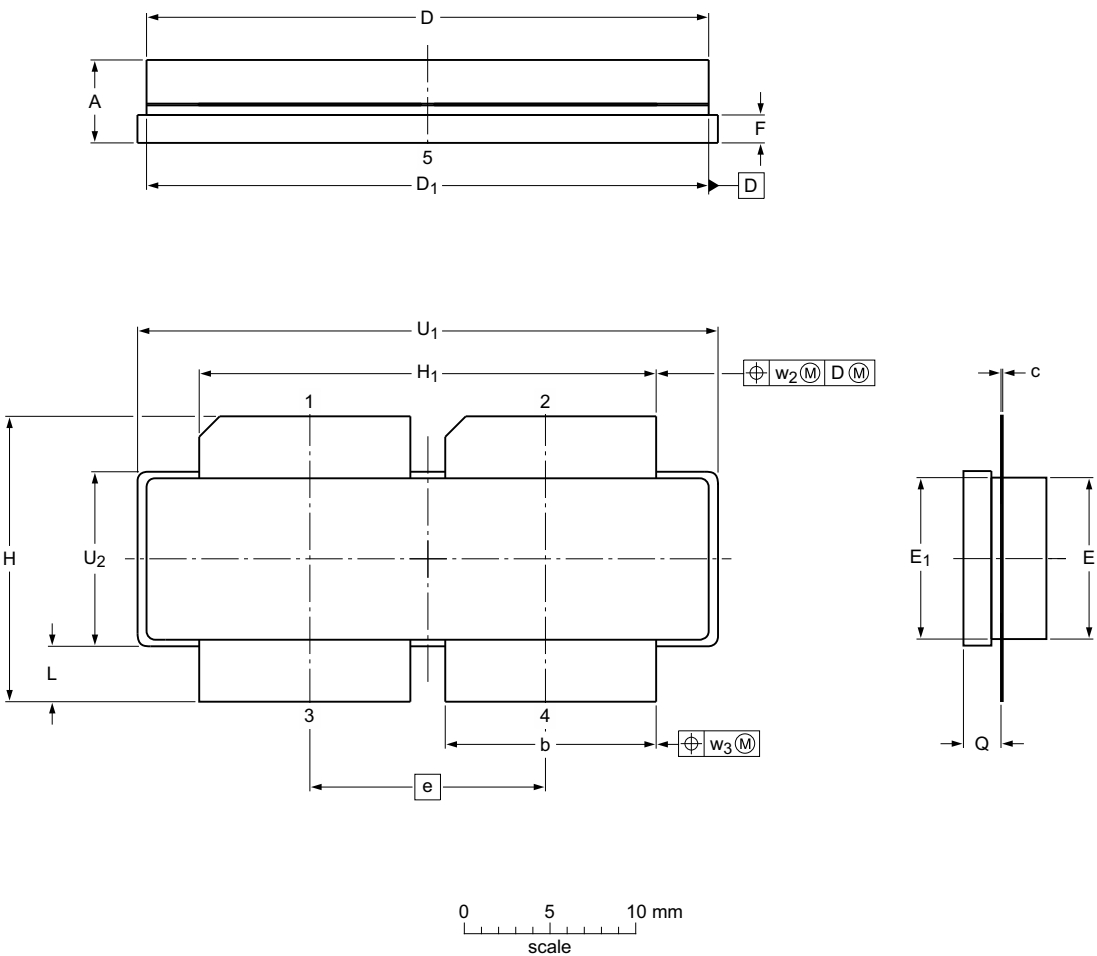


Fig 5. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads

SOT539B



Dimensions																		
Unit ⁽¹⁾		A	b	c	D	D ₁	E	E ₁	e	F	H	H ₁	L	Q	U ₁	U ₂	w ₂	w ₃
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53	13.72	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	nom min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375	0.54	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	nom min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions. sot539b_po


Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						12-05-02 13-05-24

Fig 6. Package outline SOT539B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
DVB-T	Digital Video Broadcast - Terrestrial
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OFDM	Orthogonal Frequency Division Multiplexing
PAR	Peak-to-Average Ratio
UHF	Ultra High Frequency
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF888E_BLF888ES v.2	20160830	Product data sheet	-	BLF888E_BLF888ES v.1
Modifications:	<ul style="list-style-type: none"> • Section 1.1 on page 1: section updated • Table 1 on page 1: table updated • Section 1.2 on page 1: text second list item updated • Table 5 on page 3: table updated • Table 6 on page 3: table updated • Table 8 on page 4: table updated • Section 7.1 on page 4: section updated • Section 7.3 on page 6: section added 			
BLF888E_BLF888ES v.1	20160317	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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