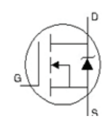
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.035	—	V/°C	Reference to 25°C, I_D = 5mA ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.0	1.4	mΩ	V_{GS} = 10V, I_D = 200A ⑤
		—	1.2	1.7		V_{GS} = 4.5V, I_D = 180A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.5	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Trans conductance	370	—	—	S	V_{DS} = 10V, I_D = 220A
R_G	Gate Resistance	—	1.9	—	Ω	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 40V, V_{GS} = 0V
		—	—	250		V_{DS} = 40V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	—	120	180	nC	I_D = 170A
Q_{gs}	Gate-to-Source Charge	—	32	—		V_{DS} = 20V
Q_{gd}	Gate-to-Drain Charge	—	71	—		V_{GS} = 4.5V⑤
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	—	49	—		
$t_{d(on)}$	Turn-On Delay Time	—	71	—	ns	V_{DD} = 26V
t_r	Rise Time	—	590	—		I_D = 220A
$t_{d(off)}$	Turn-Off Delay Time	—	94	—		R_G= 2.7Ω
t_f	Fall Time	—	200	—		V_{GS} = 4.5V⑤
C_{iss}	Input Capacitance	—	10990	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	2030	—		V_{DS} = 40V
C_{rss}	Reverse Transfer Capacitance	—	1100	—		*ƒ* = 1.0MHz
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	2520	—		V_{GS} = 0V, V_{DS} = 0V to 32V⑦
$C_{oss\ eff.(TR)}$	Effective Output Capacitance (Time Related)	—	3060	—		V_{GS} = 0V, V_{DS} = 0V to 32V⑥

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	380①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	1540		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 200A,V_{GS} = 0V ⑤
t_{rr}	Reverse Recovery Time	—	46	—	ns	T_J = 25°C V_{DD} = 34V
		—	49	—		T_J = 125°C I_F = 220A,
Q_{rr}	Reverse Recovery Charge	—	100	—	nC	T_J = 25°C di/dt = 100A/µs ⑤
		—	110	—		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	3.7	—	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
② Repetitive rating; pulse width limited by max. junction temperature.
③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.010mH, R_G = 25Ω, I_{AS} = 220A, V_{GS} =10V. Part not recommended for use above this value.
④ $I_{SD} \leq$ 220A, di/dt $\leq$ 1240A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.
⑤ Pulse width $\leq$ 400µs; duty cycle $\leq$ 2%.
⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
⑨ R_θ is measured at T_J approximately 90°C.
⑩ $R_{\theta JC}$ value shown is at time zero

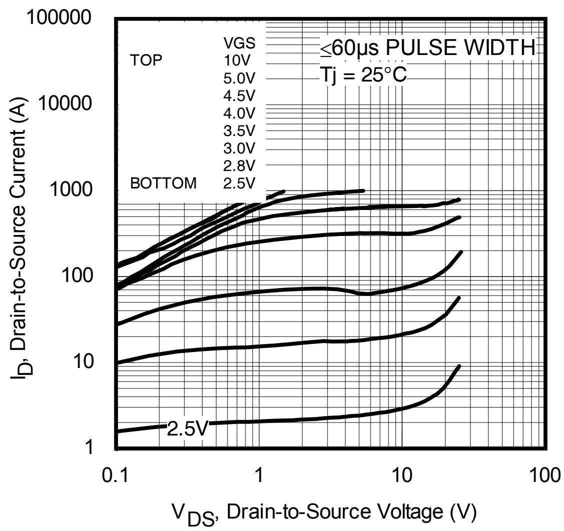


Fig. 1 Typical Output Characteristics

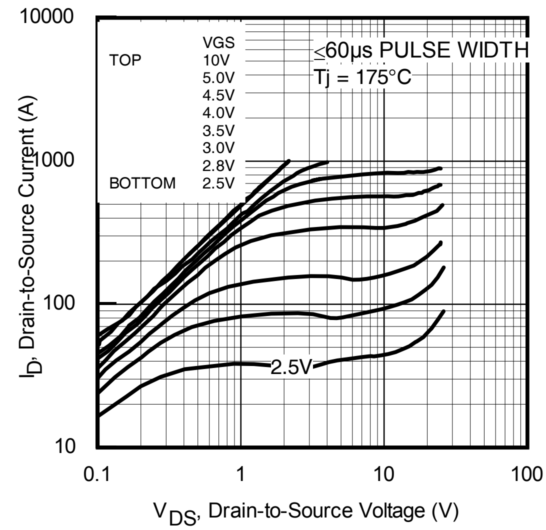


Fig. 2 Typical Output Characteristics

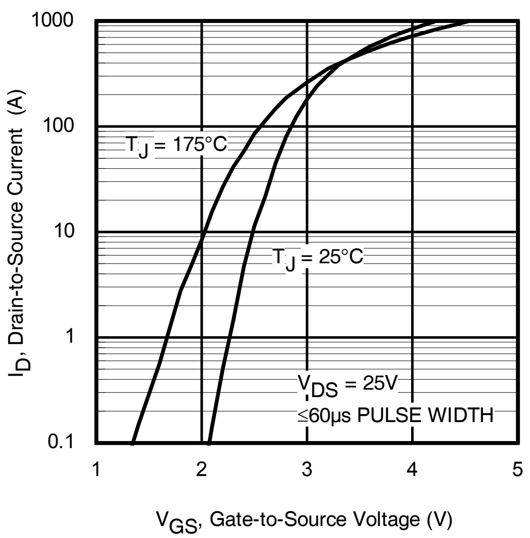


Fig. 3 Typical Transfer Characteristics

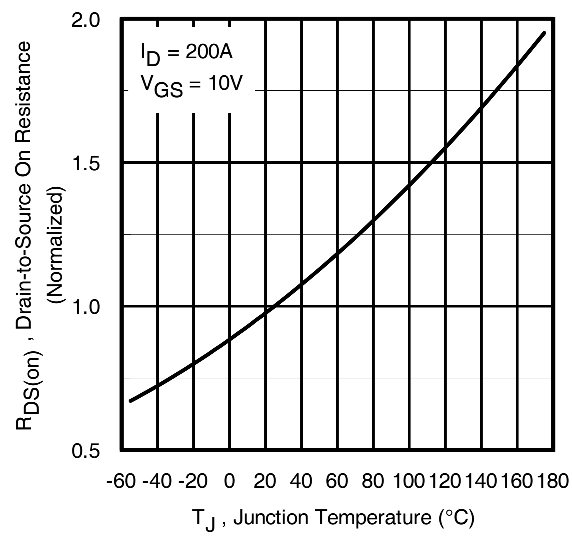


Fig. 4 Normalized On-Resistance vs. Temperature

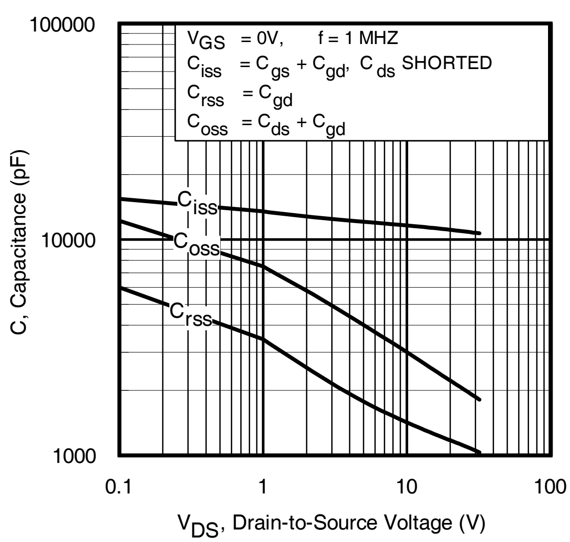


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

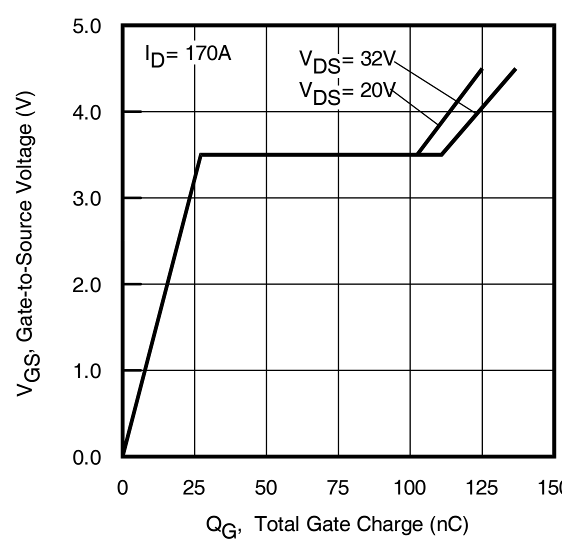


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

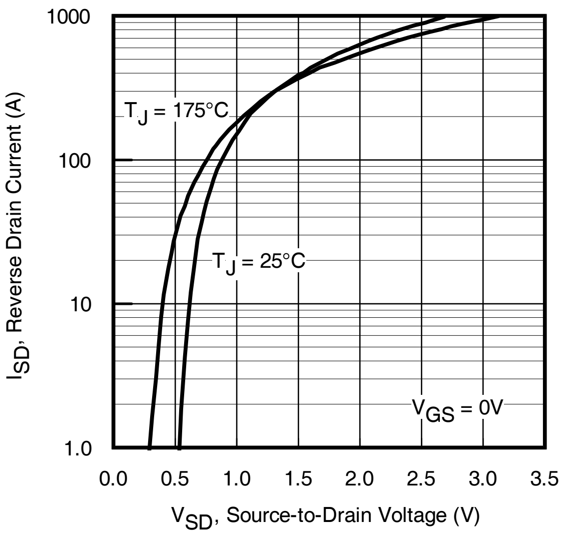


Fig. 7 Typical Source-to-Drain Diode

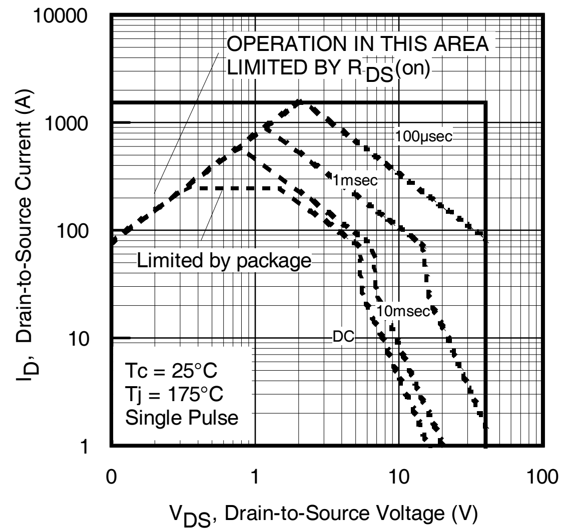


Fig 8. Maximum Safe Operating Area

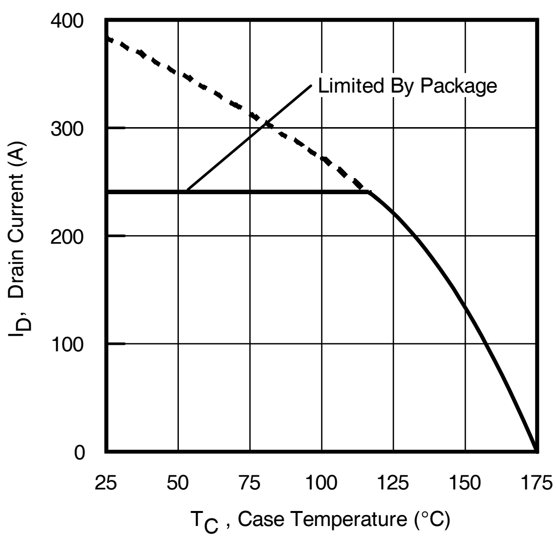


Fig 9. Maximum Drain Current vs. Case Temperature

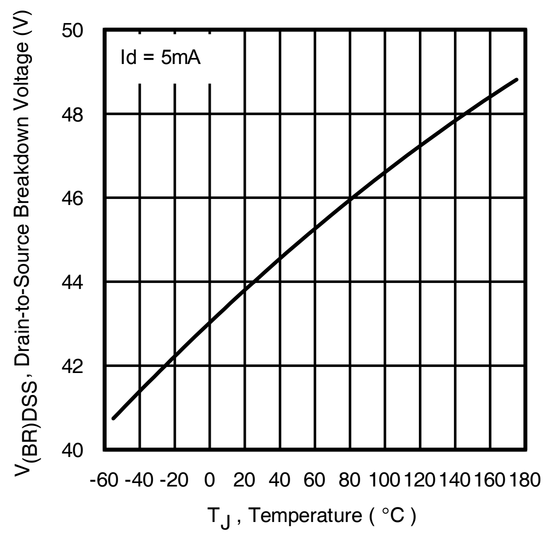


Fig 10. Drain-to-Source Breakdown Voltage

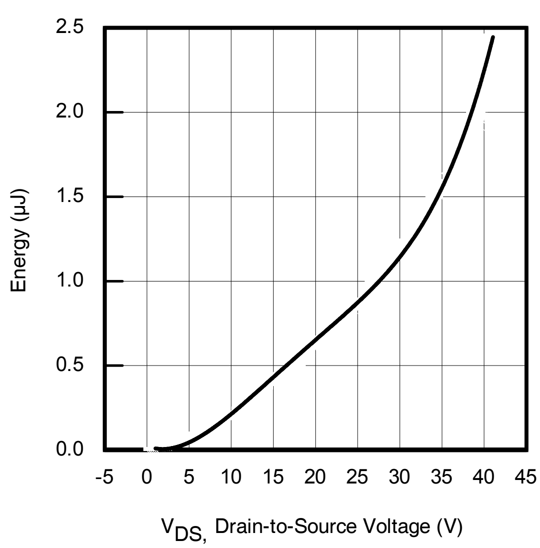


Fig 11. Typical Coss Stored Energy

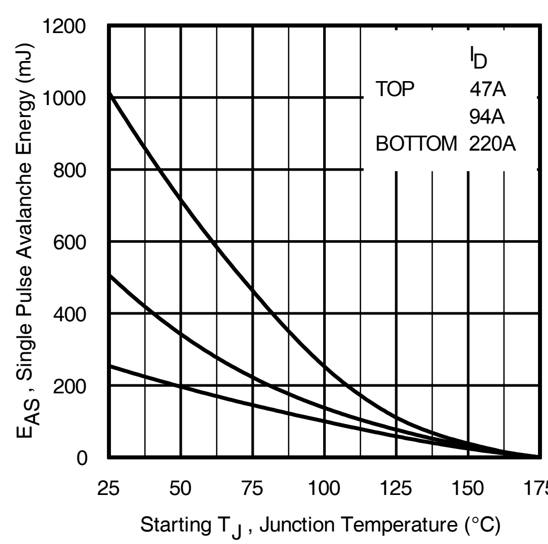
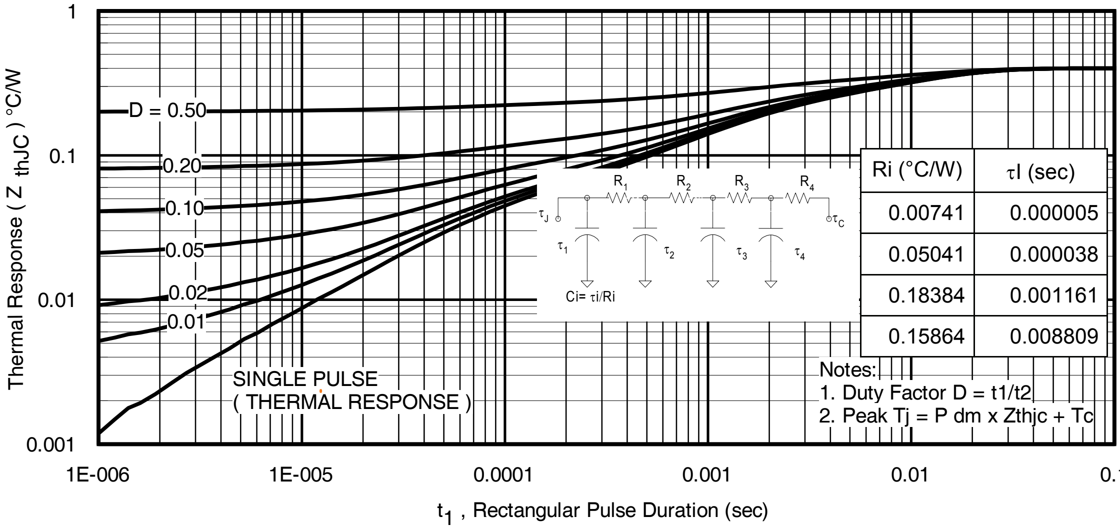


Fig 12. Maximum Avalanche Energy vs. Drain Current



Ri (°C/W)	τI (sec)
0.00741	0.000005
0.05041	0.000038
0.18384	0.001161
0.15864	0.008809

Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

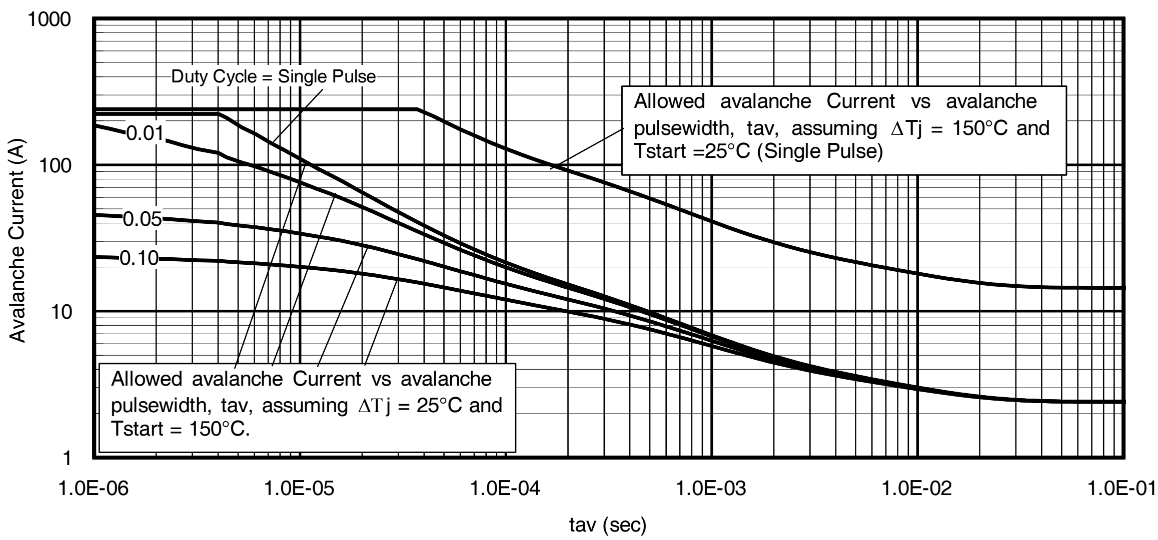


Fig 14. Avalanche Current vs. Pulse width

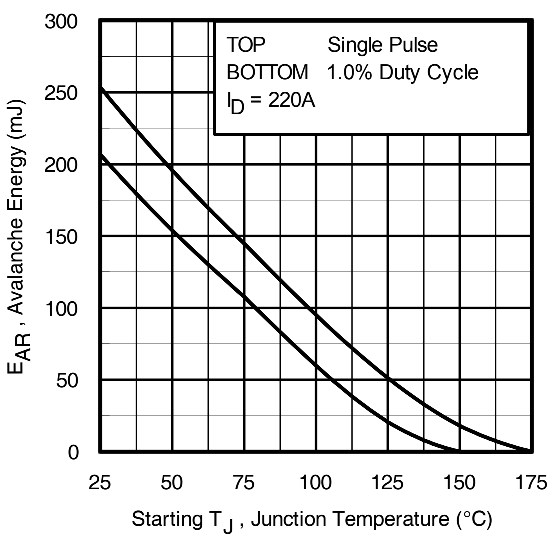


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 13, 14).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$\mathbf{P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T /\ Z_{thJC}}$$
$$\mathbf{I_{av} = 2\Delta T /\ [1.3 \cdot BV \cdot Z_{th}]}$$
$$\mathbf{E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}}$$

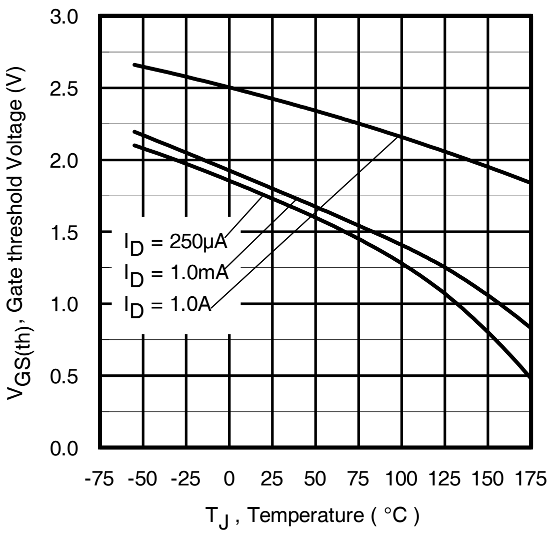


Fig 16. Threshold Voltage vs. Temperature

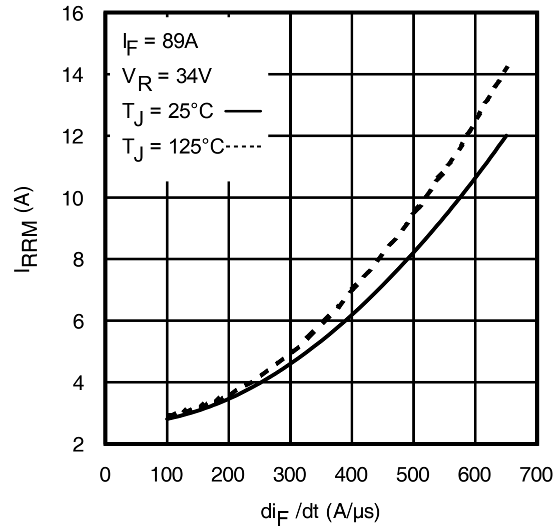


Fig. 17 - Typical Recovery Current vs. dif/dt

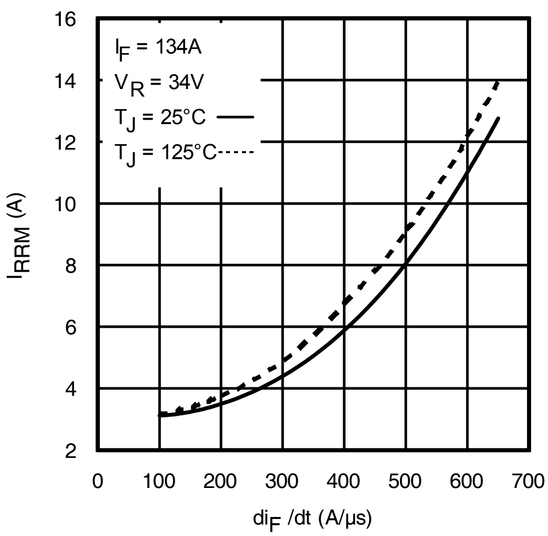


Fig. 18 - Typical Recovery Current vs. dif/dt

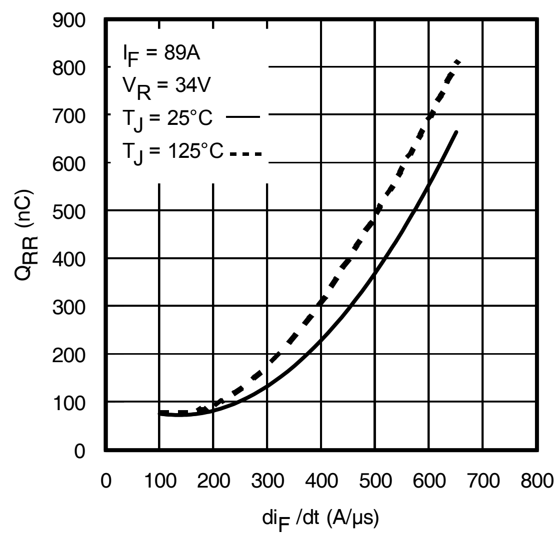


Fig. 19 - Typical Stored Charge vs. dif/dt

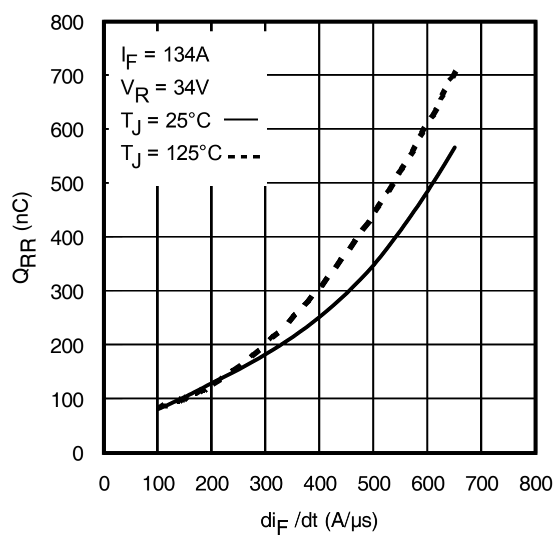


Fig. 20 - Typical Stored Charge vs. dif/dt

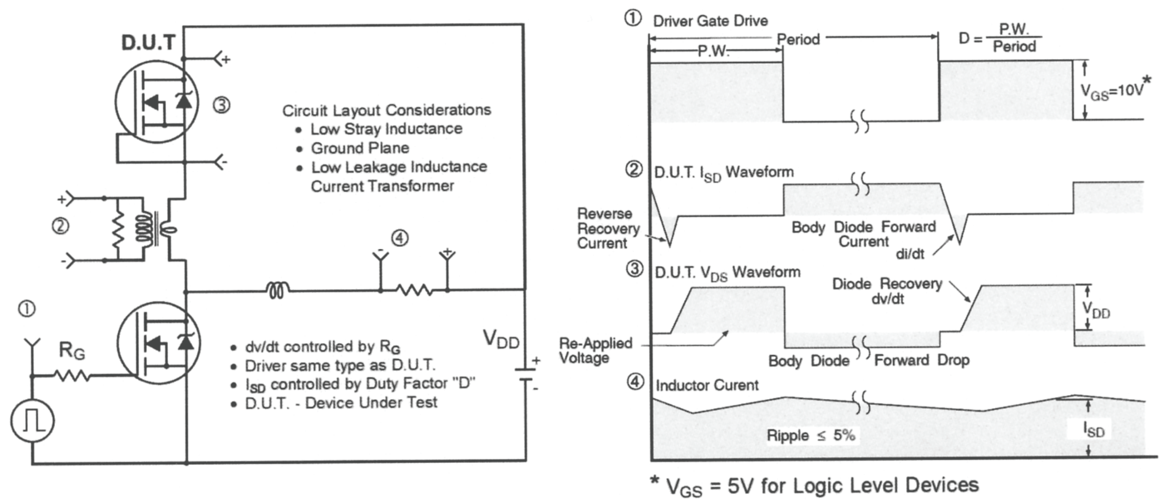


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

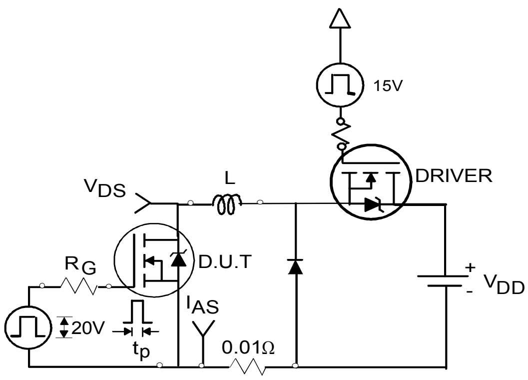


Fig 22a. Unclamped Inductive Test Circuit

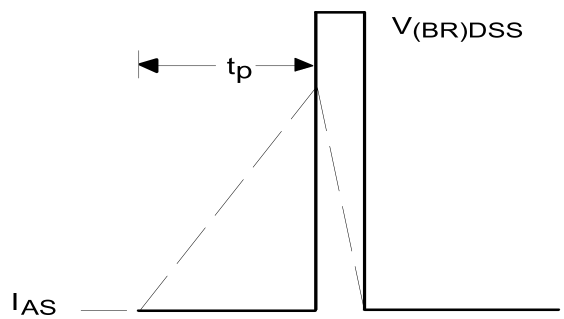


Fig 22b. Unclamped Inductive Waveforms

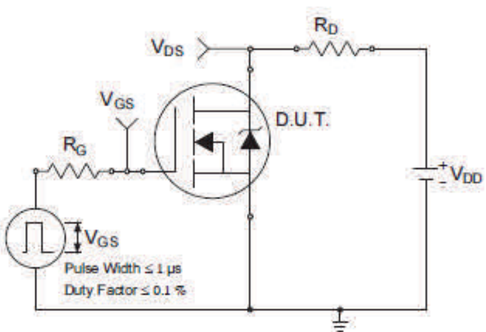


Fig 23a. Switching Time Test Circuit

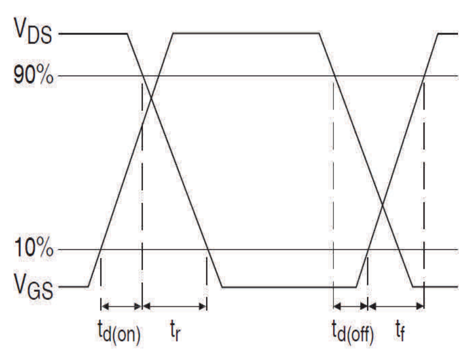


Fig 23b. Switching Time Waveforms

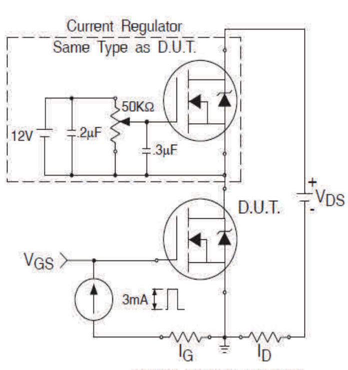


Fig 24a. Gate Charge Test Circuit

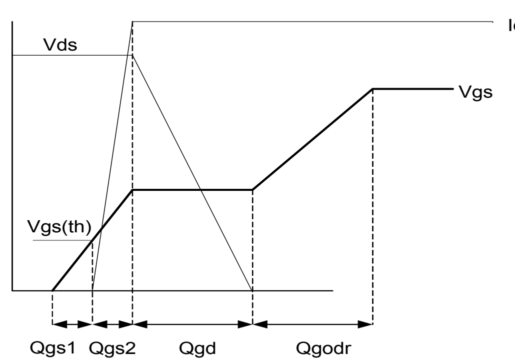
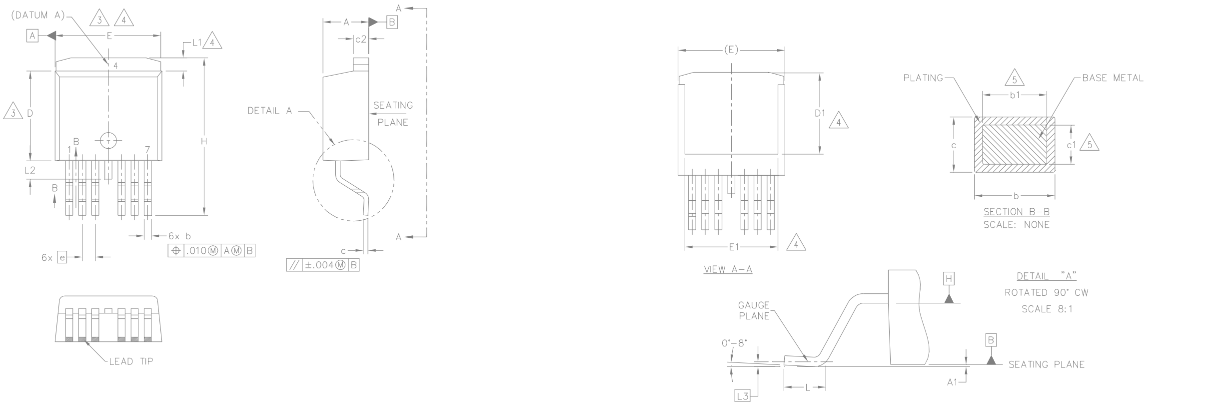


Fig 24b. Gate Charge Waveform

D²Pak - 7 Pin Package Outline (Dimensions are shown in millimeters (inches))

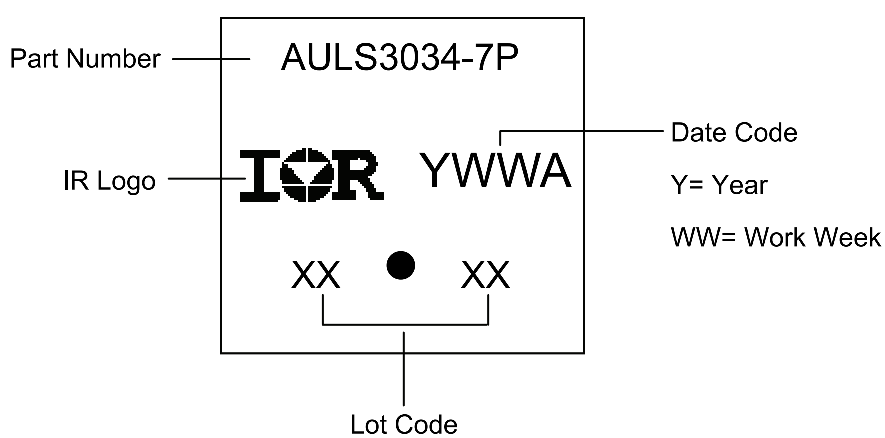


SYMBOL	DIMENSIONS MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.	NOTES
A	4.06	4.83	.160	.190	
A1	–	0.254	–	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	7.42	.270	.292	4
E	9.65	10.54	.380	.415	3,4
E1	6.22	8.48	.245	.334	4
e	1.27 BSC		.050 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO–263CB. EXCEPT FOR DIMS. E, E1 & D1.

D²Pak - 7 Pin Part Marking Information



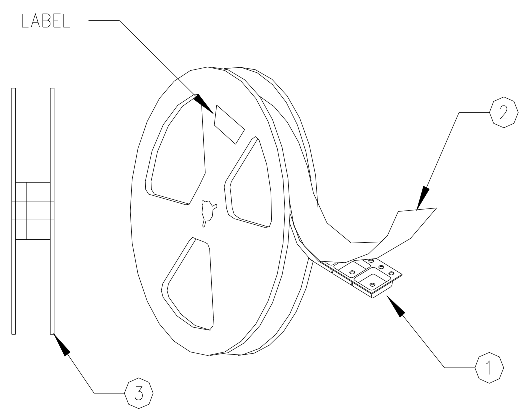
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

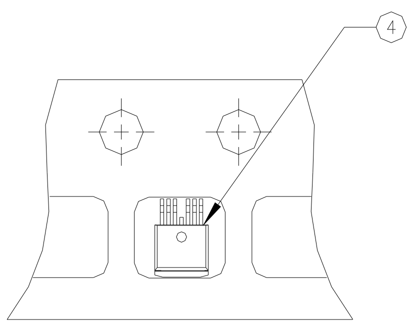
D^2Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
   - 1.1 REEL SIZE 13 INCH DIAMETER.
   - 1.2 EACH REEL CONTAINING 800 DEVICES.
   - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
   - 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
   - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
   - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

2. LABELLING (REEL AND SHIPPING BAG).
   - 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
   - 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
   - 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
   - 2.4 QUANTITY:
   - 2.5 VENDOR CODE: IR
   - 2.6 LOT CODE:
   - 2.7 DATE CODE:





Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D^2-Pak 7 Pin	MSL1
ESD	Machine Model	Class M4 (+/- 800V)† AEC-Q101-002	
	Human Body Model	Class H3A (+/- 6000V)† AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V)† AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
4/2/2014	• Added "Logic Level Gate Drive" bullet in the features section on page 1 • Updated part marking on page 8 • Updated typo on the fig.19 and fig.20, unit of y-axis from "A" to "nC" on page 6. • Updated data sheet with new IR corporate template
11/4/2015	• Updated datasheet with corporate template • Corrected ordering table on page 1.

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