Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	30	—	—	V	V_{GS} = 0V, I_D = 250µA
		P-Ch	-30	—	—		V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.032	—	V/°C	Reference to 25°C, I_D = 1mA
		P-Ch	—	-0.037	—		Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	N-Ch	—	0.038	0.045	Ω	V_{GS} = 10V, I_D = 5.8A ③
			—	0.055	0.075		V_{GS} = 4.5V, I_D = 4.9A ③
		P-Ch	—	0.070	0.090		V_{GS} = -10V, I_D = -4.3A ③
			—	0.130	0.180		V_{GS} = -4.5V, I_D = -3.7A ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	—	3.0	V	V_{DS} = V_{GS}, I_D = 250µA
		P-Ch	-1.0	—	-3.0		V_{DS} = V_{GS}, I_D = -250µA
gfs	Forward Transconductance	N-Ch	5.2	—	—	S	V_{DS} = 15V, I_D = 2.4A ③
		P-Ch	2.5	—	—		V_{DS} = -24V, I_D = -1.8A ③
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	µA	V_{DS} = 24V, V_{GS} = 0V
		P-Ch	—	—	-1.0		V_{DS} = -24V, V_{GS} = 0V
		N-Ch	—	—	25		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
		P-Ch	—	—	-25		V_{DS} = -24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage		—	—	± 100	nA	V_{GS} = ± 20V

Dynamic Electrical Characteristics @ TJ = 25°C (unless otherwise stated)

	Parameter		Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	N-Ch	—	—	25	nC	N-Channel
		P-Ch	—	—	25		I_D = 2.4A V_{DS} = 24V, V_{GS} =10V
Q_{gs}	Gate-to-Source Charge	N-Ch	—	—	2.9		
		P-Ch	—	—	2.9		P-Channel ③
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	—	7.9		I_D = -1.8A V_{DS} = -24V, V_{GS} =-10V
		P-Ch	—	—	9.0		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	6.8	—	ns	N-Channel
		P-Ch	—	11	—		V_{DD} = 15V, ID=2.4A, RG = 6.0Ω
t_r	Rise Time	N-Ch	—	21	—		R_D = 6.2Ω
		P-Ch	—	17	—		P-Channel ③
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	22	—		V_{DD} = -15V, ID=-1.8A, RG = 6.0Ω
		P-Ch	—	25	—		R_D = 8.2Ω
t_f	Fall Time	N-Ch	—	7.7	—		
		P-Ch	—	18	—		
L_D	Internal Drain Inductance	N-P	—	4.0	—	nH	Between lead, 6mm (0.25in.) from package
L_S	Internal Source Inductance	N-P	—	6.0	—		and center of die contact
C_{iss}	Input Capacitance	N-Ch	—	520	—	pF	N-Channel
		P-Ch	—	440			VGS = 0V, V_{DS} = 25V, f =1.0Mhz
C_{oss}	Output Capacitance	N-Ch	—	180	—		
		P-Ch	—	200			P-Channel
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	72	—		VGS = 0V, V_{DS} = -25V, f =1.0Mhz
		P-Ch	—	93			

Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current	N-Ch	—	—	3.1	A	
	(Body Diode)	P-Ch	—	—	-3.1		
I_{SM}	Pulsed Source Current	N-Ch	—	—	46		
	(Body Diode) ①	P-Ch	—	—	-34		
V_{SD}	Diode Forward Voltage	N-Ch	—		1.0	V	T_J = 25°C, I_S = 1.8A, V_{GS} = 0V ③
		P-Ch	—		-1.0		T_J = 25°C, I_S = -1.8A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	N-Ch	—	47	71	ns	N-Channel
		P-Ch	—	53	80		T_J = 25°C, I_F = 2.4A di/dt = 100A/µs
Q_{rr}	Reverse Recovery Charge	N-Ch	—	56	84	nC	P-Channel ③
		P-Ch	—	66	99		T_J = 25°C, I_F = -1.8A di/dt = 100A/µs

Notes ① through ④ are on page 10

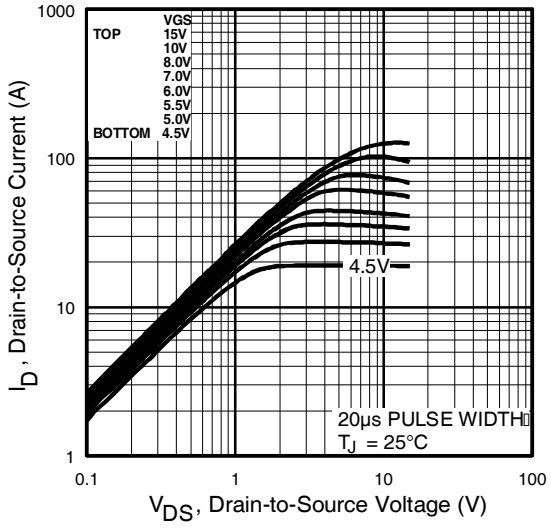


Fig 1. Typical Output Characteristics

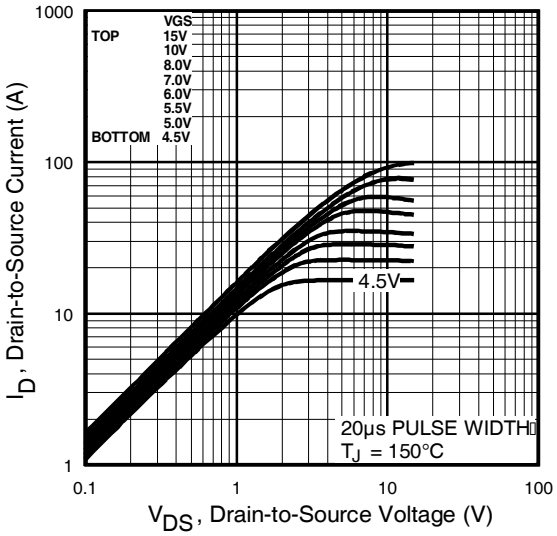


Fig 2. Typical Output Characteristics

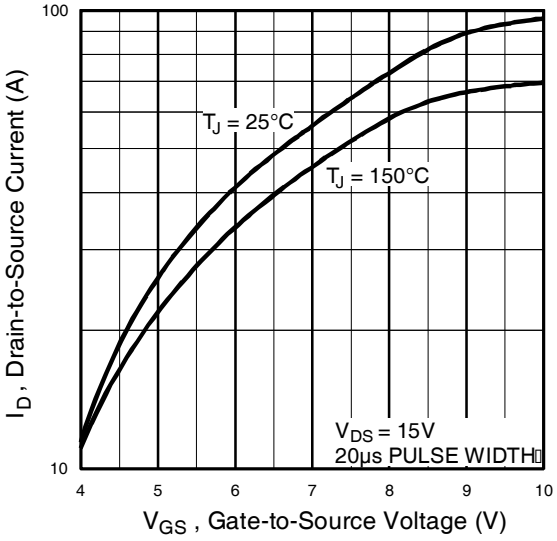


Fig 3. Typical Transfer Characteristics

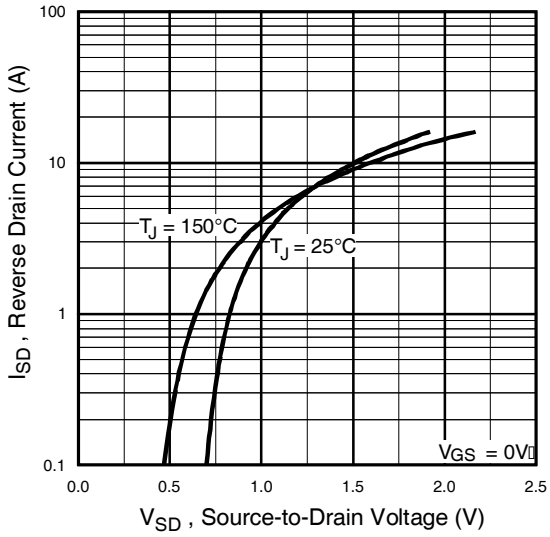


Fig 4. Typical Source-Drain Diode Forward Voltage

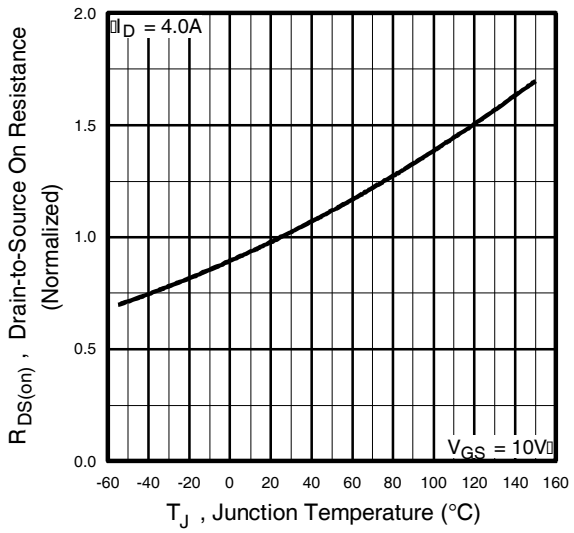


Fig 5. Normalized On-Resistance Vs. Temperature

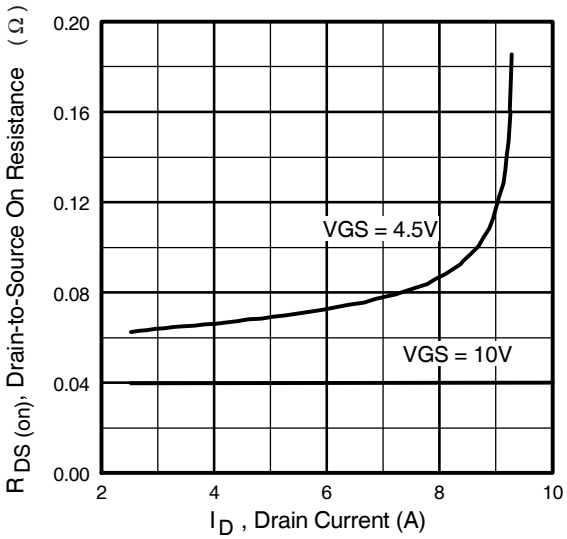


Fig 6. Typical On-Resistance Vs. Drain Current

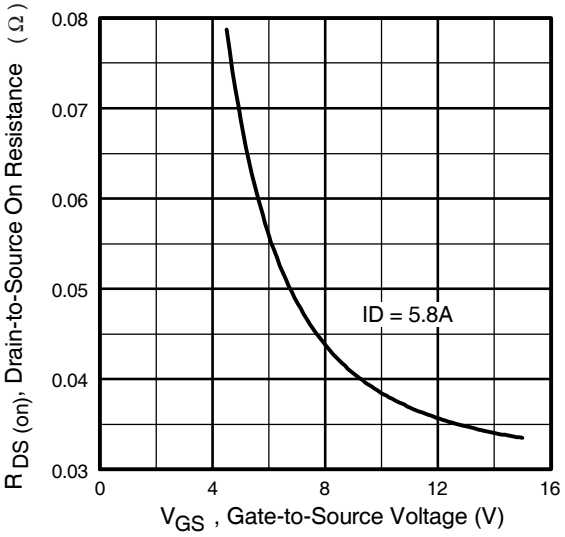


Fig 7. Typical On-Resistance Vs. Gate Voltage

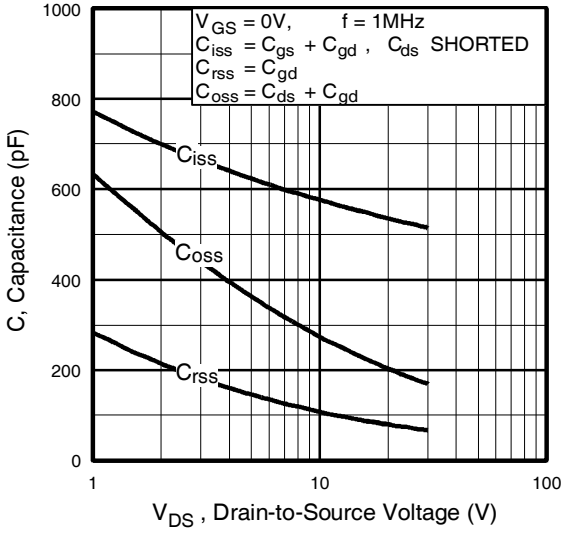


Fig 8. Typical Capacitance Vs. Drain-to-Source Voltage

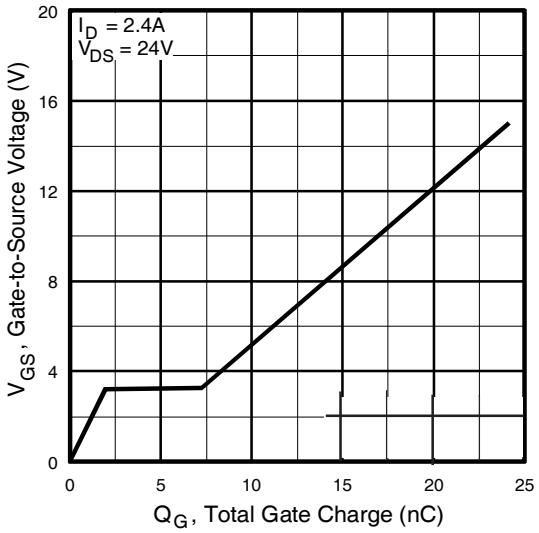


Fig 9. Typical Gate Charge Vs. Gate-to-Source Voltage

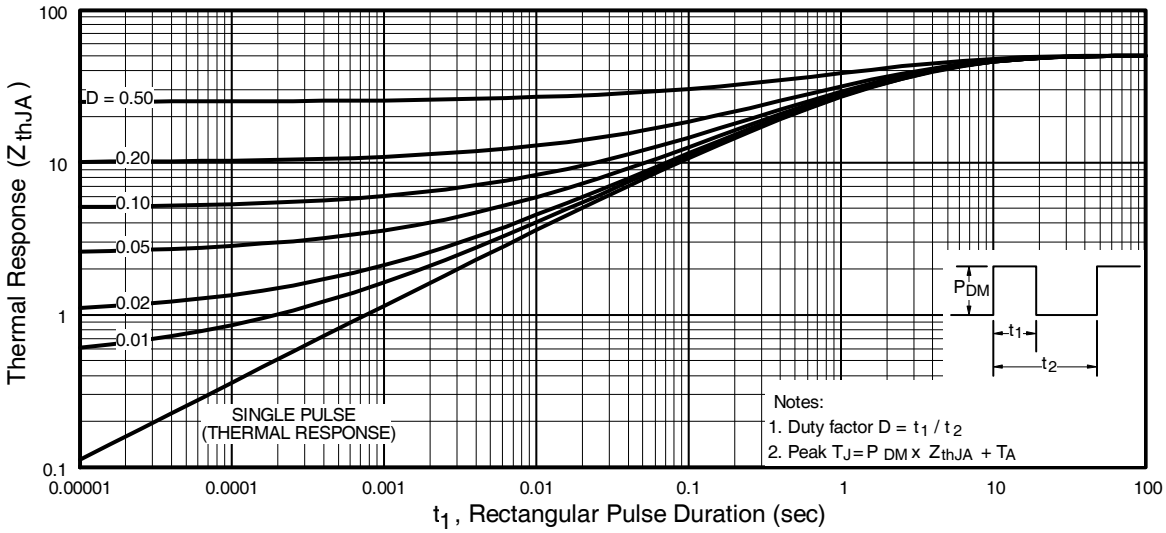


Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

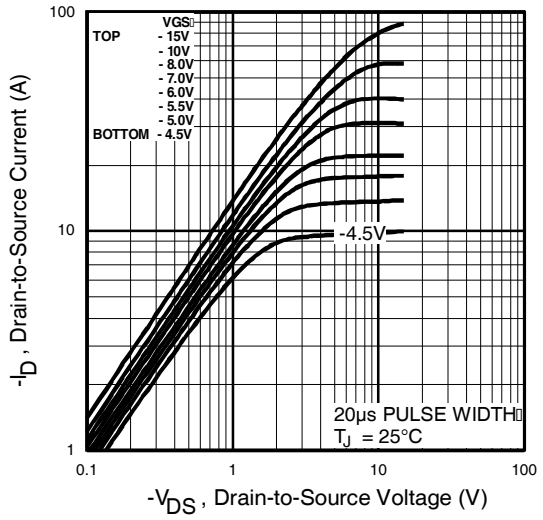


Fig 11. Typical Output Characteristics

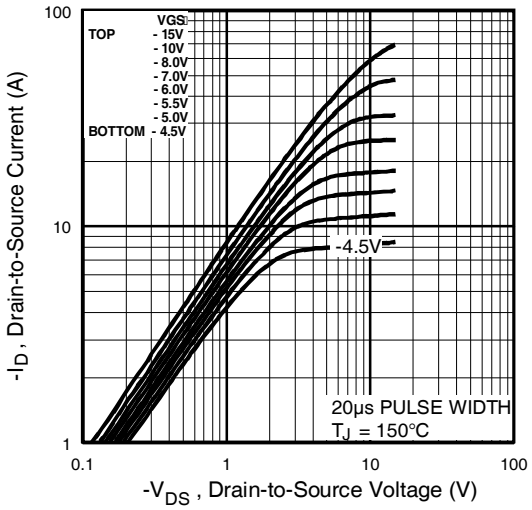


Fig 12. Typical Output Characteristics

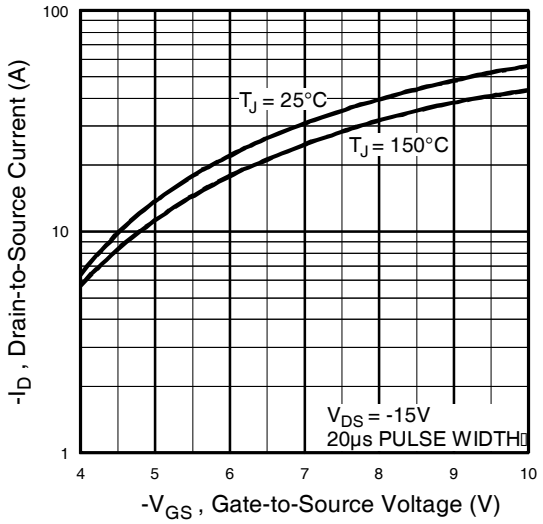


Fig 13. Typical Transfer Characteristics

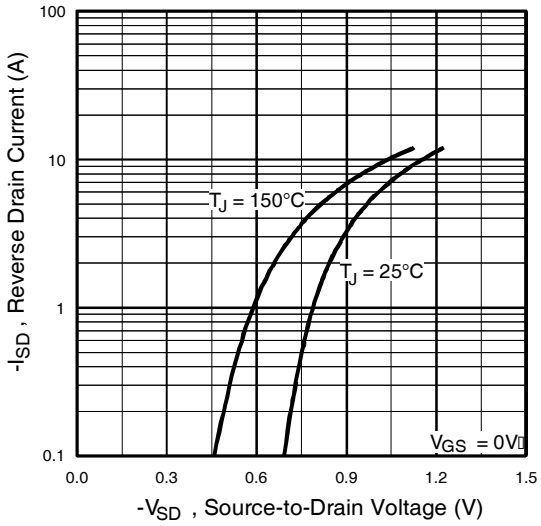


Fig 14. Typical Source-Drain Diode Forward Voltage

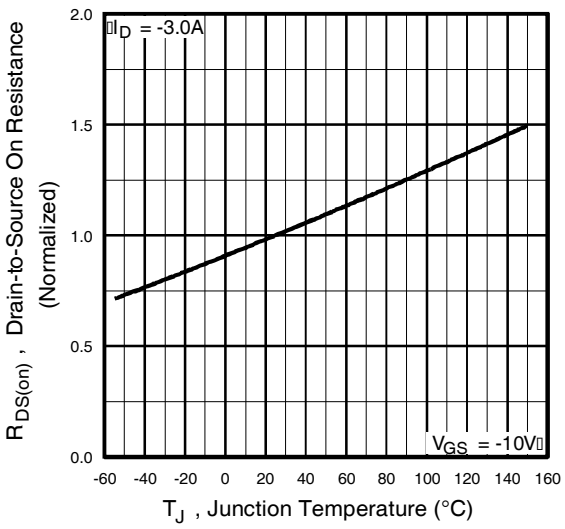


Fig 15. Normalized On-Resistance Vs. Temperature

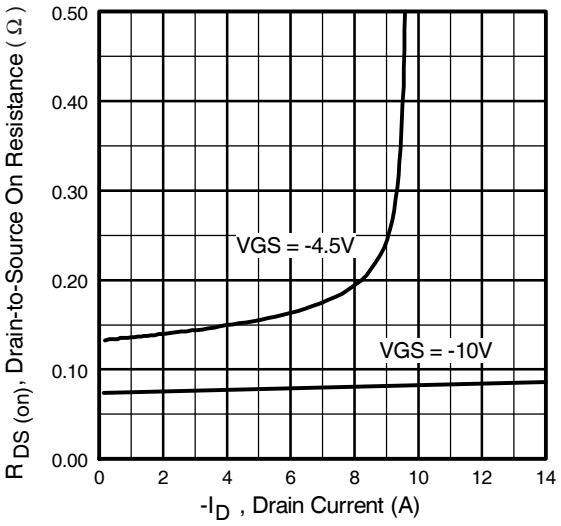


Fig 16. Typical On-Resistance Vs. Drain Current

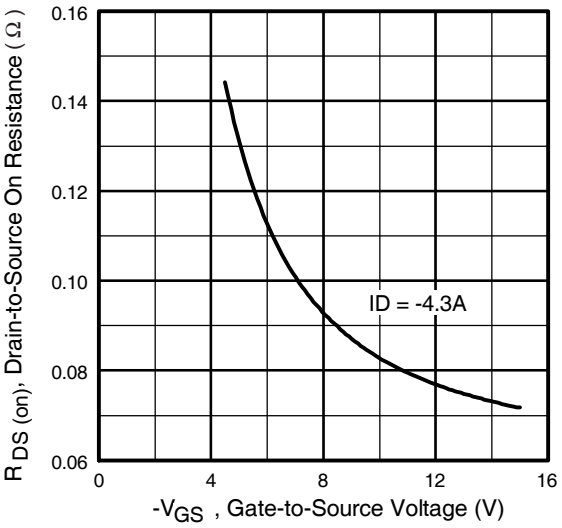


Fig 17. Typical On-Resistance Vs. Gate Voltage

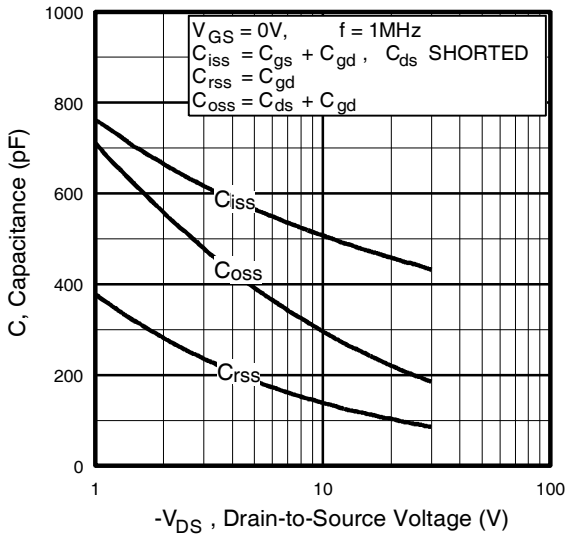


Fig 18. Typical Capacitance Vs. Drain-to-Source Voltage

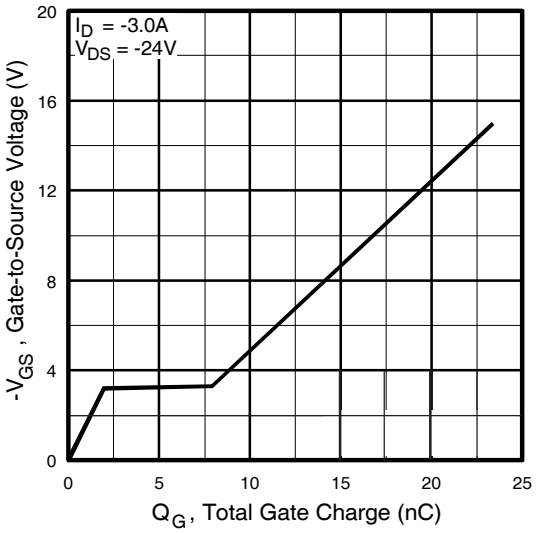


Fig 19. Typical Gate Charge Vs. Gate-to-Source Voltage

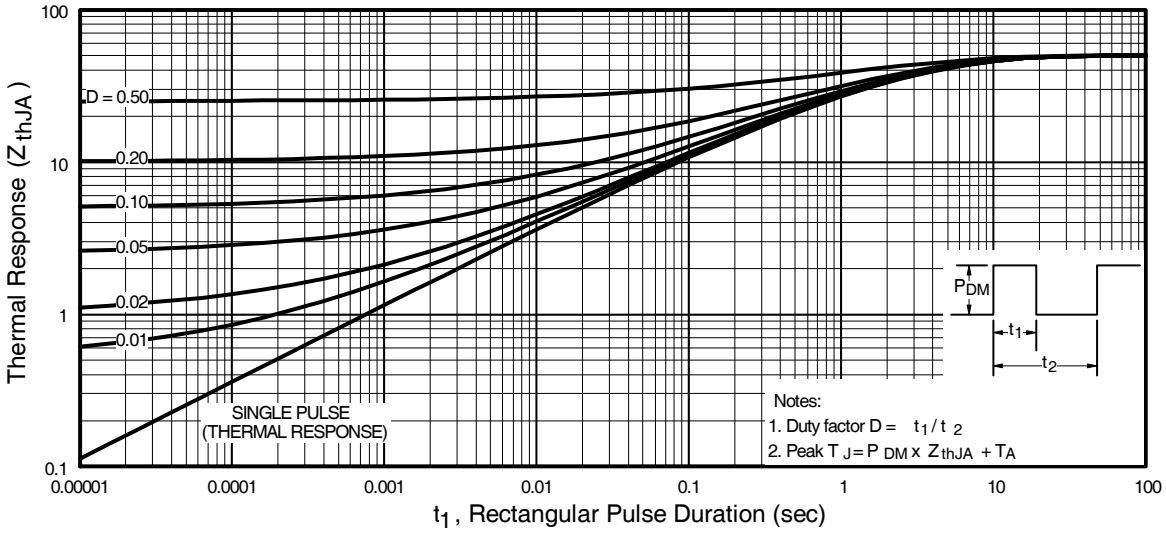
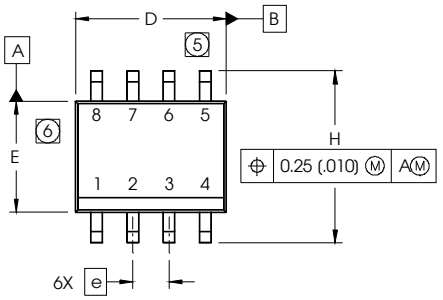


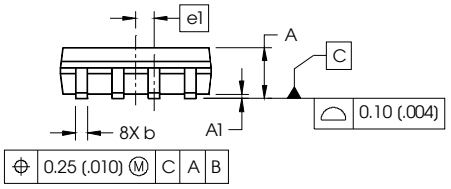
Fig 20. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

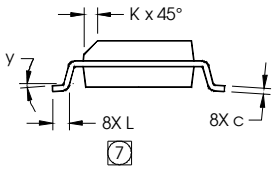
SO-8 Package Outline

Dimensions are shown in millimeters (inches)



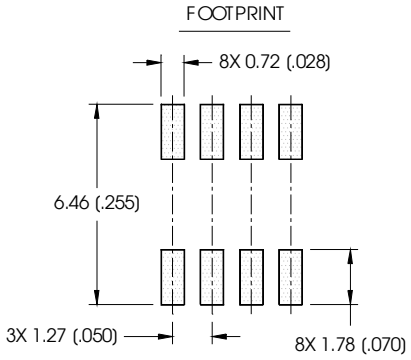
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



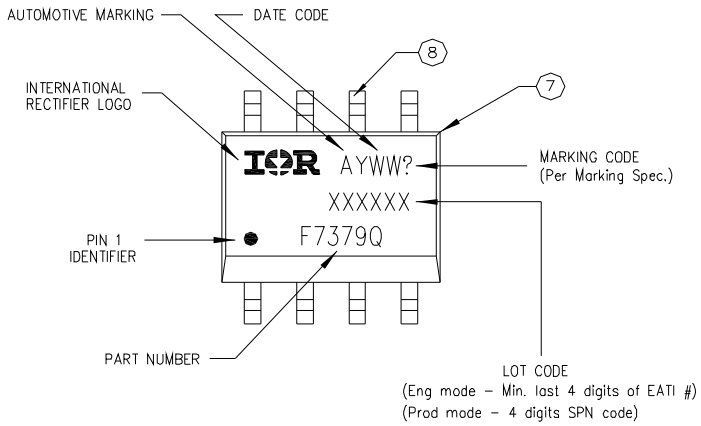


NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



SO-8 Part Marking

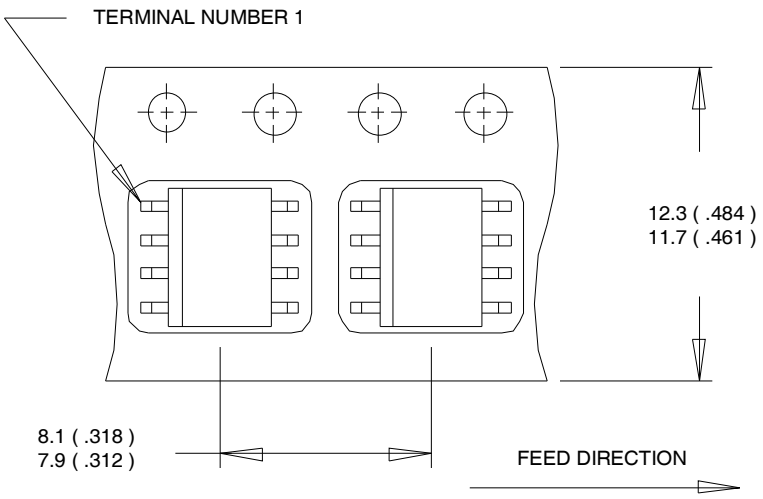


TOP MARKING (LASER)

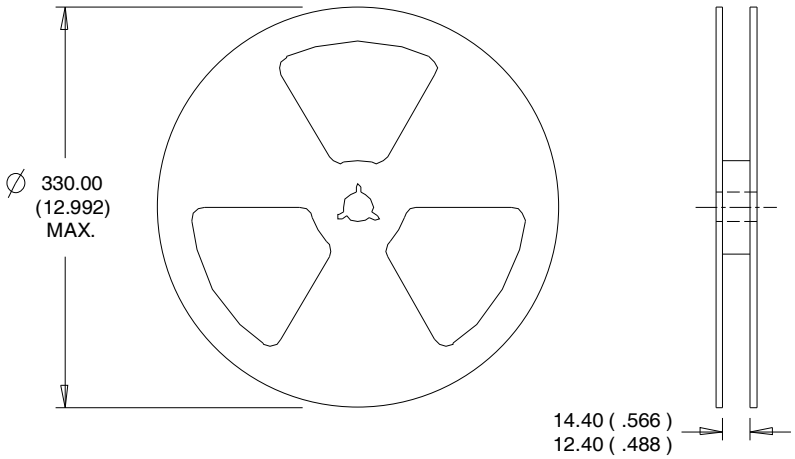
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② N-Channel $I_{SD} \leq 2.4A$, $di/dt \leq 73A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150°C$
P-Channel $I_{SD} \leq -1.8A$, $di/dt \leq 90A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150°C$
③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
④ Surface mounted on FR-4 board, $t \leq 10sec$.

Qualification Information†

Qualification Level		Automotive (per AEC-Q101) ††	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SO-8	MSL1
ESD	Machine Model	N Ch: Class M2(+/- 150V)††† (per AEC-Q101-002)	P Ch: Class M2(+/- 150V)†††
	Human Body Model	N Ch : Class H1A(+/- 500V)††† (per AEC-Q101-001)	P Ch: Class H0(+/- 250V)†††
	Charged Device Model	N Ch: Class C5(+/- 2000V)††† (per AEC-Q101-005)	P Ch: Class C5(+/- 2000V)†††
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site: http//www.irf.com/

†† Exceptions (if any) to AEC-Q101 requirements are noted in the qualification report.

††† Highest passing voltage

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For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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101 N. Sepulveda Blvd., El Segundo, California 90245
Tel: (310) 252-7105

Revision History

Date	Comments
3/10/2014	• Added "Logic Level Gate Drive" bullet in the features section on page 1 • Updated data sheet with new IR corporate template