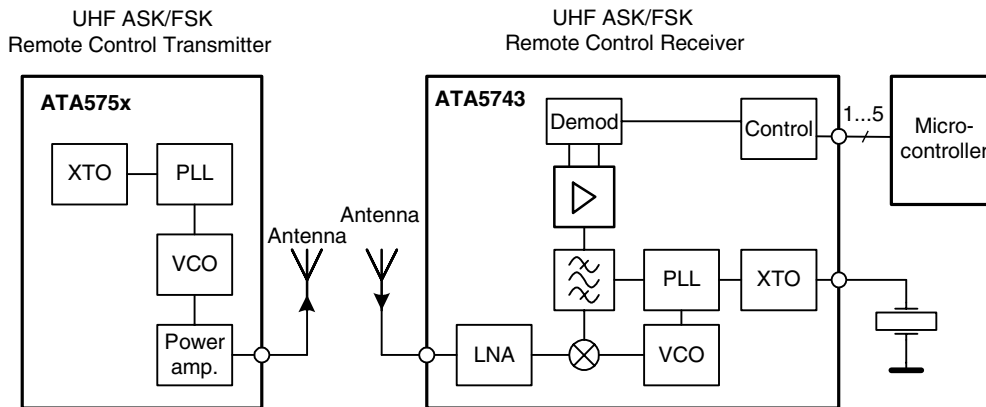


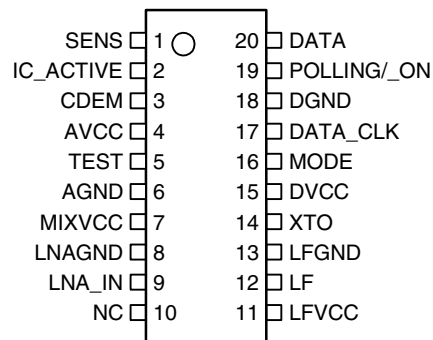
## 2. System Block Diagram

Figure 2-1. System Block Diagram



## 3. Pin Configuration

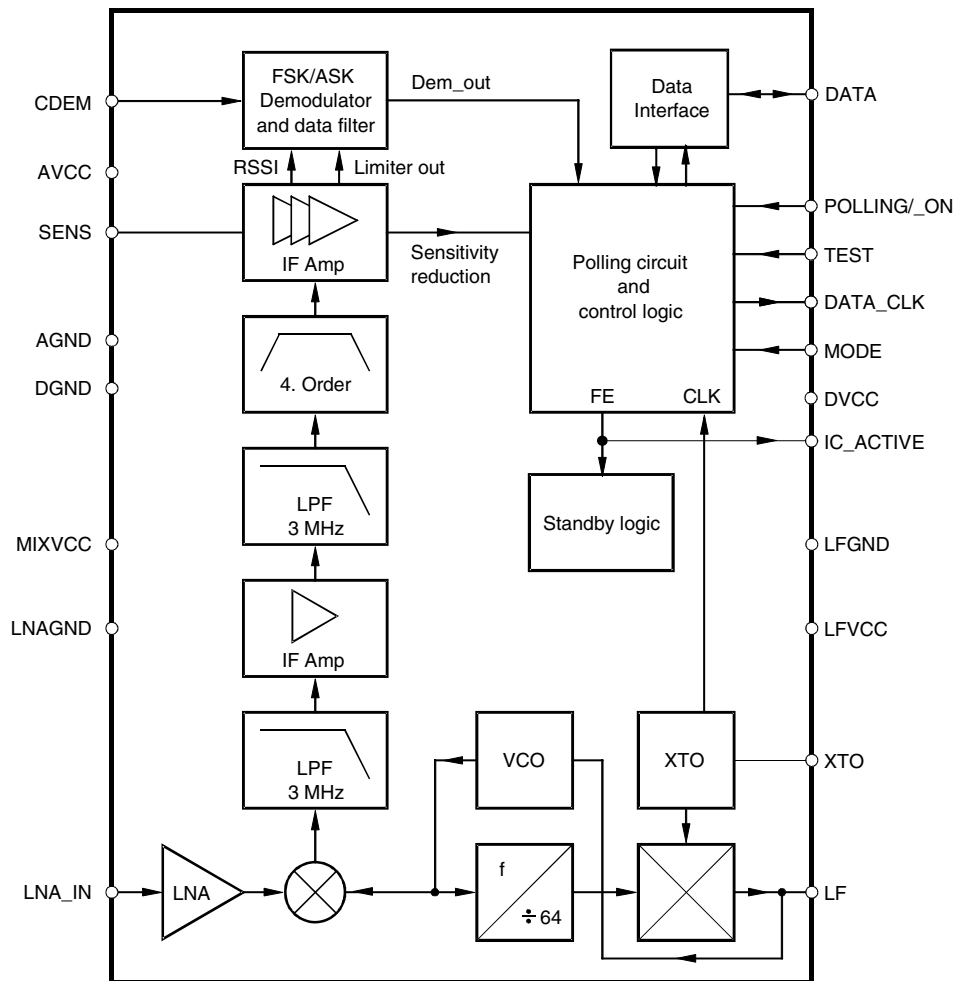
Figure 3-1. Pinning SSO20



**Table 3-1.** Pin Description

Pin	Symbol	Function
1	SENS	Sensitivity-control resistor
2	IC_ACTIVE	IC condition indicator Low = sleep mode High = active mode
3	CDEM	Lower cut-off frequency data filter
4	AVCC	Analog power supply
5	TEST	Test pin, during operation at GND
6	AGND	Analog ground
7	MIXVCC	Power supply mixer
8	LNAGND	High-frequency ground LNA and mixer
9	LNA_IN	RF input
10	NC	Not connected
11	LFVCC	Power supply VCO
12	LF	Loop filter
13	LFGND	Ground VCO
14	XTO	Crystal oscillator
15	DVCC	Digital power supply
16	MODE	Selecting 433.92 MHz/315 MHz Low: $f_{XT0} = 4.90625$ MHz (USA) High: $f_{XT0} = 6.76438$ MHz (Europe)
17	DATA_CLK	Bit clock of data stream
18	DGND	Digital ground
19	POLLING/_ON	Selects polling or receiving mode Low: receiving mode High: polling mode
20	DATA	Data output/configuration input

**Figure 3-2.** Block Diagram



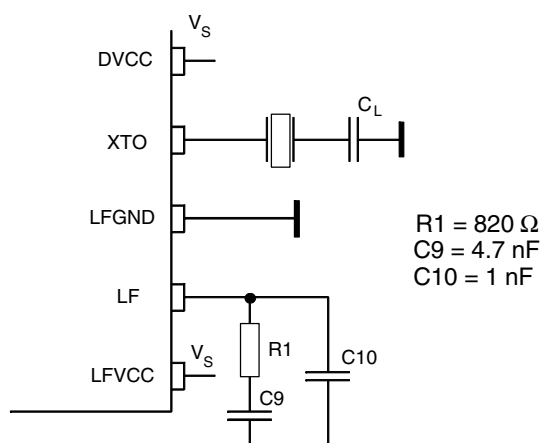
## 4. RF Front-end

The RF front-end of the receiver is a heterodyne configuration that converts the input signal into a 1 MHz IF signal. As seen in [Figure 3-2 on page 4](#), the front-end consists of an LNA (Low-Noise Amplifier), an LO (Local Oscillator), a mixer, and an RF amplifier.

The LO generates the carrier frequency for the mixer via a PLL synthesizer. The XTO (crystal oscillator) generates the reference frequency  $f_{XTO}$ . The VCO (voltage-controlled oscillator) generates the drive voltage frequency  $f_{LO}$  for the mixer.  $f_{LO}$  is dependent on the voltage at pin LF, and is then divided by 64. The divided frequency is compared to  $f_{XTO}$  by the phase frequency detector. The current output of the phase frequency detector is connected to a passive loop filter and thereby generates the control voltage  $V_{LF}$  for the VCO. By means of that configuration,  $V_{LF}$  is controlled in a way that  $f_{LO}/64$  is equal to  $f_{XTO}$ . If  $f_{LO}$  is determined,  $f_{XTO}$  can be calculated using the following formula:  $f_{XTO} = f_{LO}/64$ .

The XTO is a one-pin oscillator that operates at the series resonance of the quartz crystal. As demonstrated in [Figure 4-1](#), the crystal should be connected to GND via a capacitor  $C_L$ . The value of that capacitor is recommended by the crystal supplier. The value of  $C_L$  should be optimized for the individual board layout to achieve the exact value of  $f_{XTO}$  and hereby of  $f_{LO}$ . When designing the system in terms of receiving bandwidth, the accuracy of the crystal and the XTO must be considered.

**Figure 4-1.** PLL Peripherals



The passive loop filter connected to pin LF is designed for a loop bandwidth of  $B_{Loop} = 100\ \text{kHz}$ . This value for  $B_{Loop}$  exhibits the best possible noise performance of the LO. [Figure 4-1](#) shows the appropriate loop filter components to achieve the desired loop bandwidth. If the filter components are changed for any reason, please note that the maximum capacitive load at pin LF is limited. If the capacitive load is exceeded, a bit check may no longer be possible since  $f_{LO}$  cannot settle in time before the bit check starts to evaluate the incoming data stream. Self polling will also not work in that case.

$f_{LO}$  is determined by the RF input frequency  $f_{RF}$  and the IF frequency  $f_{IF}$  using the following formula:  $f_{LO} = f_{RF} - f_{IF}$

To determine  $f_{LO}$ , the construction of the IF filter must be considered at this point. The nominal IF frequency is  $f_{IF} = 1\ \text{MHz}$ . To achieve a good accuracy of the filter's corner frequencies, the filter is tuned by the crystal frequency  $f_{XTO}$ . This means that there is a fixed relation between  $f_{IF}$  and  $f_{LO}$ . This relation is dependent on the logic level at pin MODE.

This is described by the following formulas:

$$\text{MODE} = 0 \text{ (USA)} : f_{\text{IF}} = \frac{f_{\text{LO}}}{314}$$

$$\text{MODE} = 1 \text{ (Europe)} : f_{\text{IF}} = \frac{f_{\text{LO}}}{432.92}$$

The relation is designed to achieve the nominal IF frequency of  $f_{\text{IF}} = 1 \text{ MHz}$  for most applications. For applications where  $f_{\text{RF}} = 315 \text{ MHz}$ , MODE must be set to “0”. In the case of  $f_{\text{RF}} = 433.92 \text{ MHz}$ , MODE must be set to “1”. For other RF frequencies,  $f_{\text{IF}}$  is not equal to 1 MHz.  $f_{\text{IF}}$  is then dependent on the logical level at pin MODE and on  $f_{\text{RF}}$ . [Table 4-1](#) summarizes the different conditions.

The RF input either from an antenna or from a generator must be transformed to the RF input pin LNA\_IN. The input impedance of that pin is provided in the electrical parameters. The parasitic board inductances and capacitances also influence the input matching. The RF receiver ATA5743 exhibits its highest sensitivity at the best signal-to-noise ratio (SNR) in the LNA. Hence, noise matching is the best choice for designing the transformation network.

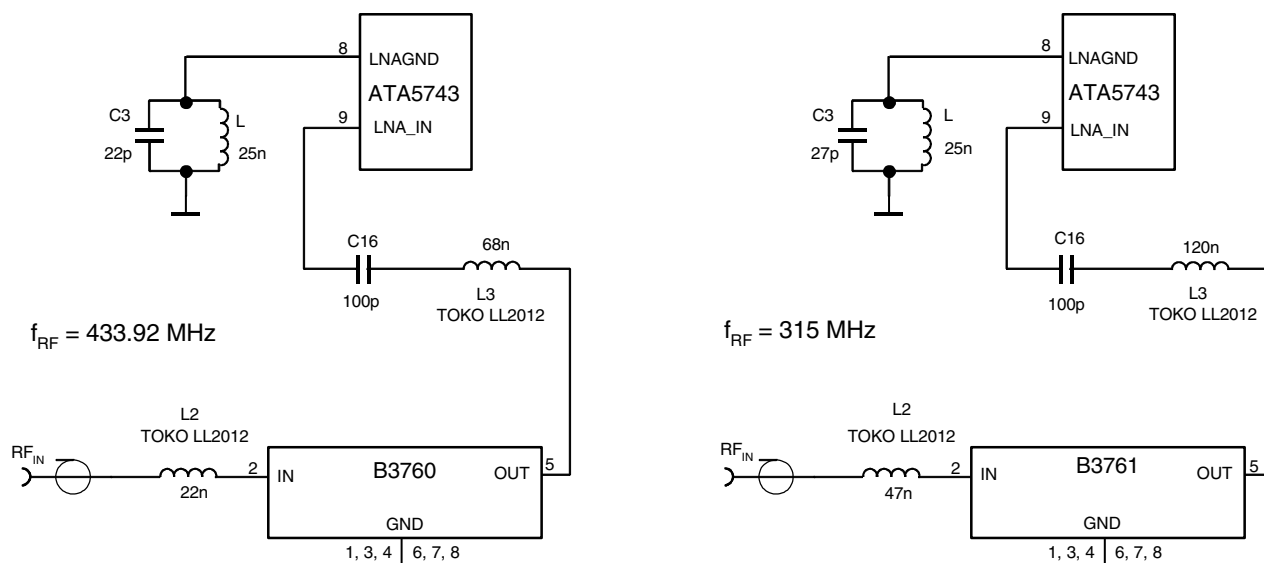
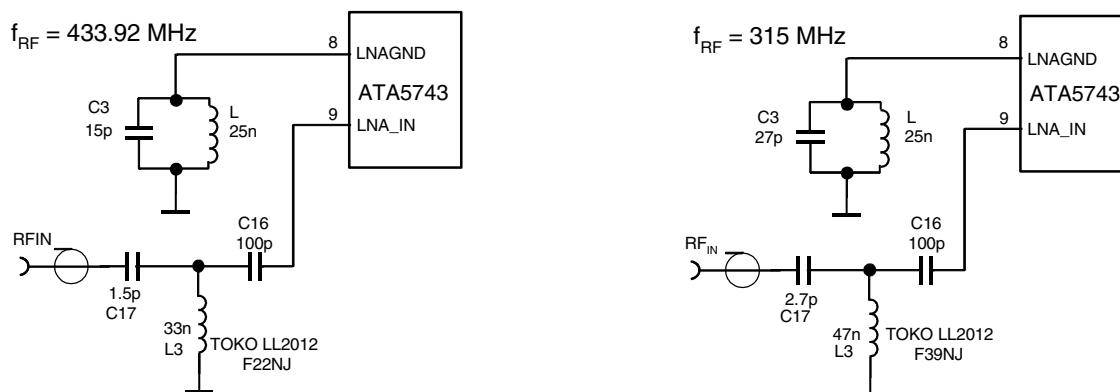
A good practice when designing the network is to start with power matching. From that starting point, the values of the components can be varied to some extent to achieve the best sensitivity.

If a SAW is implemented into the input network, a mirror frequency suppression of  $\Delta P_{\text{Ref}} = 40 \text{ dB}$  can be achieved. There are SAWs available that exhibit a notch at  $\Delta f = 2 \text{ MHz}$ . These SAWs work best for an intermediate frequency of  $f_{\text{IF}} = 1 \text{ MHz}$ . The selectivity of the receiver is also improved by using a SAW. In typical automotive applications, a SAW is used.

[Figure 4-2 on page 7](#) shows a typical input matching network, for  $f_{\text{RF}} = 315 \text{ MHz}$  and  $f_{\text{RF}} = 433.92 \text{ MHz}$ , using a SAW. [Figure 4-3 on page 7](#) illustrates an according input matching to  $50\Omega$  without a SAW. The input matching networks shown in [Figure 4-3 on page 7](#) are the reference networks for the parameters given in the table “[Electrical Characteristics](#)” on [page 33](#).

**Table 4-1.** Calculation of LO and IF Frequency

Conditions	Local Oscillator Frequency	Intermediate Frequency
$f_{\text{RF}} = 315 \text{ MHz}$ , MODE = 0	$f_{\text{LO}} = 314 \text{ MHz}$	$f_{\text{IF}} = 1 \text{ MHz}$
$f_{\text{RF}} = 433.92 \text{ MHz}$ , MODE = 1	$f_{\text{LO}} = 432.92 \text{ MHz}$	$f_{\text{IF}} = 1 \text{ MHz}$
$300 \text{ MHz} < f_{\text{RF}} < 365 \text{ MHz}$ , MODE = 0	$f_{\text{LO}} = \frac{f_{\text{RF}}}{1 + \frac{1}{314}}$	$f_{\text{IF}} = \frac{f_{\text{LO}}}{314}$
$365 \text{ MHz} < f_{\text{RF}} < 450 \text{ MHz}$ , MODE = 1	$f_{\text{LO}} = \frac{f_{\text{RF}}}{1 + \frac{1}{432.32}}$	$f_{\text{IF}} = \frac{f_{\text{LO}}}{432.92}$

**Figure 4-2.** Input Matching Network with SAW Filter

**Figure 4-3.** Input Matching Network without SAW Filter


Please notice that for all coupling conditions (see [Figure 4-2](#) and [Figure 4-3](#)), the bond wire inductivity of the LNA ground is compensated.  $C3$  forms a series resonance circuit together with the bond wire.  $L = 25 \text{ nH}$  is a feed inductor to establish a DC path. Its value is not critical, but must be large enough not to detune the series resonance circuit. For cost reduction this inductor can be easily printed on the PCB. This configuration improves the sensitivity of the receiver by about 1 to 2 dB.

## 5. Analog Signal Processing

### 5.1 IF Amplifier

The signals coming from the RF front-end are filtered by the fully integrated 4<sup>th</sup>-order IF filter. The IF center frequency is  $f_{IF} = 1$  MHz for applications where  $f_{RF} = 315$  MHz or  $f_{RF} = 433.92$  MHz. For other RF input frequencies refer to [Table 4-1 on page 6](#) to determine the center frequency.

The ATA5743 is available with two different IF bandwidths. ATA5743P3, the version with  $B_{IF} = 300$  kHz, is well suited for ASK systems where Atmel's PLL transmitter U2741B is used. The receiver ATA5743P6 employs an IF bandwidth of  $B_{IF} = 600$  kHz. Both versions can be used together with the U2741B in ASK and FSK mode. If used in ASK applications, higher tolerances for the receiver and PLL transmitter crystals are allowed. SAW transmitters exhibit much higher transmit frequency tolerances compared to PLL transmitters. Generally, it is necessary to use  $B_{IF} = 600$  kHz together with SAW transmitters.

### 5.2 RSSI Amplifier

The subsequent RSSI amplifier enhances the output signal of the IF amplifier before it is fed into the demodulator. The dynamic range of this amplifier is  $DR_{RSSI} = 60$  dB. If the RSSI amplifier is operated within its linear range, the best SNR is maintained in ASK mode. If the dynamic range is exceeded by the transmitter signal, the SNR is defined by the ratio of the maximum RSSI output voltage and the RSSI output voltage due to a disturber. The dynamic range of the RSSI amplifier is exceeded if the power of the input signal is 60 dB higher than the sensitivity of the receiver.

In FSK mode the SNR is not affected by the dynamic range of the RSSI amplifier.

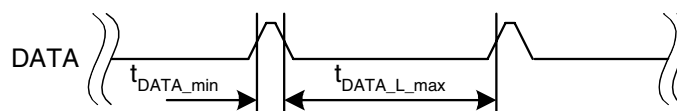
The output voltage of the RSSI amplifier is internally compared to a threshold voltage  $V_{Th\_red}$ .  $V_{Th\_red}$  is determined by the value of the external resistor  $R_{Sense}$ .  $R_{Sense}$  is connected between pin SENS and GND or  $V_S$ . The output of the comparator is fed into the digital control logic. By this means it is possible to operate the receiver at a lower sensitivity.

If  $R_{Sense}$  is connected to GND, the receiver operates at full sensitivity.

If  $R_{Sense}$  is connected to  $V_S$ , the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of  $R_{Sense}$ , the maximum sensitivity by the SNR of the LNA input. The reduced sensitivity depends on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is illustrated in [Figure 4-3 on page 7](#) and exhibits the best possible sensitivity.

$R_{Sense}$  can be connected to  $V_S$  or GND via a microcontroller. The receiver can be switched from full sensitivity to reduced sensitivity or vice versa at any time. In polling mode, the receiver will not wake up if the RF input signal does not exceed the selected sensitivity. If the receiver is already active, the data stream at pin DATA will disappear when the input signal is lower than defined by the reduced sensitivity. Instead of the data stream, the pattern shown in [Figure 5-1 on page 9](#) is issued at pin DATA to indicate that the receiver is still active (see [Figure 6-26 on page 29](#)).

**Figure 5-1.** Steady L State Limited DATA Output Pattern

### 5.3 FSK/ASK Demodulator and Data Filter

The signal coming from the RSSI amplifier is converted into the raw data signal by the ASK/FSK demodulator. The operating mode of the demodulator is set via the bit ASK/\_FSK in the OPMODE register. Logic 'L' sets the demodulator to FSK, applying 'H' to ASK mode.

In ASK mode, an automatic threshold control circuit (ATC) is used to set the detection reference voltage to a value where a good SNR is achieved. This circuit effectively suppresses any kind of inband noise signals or competing transmitters. If the SNR (ratio to suppress inband noise signals) exceeds 10 dB, the data signal can be detected properly.

The FSK demodulator is intended to be used for an FSK deviation of  $10 \text{ kHz} \leq \Delta f \leq 100 \text{ kHz}$ . In FSK mode the data signal can be detected if the SNR (ratio to suppress inband noise signals) exceeds 2 dB. This value is guaranteed for all modulation schemes of a disturber signal.

The output signal of the demodulator is filtered by the data filter before it is fed into the digital signal processing circuit. The data filter improves the SNR as its passband can be adopted to the characteristics of the data signal. The data filter consists of a 1<sup>st</sup>-order high-pass and a 2<sup>nd</sup>-order low-pass filter.

The high-pass filter cut-off frequency is defined by an external capacitor connected to pin CDEM. The cut-off frequency of the high-pass filter is defined by the following formula:

$$f_{cu\_DF} = \frac{1}{2 \times \pi \times 30 \text{ k}\Omega \times \text{CDEM}}$$

In self-polling mode, the data filter must settle very rapidly to achieve a low current consumption. Therefore, CDEM cannot be increased to very high values if self-polling is used. On the other hand, CDEM must be large enough to meet the data filter requirements according to the data signal. Recommended values for CDEM are given in the electrical characteristics.

The cut-off frequency of the low-pass filter is defined by the selected baud-rate range (BR\_Range). The BR\_Range is defined in the OPMODE register (refer to section [“Configuration of the Receiver” on page 24](#)). The BR\_Range must be set in accordance to the used baud rate.

The ATA5743 is designed to operate with data coding where the DC level of the data signal is 50%. This is valid for Manchester and Bi-phase coding. If other modulation schemes are used, the DC level should always remain within the range of  $V_{DC\_min} = 33\%$  and  $V_{DC\_max} = 66\%$ . Even then, the sensitivity will be reduced by up to 2 dB.

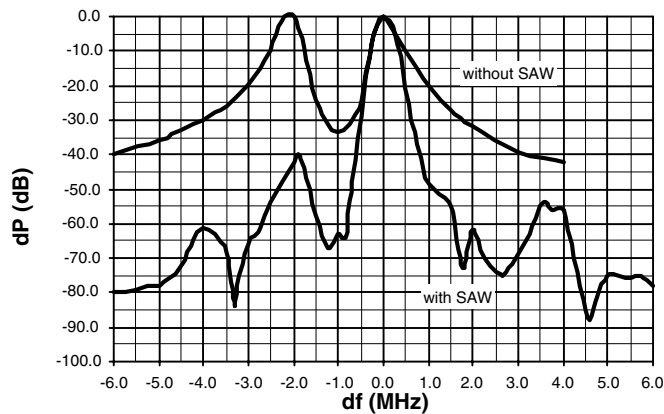
Each BR\_Range is also defined by a minimum and a maximum edge-to-edge time ( $t_{ee\_sig}$ ). These limits are defined in the electrical characteristics; to maintain full sensitivity of the receiver, they should not be exceeded.



## 5.4 Receiving Characteristics

The RF receiver ATA5743 can be operated with and without a SAW front-end filter. In a typical automotive application, a SAW filter is used to achieve better selectivity. The selectivity with and without a SAW front-end filter is illustrated in Figure 5-2. This example relates to ASK mode and the 300-kHz bandwidth version of the ATA5743. FSK mode and the 600-kHz bandwidth version of the receiver exhibit similar behavior. Note that the mirror frequency is reduced by 40 dB. The plots are printed relative to the maximum sensitivity. If a SAW filter is used, an insertion loss of about 4 dB must be considered.

**Figure 5-2.** Receiving Frequency Response



When designing the system in terms of receiving bandwidth, the LO deviation must be considered as it also determines the IF center frequency. The total LO deviation is calculated to be the sum of the deviation of the crystal and the XTO deviation of the ATA5743. Low-cost crystals are specified to be within  $\pm 100$  ppm. The XTO deviation of the ATA5743 is an additional deviation due to the XTO circuit. This deviation is specified to be  $\pm 30$  ppm. If a crystal of  $\pm 100$  ppm is used, the total deviation is  $\pm 130$  ppm in that case. Note that the receiving bandwidth and the IF-filter bandwidth are equivalent in ASK mode, but not in FSK mode.

## 6. Polling Circuit and Control Logic

The receiver is designed to consume less than 1 mA while being sensitive to signals from a corresponding transmitter. This is achieved via the polling circuit. This circuit enables the signal path periodically for a short time. During this time the bit-check logic verifies the presence of a valid transmitter signal. Only if a valid signal is detected will the receiver remain active and transfer the data to the connected microcontroller. If there is no valid signal present, the receiver remains in sleep mode most of the time, resulting in low current consumption; this condition is called polling mode. A connected microcontroller is disabled during this time.

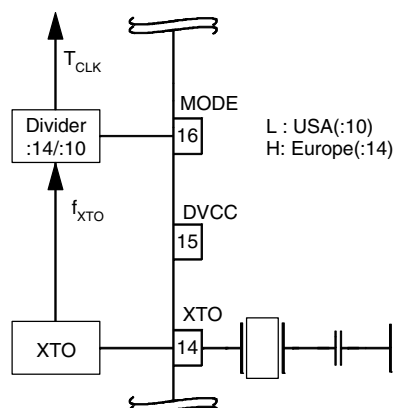
All relevant parameters of the polling logic can be configured by the connected microcontroller. This flexibility enables the user to meet the specifications in terms of current consumption, system response time, data rate, etc.

Regarding the number of connection wires to the microcontroller, the receiver is very flexible. It can be either operated by a single bi-directional line (to save ports to the connected microcontroller), or it can be operated by up to five uni-directional ports.

## 6.1 Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry and the analog filtering is derived from one clock. As seen in Figure 6-1, this clock cycle  $T_{CLK}$  is derived from the crystal oscillator (XTO) in combination with a divider. The division factor is controlled by the logical state at pin MODE. As described in section “RF Front-end” on page 5, the frequency of the crystal oscillator ( $f_{XTO}$ ) is defined by the RF input signal ( $f_{RFIn}$ ) which also defines the operating frequency of the local oscillator ( $f_{LO}$ ).

**Figure 6-1.** Generation of the Basic Clock Cycle



Pin MODE can now be set in accordance with the desired clock cycle  $T_{CLK}$ , which controls the following application relevant parameters:

- Timing of the polling circuit including bit check
- Timing of the analog and digital signal processing
- Timing of the register programming
- Frequency of the reset marker
- IF filter center frequency ( $f_{IF0}$ )

Most applications are dominated by two transmission frequencies:  $f_{Send} = 315$  MHz is mainly used in the USA,  $f_{Send} = 433.92$  MHz in Europe. In order to ease the usage of all  $T_{CLK}$ -dependent parameters on these electrical characteristics, here are displayed the three conditions for each parameter.

- Application USA ( $f_{XTO} = 4.90625$  MHz, MODE = L,  $T_{CLK} = 2.0383$   $\mu$ s)
- Application Europe ( $f_{XTO} = 6.76438$  MHz, MODE = H,  $T_{CLK} = 2.0697$   $\mu$ s)
- Other applications ( $T_{CLK}$  is dependent on  $f_{XTO}$  and on the logical state of pin MODE. The electrical characteristic is given as a function of  $T_{CLK}$ ).

The clock cycle of some function blocks depends on the selected baud-rate range (BR\_Range) which is defined in the OPMODE register. This clock cycle  $T_{XCLK}$  is defined by the following formulas for further reference:

BR_Range =	BR_Range0:	$T_{XCLK} = 8 \times T_{CLK}$
	BR_Range1:	$T_{XCLK} = 4 \times T_{CLK}$
	BR_Range2:	$T_{XCLK} = 2 \times T_{CLK}$
	BR_Range3:	$T_{XCLK} = 1 \times T_{CLK}$

## 6.2 Polling Mode

As shown in [Figure 6-2 on page 13](#), the receiver's polling mode consists of a continuous cycle of three different modes. In sleep mode, the signal processing circuitry is disabled for the time period  $T_{\text{Sleep}}$  while consuming low current of  $I_S = I_{\text{Soff}}$ . During the start-up period,  $T_{\text{Startup}}$ , all signal processing circuits are enabled and settled. In the following bit-check mode, the incoming data stream is analyzed bit-by-bit, looking for a valid transmitter signal. If no valid signal is present, the receiver is set back to sleep mode after the period  $T_{\text{Bit-check}}$ . This period varies check-by-check as it is a statistical process. An average value for  $T_{\text{Bit-check}}$  is given in the electrical characteristics. During  $T_{\text{Startup}}$  and  $T_{\text{Bit-check}}$ , the current consumption is  $I_S = I_{\text{Son}}$ . The condition of the receiver is indicated on pin IC\_ACTIVE.

The average current consumption in polling mode is dependent on the duty cycle of the active mode and can be calculated as:

$$I_{\text{Spoll}} = \frac{I_{\text{Soff}} \times T_{\text{Sleep}} + I_{\text{Son}} \times (T_{\text{Startup}} + T_{\text{Bit-check}})}{T_{\text{Sleep}} + T_{\text{Startup}} + T_{\text{Bit-check}}}$$

During  $T_{\text{Sleep}}$  and  $T_{\text{Startup}}$ , the receiver is not sensitive to a transmitter signal. To guarantee the reception of a transmitted command, the transmitter must start the telegram with an adequate preburst. The required length of the preburst depends on the polling parameters  $T_{\text{Sleep}}$ ,  $T_{\text{Startup}}$ ,  $T_{\text{Bit-check}}$ , and the start-up time of a connected microcontroller ( $T_{\text{Start}}$ ,  $\mu\text{C}$ ). Thus,  $T_{\text{Bit-check}}$  depends on the actual bit rate and the number of bits ( $N_{\text{Bit-check}}$ ) to be tested.

The following formula indicates how to calculate the preburst length.

$$T_{\text{Peburst}} \geq T_{\text{Sleep}} + T_{\text{Startup}} + T_{\text{Bit-check}} + T_{\text{Start}} \mu\text{C}$$

## 6.3 Sleep Mode

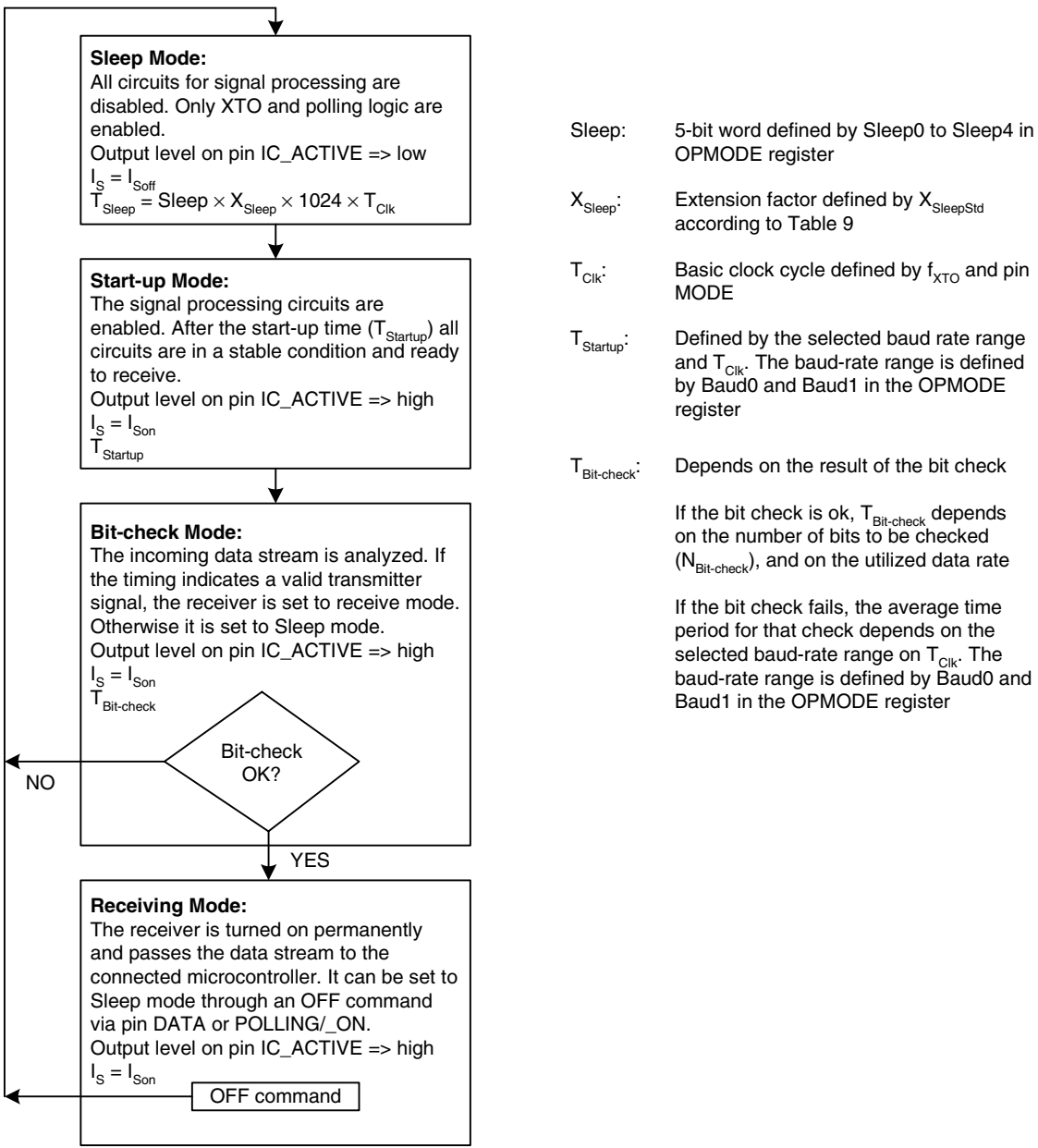
The length of period  $T_{\text{Sleep}}$  is defined by the 5-bit word Sleep of the OPMODE register, the extension factor  $X_{\text{Sleep}}$  (see [Table 6-8 on page 26](#)), and the basic clock cycle  $T_{\text{Cik}}$ . It is calculated to be:

$$T_{\text{Sleep}} = \text{Sleep} \times X_{\text{Sleep}} \times 1024 \times T_{\text{Cik}}$$

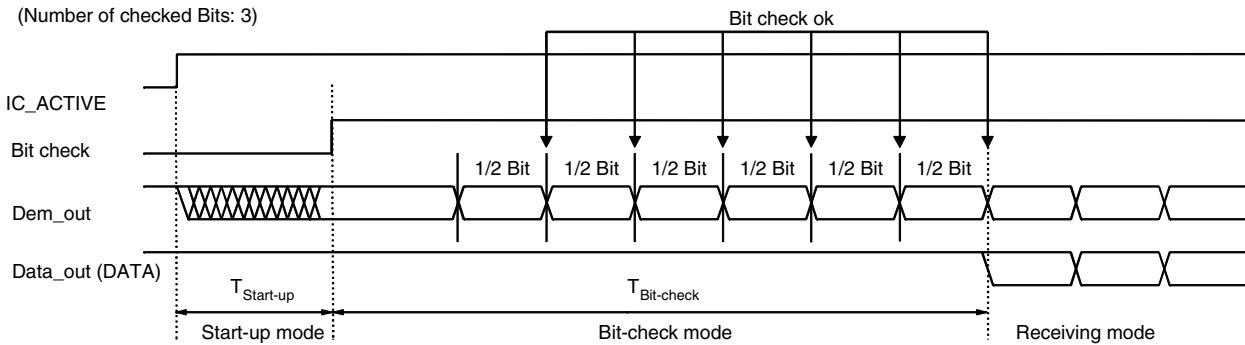
In US and European applications, the maximum value of  $T_{\text{Sleep}}$  is about 60 ms if  $X_{\text{Sleep}}$  is set to "1"; the time resolution is about 2 ms in that case. The sleep time can be extended to almost half a second by setting  $X_{\text{Sleep}}$  to 8.  $X_{\text{Sleep}}$  can be set to 8 by setting bit  $X_{\text{SleepStd}}$  to "1".

As seen in [Table 6-7 on page 26](#), the highest register value of sleep sets the receiver into a permanent sleep condition. The receiver remains in that condition until another value for Sleep is programmed into the OPMODE register. This function is desirable where several devices share a single data line and may also be used for microcontroller polling – via pin POLLING/\_ON, the receiver can be switched on and off.

Figure 6-2. Polling Mode Flow Chart



**Figure 6-3.** Timing Diagram for Complete Successful Bit Check



### 6.3.1 Bit-check Mode

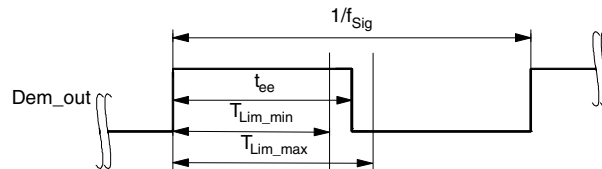
In bit-check mode the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter, and signals due to noise. This is done by subsequent time frame checks where the distances between two signal edges are continuously compared to a programmable time window. The maximum count of this edge-to-edge test before the receiver switches to receiving mode is also programmable.

### 6.3.2 Configuring the Bit Check

Assuming a modulation scheme that contains two edges per bit, two time frame checks verify one bit. This is valid for Manchester, Bi-phase, and most other modulation schemes. The maximum count of bits to be checked can be set to 0, 3, 6 or 9 bits via the variable  $N_{Bit-check}$  in the OPMODE register. This implies 0, 6, 12 and 18 edge-to-edge checks, respectively. If  $N_{Bit-check}$  is set to a higher value, the receiver is less likely to switch to receiving mode due to noise. In the presence of a valid transmitter signal, the bit check takes less time if  $N_{Bit-check}$  is set to a lower value. In polling mode, the bit-check time is not dependent on  $N_{Bit-check}$ . Figure 6-3 shows an example where 3 bits are tested successfully and the data signal is transferred to pin DATA.

As demonstrated in Figure 6-4, the time window for the bit check is defined by two separate time limits. If the edge-to-edge time  $t_{ee}$  is between the lower bit-check limit,  $T_{Lim\_min}$ , and the upper bit-check limit,  $T_{Lim\_max}$ , the check will be continued. If  $t_{ee}$  is smaller than  $T_{Lim\_min}$ , or  $t_{ee}$  exceeds  $T_{Lim\_max}$ , the bit check will be terminated and the receiver will switch to sleep mode.

**Figure 6-4.** Valid Time Window for Bit Check



For best noise immunity it is recommended to use a low span between  $T_{Lim\_min}$  and  $T_{Lim\_max}$ . This is achieved by using a fixed frequency at a 50% duty cycle for the transmitter preburst. For this reason, a “11111...” or a “10101...” sequence in Manchester or Bi-phase is a good choice. A good compromise between receiver sensitivity and susceptibility to noise is a time window of  $\pm 25\%$  regarding the expected edge-to-edge time  $t_{ee}$ . Using preburst patterns that contain various edge-to-edge time periods, the bit-check limits must be programmed according to the required span.

The bit-check limits are determined by means of the formula below.

$$T_{\text{Lim\_min}} = \text{Lim\_min} \times T_{\text{XClk}}$$

$$T_{\text{Lim\_max}} = (\text{Lim\_max} - 1) \times T_{\text{XClk}}$$

Lim\_min and Lim\_max are defined by a 5-bit word each within the LIMIT register.

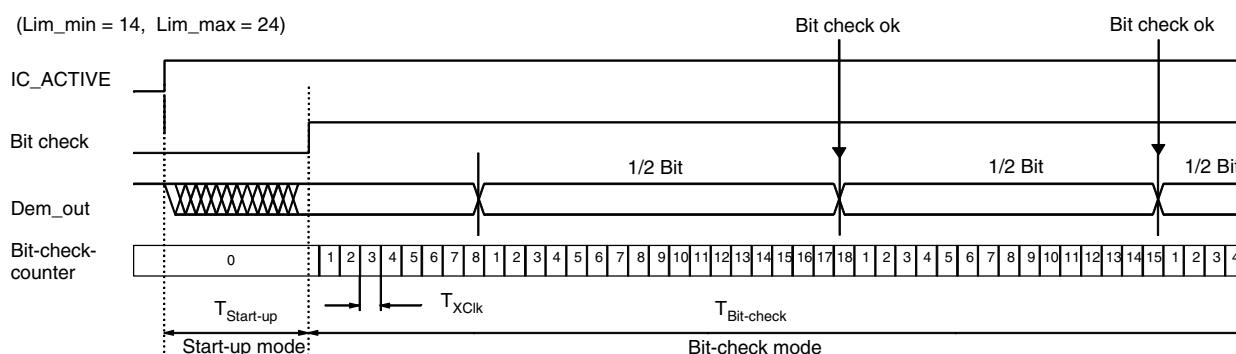
Using the above formulas, Lim\_min and Lim\_max can be determined according to the required  $T_{\text{Lim\_min}}$ ,  $T_{\text{Lim\_max}}$  and  $T_{\text{XClk}}$ . The time resolution defining  $T_{\text{Lim\_min}}$  and  $T_{\text{Lim\_max}}$  is  $T_{\text{XClk}}$ . The minimum edge-to-edge time  $t_{\text{ee}}$  ( $t_{\text{DATA\_L\_min}}$ ,  $t_{\text{DATA\_H\_min}}$ ) is defined in the section “[Digital Signal Processing](#)” on page 16. The lower limit should be set to  $\text{Lim\_min} \geq 10$ . The maximum value of the upper limit is  $\text{Lim\_max} = 63$ .

If the calculated value for Lim\_min is  $< 19$ , it is recommended to check 6 or 9 bits ( $N_{\text{Bit-check}}$ ) to prevent switching to receiving mode due to noise.

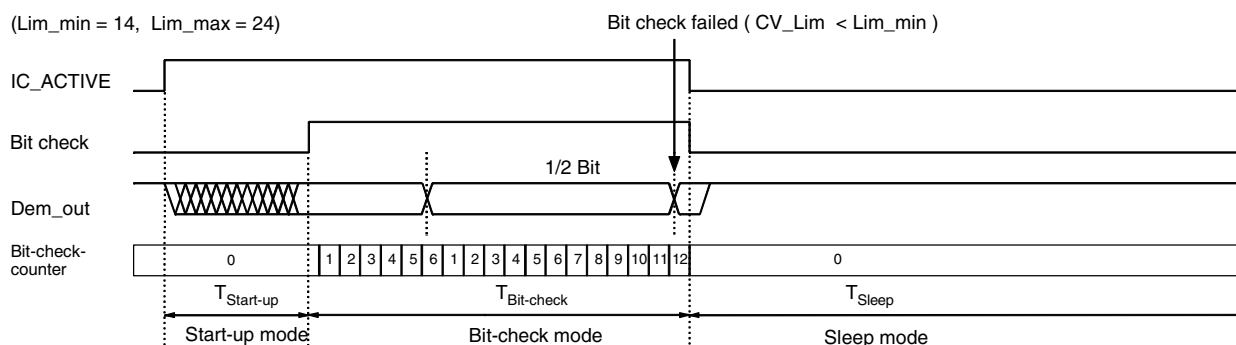
Figure 6-5, Figure 6-6 and Figure 6-7 on page 16 illustrate the bit check for the bit-check limits Lim\_min = 14 and Lim\_max = 24. When the IC is enabled, the signal processing circuits are enabled during  $T_{\text{Startup}}$ . The output of the ASK/FSK demodulator (Dem\_out) is undefined during that period. When the bit check becomes active, the bit-check counter is clocked with the cycle  $T_{\text{XClk}}$ .

Figure 6-5 shows how the bit check proceeds if the bit-check counter value CV\_Lim is within the limits defined by Lim\_min and Lim\_max at the occurrence of a signal edge. In Figure 6-6 the bit check fails as the value CV\_Lim is lower than the limit Lim\_min. The bit check also fails if CV\_Lim reaches Lim\_max. This is illustrated in Figure 6-7 on page 16.

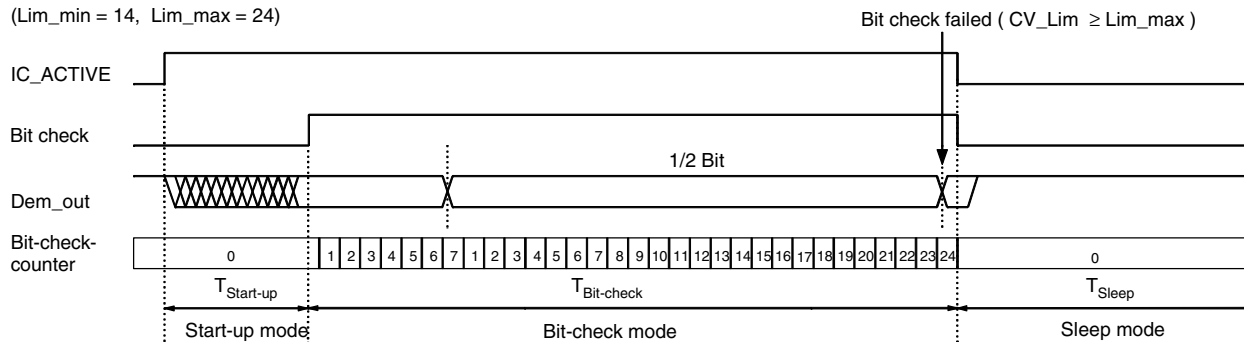
**Figure 6-5.** Timing Diagram During Bit Check



**Figure 6-6.** Timing Diagram for Failed Bit Check (Condition:  $\text{CV\_Lim} < \text{Lim\_min}$ )



**Figure 6-7.** Timing Diagram for Failed Bit Check (Condition:  $CV\_Lim \geq Lim\_max$ )



### 6.3.3 Duration of the Bit Check

If no transmitter signal is present during the bit check, the output of the ASK/FSK demodulator delivers random signals. The bit check is a statistical process and  $T_{Bit-check}$  varies for each check. Therefore, an average value for  $T_{Bit-check}$  is given in the electrical characteristics.  $T_{Bit-check}$  depends on the selected baud-rate range and on  $T_{Clk}$ . A higher baud-rate range causes a lower value for  $T_{Bit-check}$ , resulting in lower current consumption in polling mode.

In the presence of a valid transmitter signal,  $T_{Bit-check}$  is dependent on the frequency of that signal,  $f_{Sig}$ , and the count of the checked bits,  $N_{Bit-check}$ . A higher value for  $N_{Bit-check}$  thereby results in a longer period for  $T_{Bit-check}$ , requiring a higher value for the transmitter preburst,  $T_{Preburst}$ .

### 6.3.4 Receiving Mode

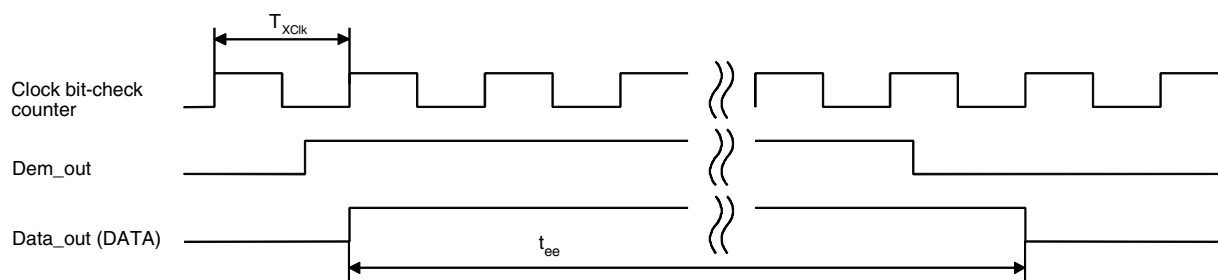
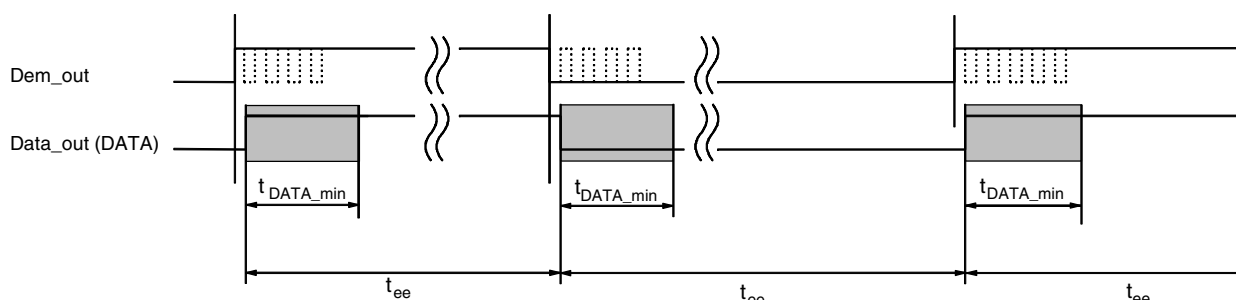
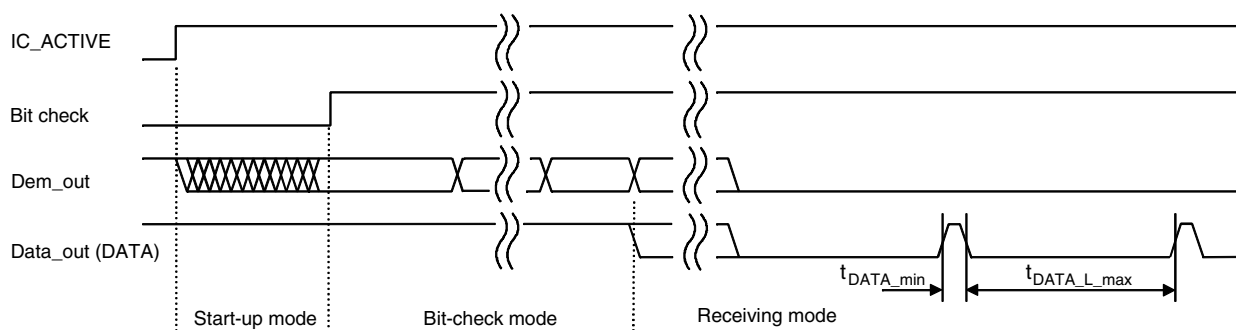
If the bit check was successful for all bits specified by  $N_{Bit-check}$ , the receiver switches to receiving mode. As shown in [Figure 6-3 on page 14](#), the internal data signal is then switched to pin DATA, and the data clock is available after the start bit has been detected ([Figure 6-14 on page 20](#)). A connected microcontroller can be woken up by the negative edge at pin DATA or by the data clock at pin DATA\_CLK. The receiver stays in that condition until it is switched back to polling mode explicitly.

### 6.3.5 Digital Signal Processing

The data from the ASK/FSK demodulator (Dem\_out) is digitally processed in different ways and converted into the output signal data. This processing depends on the selected baud-rate range (BR\_Range). [Figure 6-8 on page 17](#) illustrates how Dem\_out is synchronized by the extended clock cycle  $T_{XClk}$ . This clock is also used for the bit-check counter. Data can change its state only after  $T_{XClk}$  has elapsed. The edge-to-edge time period  $t_{ee}$  of the Data signal, as a result, is always an integral multiple of  $T_{XClk}$ .

The minimum time period between two edges of the data signal is limited to  $t_{ee} \geq T_{DATA\_min}$  (see [Figure 6-9 on page 17](#)). This implies an efficient suppression of spikes at the DATA output during data reception. At the same time, it limits the maximum frequency of edges at DATA. This eases the interrupt handling of a connected microcontroller.

The maximum time period for DATA to stay Low is limited to  $T_{DATA\_L\_max}$ . This function is employed to ensure a finite response time in programming or switching off the receiver via pin DATA.  $T_{DATA\_L\_max}$  is thereby longer than the maximum time period indicated by the transmitter data stream. [Figure 6-10 on page 17](#) shows an example where Dem\_out remains Low after the receiver has switched to receiving mode.

**Figure 6-8.** Synchronization of the Demodulator Output**Figure 6-9.** Debouncing of the Demodulator Output**Figure 6-10.** Steady L State Limited DATA Output Pattern After Transmission

After the end of a data transmission, the receiver remains active. Depending on the bit Noise\_Disable in the OPMODE register, the output signal at pin DATA is high, or random noise pulses appear at pin DATA (see section [“Digital Noise Suppression”](#) on page 22). The edge-to-edge time period  $t_{ee}$  of the majority of these noise pulses is equal or slightly higher than  $T_{DATA\_min}$ .



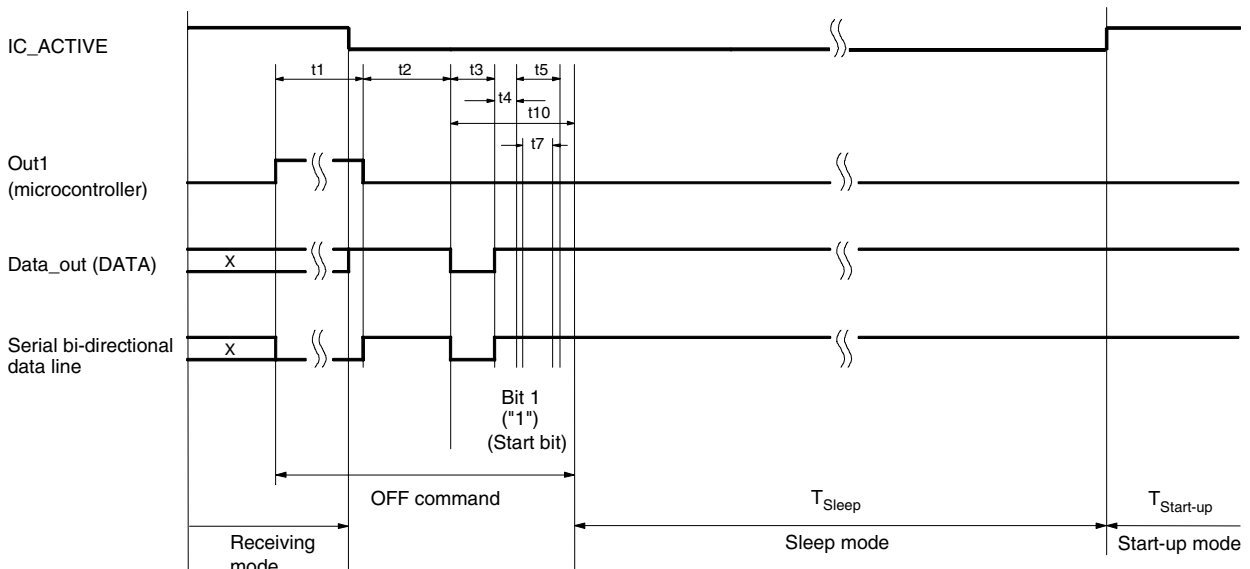
### 6.3.6 Switching the Receiver Back to Sleep Mode

The receiver can be set back to polling mode via pin DATA or via pin POLLING/\_ON.

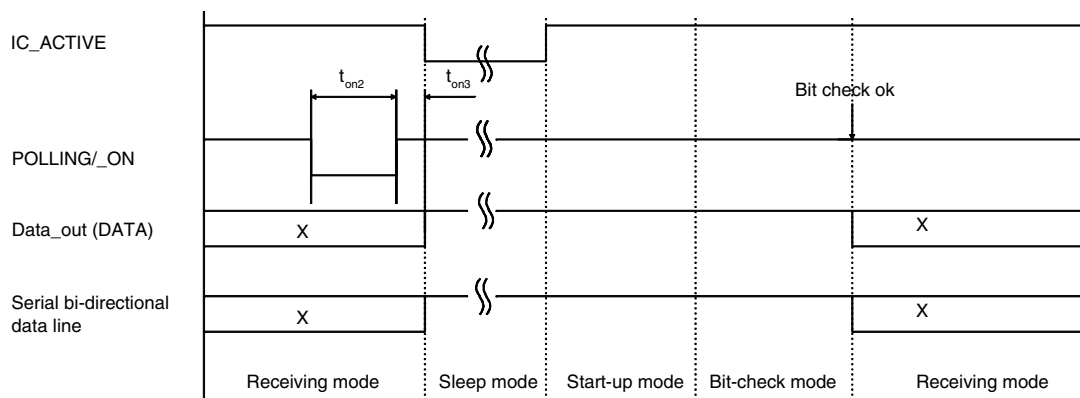
When using pin DATA, this pin must be pulled to Low by the connected microcontroller for the period  $t_1$ . Figure 6-11 illustrates the timing of the OFF command (see also Figure 6-26 on page 29). The minimum value of  $t_1$  depends on BR\_Range. The maximum value for  $t_1$  is not limited, but it is recommended not to exceed the specified value to prevent erasing the reset marker. (see section “Programming the Configuration Register” on page 28) Note also that an internal reset for the OPMODE and the LIMIT register will be generated if  $t_1$  exceeds the specified values. This item is explained in more detail in the section “Configuration of the Receiver” on page 24. Setting the receiver to sleep mode via DATA is achieved by programming bit 1 to be “1” during the register configuration. Only one sync pulse ( $t_3$ ) is issued.

The duration of the OFF command is determined by the sum of  $t_1$ ,  $t_2$  and  $t_{10}$ . After the OFF command the sleep time  $T_{\text{Sleep}}$  elapses. Note that the capacitive load at pin DATA is limited (see section “Data Interface” on page 30).

**Figure 6-11.** Timing Diagram of the OFF command via Pin DATA



**Figure 6-12.** Timing Diagram of the OFF command via Pin POLLING/\_ON



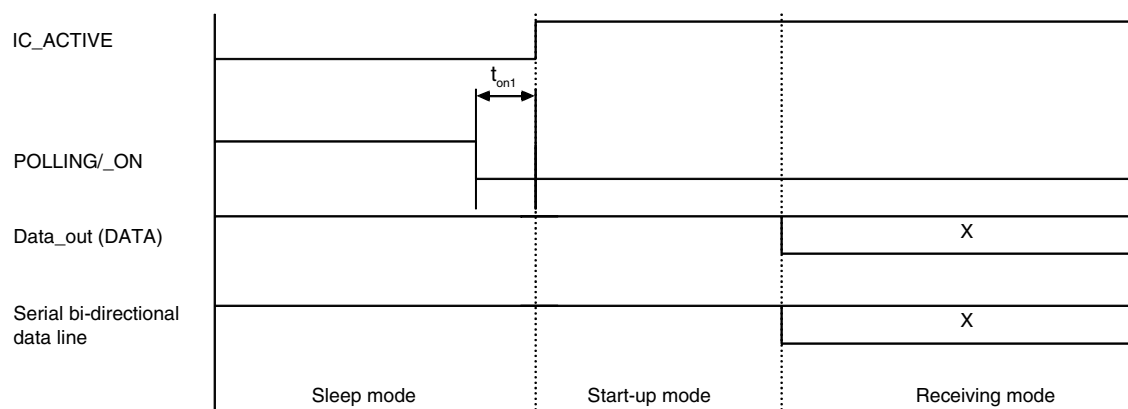
**Figure 6-13.** Activating the Receiving Mode via Pin POLLING/\_ON

Figure 6-12 on page 18 illustrates how to set the receiver back to polling mode via pin POLLING/\_ON. The pin POLLING/\_ON must be held to low for the time period  $t_{on2}$ . After the positive edge on pin POLLING/\_ON and the delay  $t_{on3}$ , the polling mode is active and the sleep time  $T_{Sleep}$  elapses.

This command is faster than using pin DATA, but at the cost of an additional connection to the microcontroller.

Figure 6-13 illustrates how to set the receiver to receive mode via the pin POLLING/\_ON. The pin POLLING/\_ON must be held to Low. After the delay  $t_{on1}$ , the receiver changes from sleep mode to start-up mode regardless of the programmed values for  $T_{Sleep}$  and  $N_{Bit-check}$ . As long as POLLING/\_ON is held to Low, the values for  $T_{Sleep}$  and  $N_{Bit-check}$  will be ignored, but not deleted (see section “Digital Noise Suppression” on page 22).

If the receiver is polled exclusively by a microcontroller,  $T_{Sleep}$  must be programmed to 31 (permanent sleep mode). In this case, the receiver remains in sleep mode as long as POLLING/\_ON is held to High.

## 6.4 Data Clock

The pin DATA\_CLK makes a data shift clock available to sample the data stream into a shift register. Using this data clock, a microcontroller can easily synchronize the data stream. This clock can only be used for Manchester- and Bi-phase-coded signals.

### 6.4.1 Generation of the Data Clock

After a successful bit check, the receiver switches from polling mode to receiving mode and the data stream is available at pin DATA. In receiving mode, the data clock control logic (Manchester/Bi-phase demodulator) is active and examines the incoming data stream. This is done, as in the bit check, by subsequent time frame checks where the distance between two edges is continuously compared to a programmable time window. As illustrated in Figure 6-14 on page 20, only two distances between two edges in Manchester- and Bi-phase-coded signals are valid ( $T$  and  $2T$ ).

The limits for  $T$  are the same as used for the bit check. They can be programmed in the LIMIT-register (Lim\_min and Lim\_max, see Table 6-10 on page 27 and Table 6-11 on page 27).

The limits for 2T are calculated as follows:

Lower limit of 2T:  $\text{Lim\_min\_2T} = (\text{Lim\_min} + \text{Lim\_max}) - (\text{Lim\_max} - \text{Lim\_min})/2$

Upper limit of 2T:  $\text{Lim\_max\_2T} = (\text{Lim\_min} + \text{Lim\_max}) + (\text{Lim\_max} - \text{Lim\_min})/2$

Note: If the result for “Lim\_min\_2T” or “Lim\_max\_2T” is not an integer value, it will be rounded up.

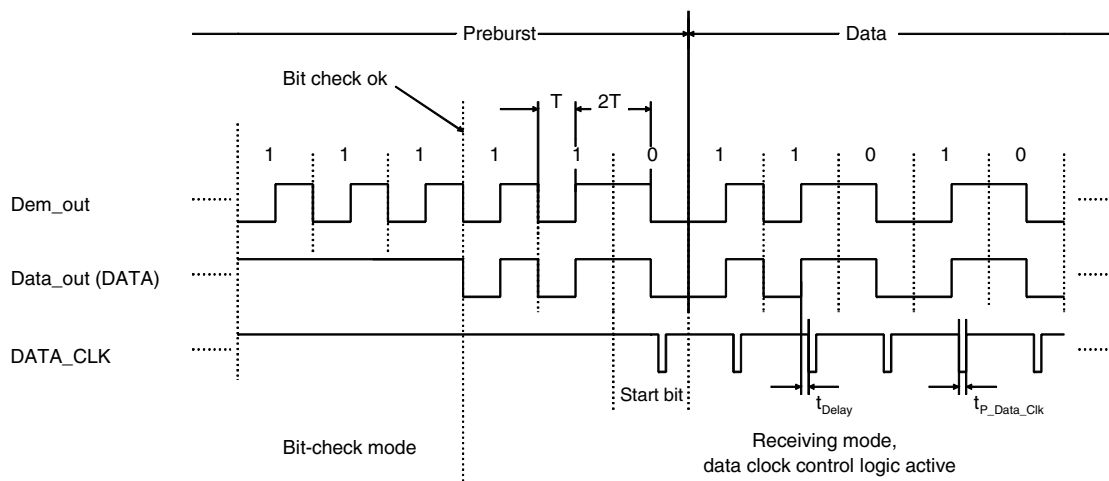
The data clock is available after the data clock control logic has detected the distance 2T (Start bit), and then issues pulses with a delay of  $t_{\text{Delay}}$  after the edges on pin DATA (see Figure 6-14).

If the data clock control logic detects a timing or logical error (Manchester code violation), as illustrated in Figure 6-15 and Figure 6-16 on page 21, it stops the output of the data clock. The receiver remains in receiving mode and starts with the bit check. If the bit check was successful and the start bit has been detected, the data clock control logic starts again with the generation of the data clock (see Figure 6-17 on page 21).

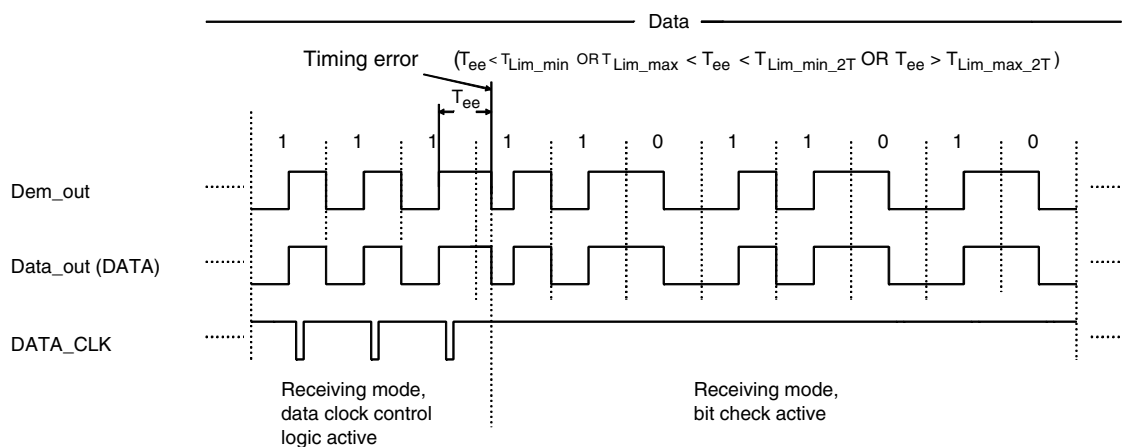
It is recommended to use the function of the data clock only in conjunction with the bit check 3, 6 or 9. If the bit check is set to 0 or the receiver is set to receiving mode via the pin POLLING/\_ON, the data clock is available if the data clock control logic has detected the distance 2T (Start bit).

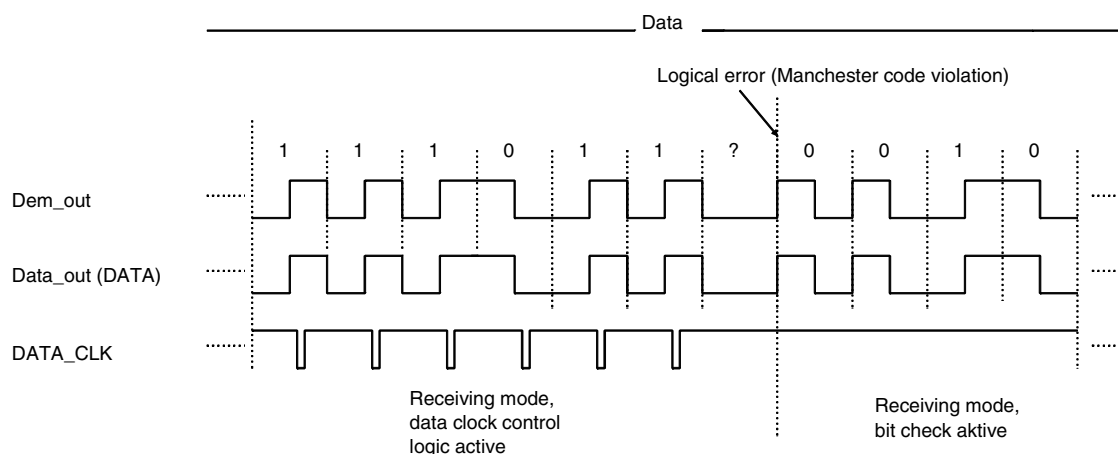
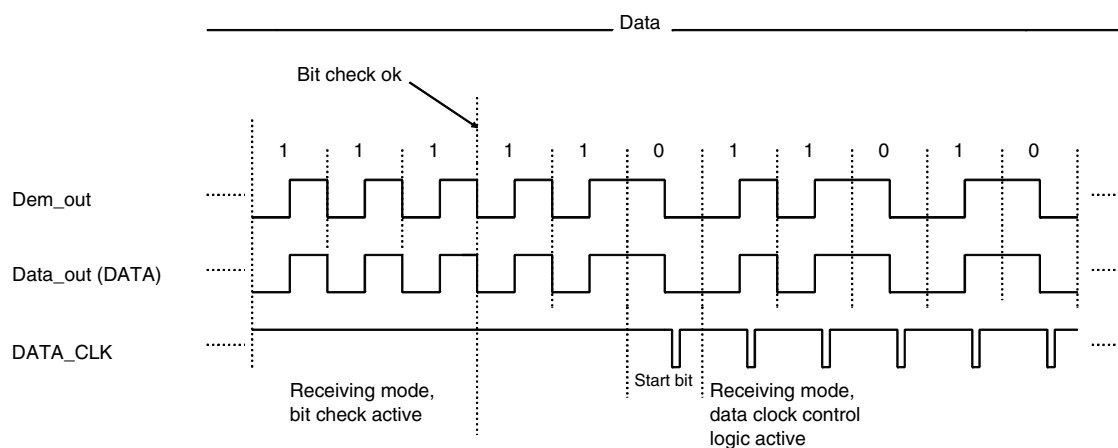
Note that for Bi-phase-coded signals, the data clock is issued at the end of the bit.

**Figure 6-14.** Timing Diagram of the Data Clock



**Figure 6-15.** Data Clock Disappears Because of a Timing Error



**Figure 6-16.** Data Clock Disappears Because of a Logical Error**Figure 6-17.** Output of the Data Clock After a Successful Bit Check

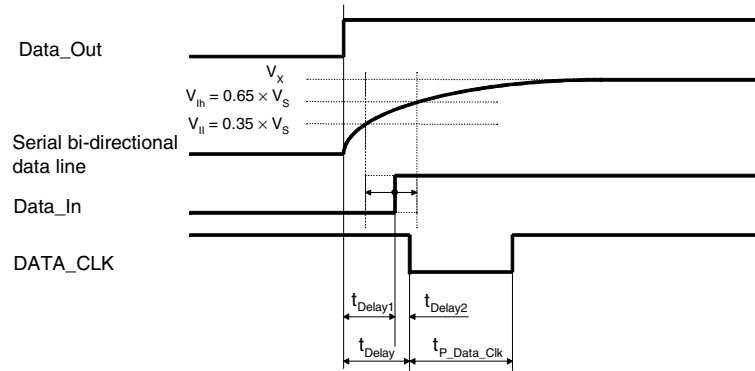
The delay of the data clock is calculated as follows:

$$t_{\text{Delay}} = t_{\text{Delay1}} + t_{\text{Delay2}}$$

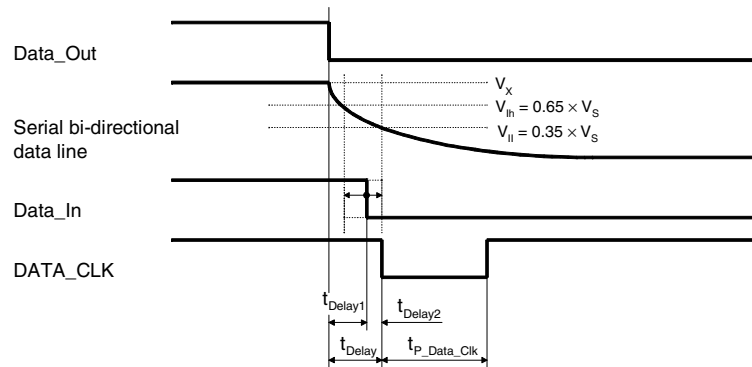
$t_{\text{Delay1}}$  is the delay between the internal signals Data\_Out and Data\_In. For the rising edge,  $t_{\text{Delay1}}$  depends on the capacitive load  $C_L$  at pin DATA and the external pull-up resistor  $R_{\text{pup}}$ . For the falling edge,  $t_{\text{Delay1}}$  depends additionally on the external voltage  $V_X$  (see [Figure 6-18 on page 22](#), [Figure 6-19 on page 22](#) and [Figure 6-26 on page 29](#)). When the level of Data\_In is equal to the level of Data\_Out, the data clock is issued after an additional delay  $t_{\text{Delay2}}$ .

Note that the capacitive load at pin DATA is limited. If the maximum tolerated capacitive load at pin DATA is exceeded, the data clock disappears (see section ["Data Interface" on page 29](#)).

**Figure 6-18.** Timing Characteristic of the Data Clock (Rising Edge on Pin DATA)



**Figure 6-19.** Timing Characteristic of the Data Clock (Falling Edge on Pin DATA)



## 6.5 Digital Noise Suppression

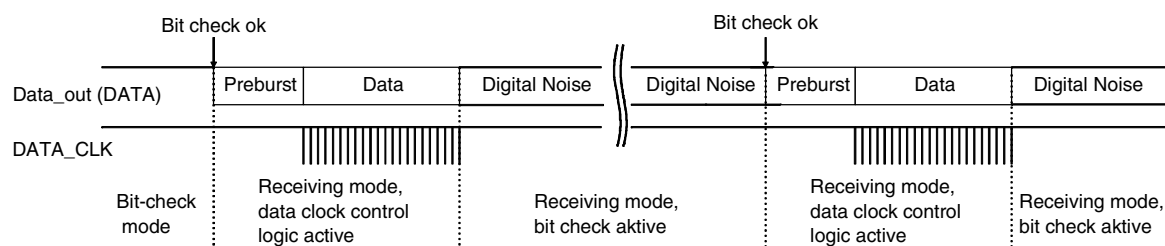
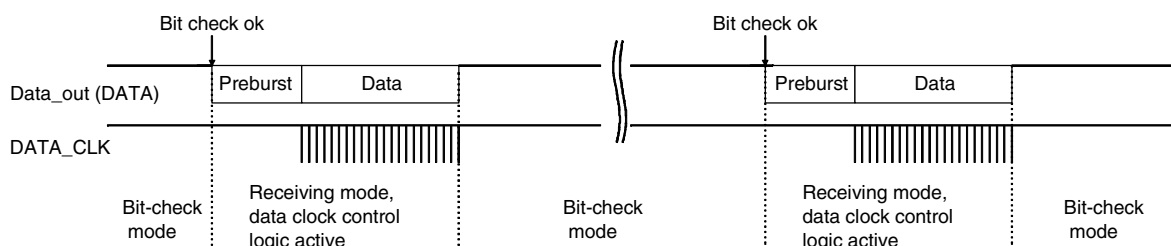
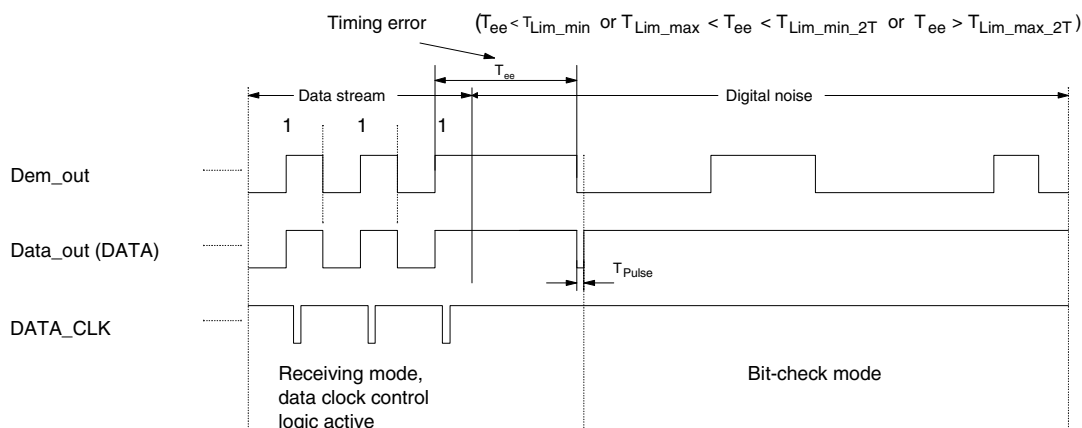
After a data transmission, digital noise appears on the data output (see [Figure 6-20 on page 23](#)). To prevent digital noise from keeping the connected microcontroller busy, it can be suppressed in two different ways.

### 6.5.1 Automatic Noise Suppression

The automatic noise suppression is illustrated in [Figure 6-21 on page 23](#). If the bit Noise\_Disable ([Table 6-9 on page 26](#)) in the OPMODE register is set to “1” (default), the receiver changes to bit-check mode at the end of a valid data stream. The digital noise is suppressed and the level at pin DATA is High in that case. The receiver changes back to receiving mode, if the bit check was successful.

This way of suppressing the noise is recommended if the data stream is Manchester or Bi-phase coded and is active after power on.

[Figure 6-22 on page 23](#) illustrates the behavior of the data output at the end of a data stream. Note that if the last period of the data stream is a high period (rising edge to falling edge), a pulse occurs on pin DATA. The length of the pulse depends on the selected baud-rate range.

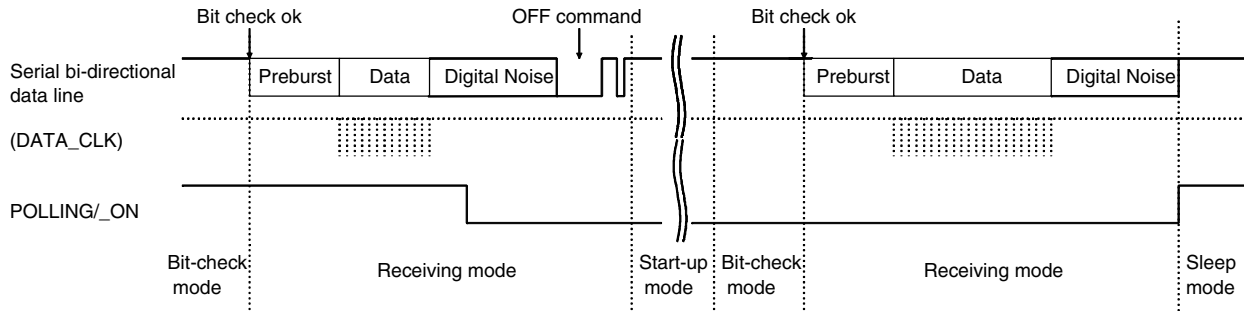
**Figure 6-20.** Output of Digital Noise at the End of the Data Stream**Figure 6-21.** Automatic Noise Suppression**Figure 6-22.** Occurrence of a Pulse at the End of the Data Stream

### 6.5.2 Controlled Noise Suppression by the Microcontroller

The controlled noise suppression is illustrated in [Figure 6-23 on page 24](#). If the bit `Noise_Disable` (see [Table 6-9 on page 26](#)) in the `OPMODE` register is set to "0", digital noise appears at the end of a valid data stream. To suppress the noise, the pin `POLLING/_ON` must be set to Low. The receiver remains in receiving mode. Then, the OFF command causes the change to the start-up mode. The programmed sleep time (see [Table 6-7 on page 26](#)) will not be executed because the level at pin `POLLING/_ON` is Low, but the bit check is active. The OFF command activates the bit check also if the pin `POLLING/_ON` is held to Low. The receiver changes back to receiving mode if the bit check was successful. To activate the polling mode at the end of the data transmission, the pin `POLLING/_ON` must be set to High.

This way of suppressing the noise is recommended if the data stream is not Manchester or Bi-phase coded.

**Figure 6-23. Controlled Noise Suppression**



## 6.6 Configuration of the Receiver

The ATA5743 receiver is configured via two 12-bit RAM registers called OPMODE and LIMIT. The registers can be programmed by means of the bi-directional DATA port. If the register contents have changed due to a voltage drop, this condition is indicated by a certain output pattern called reset marker (RM). The receiver must be reprogrammed in that case. After a power-on reset (POR), the registers are set to default mode. If the receiver is operated in default mode, there is no need to program the registers. [Table 6-3 on page 25](#) shows the structure of the registers. As seen in [Table 6-1](#), bit 1 defines if the receiver is set back to polling mode via the OFF command (see section [“Receiving Mode” on page 16](#)) or if it is programmed. Bit 2 represents the register address. It selects the appropriate register to be programmed. To get a high programming reliability, bit 15 (Stop bit), at the end of the programming operation, must be set to “0”.

**Table 6-1. Effect of Bit 1 and Bit 2 on Programming the Registers**

Bit 1	Bit 2	Action
1	x	The receiver is set back to polling mode (OFF command)
0	1	The OPMODE register is programmed
0	0	The LIMIT register is programmed

**Table 6-2. Effect of Bit 15 on Programming the Register**

Bit 15	Action
0	The values will be written into the register (OPMODE or LIMIT)
1	The values will not be written into the register

**Table 6-3.** Effect of the Configuration Words Within the Registers

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
OFF command														
1														
OPMODE register														
0	1	BR_Range		N <sub>Bit-check</sub>		Modu-lat ion	Sleep					X Sleep	Noise Suppression	0
		Baud1	Baud0	BitChk1	BitChk0	ASK/_ FSK	Sleep4	Sleep3	Sleep2	Sleep1	Sleep0	X <sub>SleepStd</sub>	Noise_ Disable	
Default values of bits 3 to 14		0	0	0	1	0	0	0	1	1	0	0	1	
LIMIT register														
0	0	Lim_min						Lim_max						0
		Lim_ min5	Lim_ min4	Lim_ min3	Lim_ min2	Lim_ min1	Lim_ min0	Lim_ max5	Lim_ max4	Lim_ max3	Lim_ max2	Lim_ max1	Lim_ max0	
Default values of bits 3 to 14		0	1	0	1	0	1	1	0	1	0	0	1	

Table 6-4 on page 25 to Table 6-11 on page 27 illustrate the effect of the individual configuration words. The default configuration is highlighted for each word.

BR\_Range sets the appropriate baud-rate range and simultaneously defines XLim. XLim is used to define the bit-check limits  $T_{Lim\_min}$  and  $T_{Lim\_max}$  as shown in Table 6-10 on page 27 and Table 6-11 on page 27.

**Table 6-4.** Effect of the Configuration Word BR\_Range

BR_Range		Baud-Rate Range/Extension Factor for Bit-Check Limits (XLim)
Baud1	Baud0	
0	0	BR_Range0 (application USA/Europe: BR_Range0 = 1.0 kBaud to 1.8 kBaud) XLim = 8 (default)
0	1	BR_Range1 (application USA/Europe: BR_Range1 = 1.8 kBaud to 3.2 kBaud) XLim = 4
1	0	BR_Range2 (application USA/Europe: BR_Range2 = 3.2 kBaud to 5.6 kBaud) XLim = 2
1	1	BR_Range3 (application USA/Europe: BR_Range3 = 5.6 kBaud to 10 kBaud) XLim = 1

**Table 6-5.** Effect of the Configuration Word N<sub>Bit-check</sub>

N <sub>Bit-check</sub>		Number of Bits to be Checked
BitChk1	BitChk0	
0	0	0
0	1	3 (default)
1	0	6
1	1	9



**Table 6-6.** Effect of the Configuration Bit Modulation

Modulation	Selected Modulation
ASK/_FSK	
0	FSK (default)
1	ASK

**Table 6-7.** Effect of the Configuration Word Sleep

Sleep					Start Value for Sleep Counter ( $T_{\text{Sleep}} = \text{Sleep} \times X_{\text{Sleep}} \times 1024 \times T_{\text{Cik}}$ )
Sleep4	Sleep3	Sleep2	Sleep1	Sleep0	
0	0	0	0	0	0 (Receiver is continuously polling until a valid signal occurs)
0	0	0	0	1	1 ( $T_{\text{Sleep}} \approx 2 \text{ ms}$ for $X_{\text{Sleep}} = 1$ in US-/European applications)
0	0	0	1	0	2
0	0	0	1	1	3
...	...	...	...	...	...
0	0	1	1	0	6 (USA: $T_{\text{Sleep}} = 12.52 \text{ ms}$ , Europe: $T_{\text{Sleep}} = 12.72 \text{ ms}$ ) (default)
...	...	...	...	...	...
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31 (Permanent sleep mode)

**Table 6-8.** Effect of the Configuration Bit  $X_{\text{Sleep}}$

$X_{\text{Sleep}}$	Extension Factor for Sleep Time ( $T_{\text{Sleep}} = \text{Sleep} \times X_{\text{Sleep}} \times 1024 \times T_{\text{Cik}}$ )
$X_{\text{SleepStd}}$	
0	1 (default)
1	8

**Table 6-9.** Effect of the Configuration Bit Noise Suppression

Noise Suppression	Suppression of the Digital Noise at Pin DATA
Noise_Disable	
0	Noise suppression is inactive
1	Noise suppression is active (default)

**Table 6-10.** Effect of the Configuration Word Lim\_min

Lim_min <sup>(1)</sup> (Lim_min < 10 Is Not Applicable)						Lower Limit Value for Bit Check
Lim_min5	Lim_min4	Lim_min3	Lim_min2	Lim_min1	Lim_min0	( $T_{Lim\_min} = Lim\_min \times Lim \times T_{Clk}$ )
0	0	1	0	1	0	10
0	0	1	0	1	1	11
0	0	1	1	0	0	12
...	...	...	...	...	...	
0	1	0	1	0	1	21 (default) USA: $T_{Lim\_min} = 342 \mu s$ , Europe: $T_{Lim\_min} = 348 \mu s$ )
...	...	...	...	...	...	
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Note: 1. Lim\_min is also used to determine the margins of the data clock control logic (see section “Data Clock” on page 19).

**Table 6-11.** Effect of the Configuration Word Lim\_max

Lim_max <sup>(1)</sup> (Lim_max < 12 Is Not Applicable)						Upper Limit Value for Bit Check
Lim_max 5	Lim_max 4	Lim_max 3	Lim_max 2	Lim_max 1	Lim_max 0	( $T_{Lim\_max} = (Lim\_max - 1) \times XLim \times T_{Clk}$ )
0	0	1	1	0	0	12
0	0	1	1	0	1	13
0	0	1	1	1	0	14
...	...	...	...	...	...	
1	0	1	0	0	1	41 (default) USA: $T_{Lim\_max} = 652 \mu s$ , Europe: $T_{Lim\_max} = 662 \mu s$ )
...	...	...	...	...	...	
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Note: 1. Lim\_max is also used to determine the margins of the data clock control logic (see section “Data Clock” on page 19).

### 6.6.1 Conservation of the Register Information

The ATA5743 has integrated power-on reset and brown-out detection circuitry to provide a mechanism to preserve the RAM register information.

As seen in Figure 6-24 on page 28, a power-on reset (POR) is generated if the supply voltage  $V_S$  drops below the threshold voltage  $V_{ThReset}$ . The default parameters are programmed into the configuration registers in that condition. Once  $V_S$  exceeds  $V_{ThReset}$  the POR is cancelled after the minimum reset period  $t_{Rst}$ . A POR is also generated when the supply voltage of the receiver is turned on.

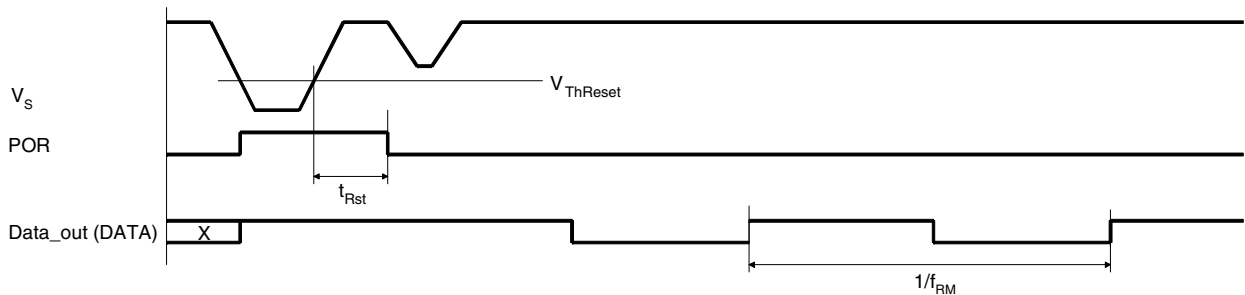
To indicate that condition, the receiver displays a reset marker (RM) at pin DATA after a reset. The RM is represented by the fixed frequency  $f_{RM}$  at a 50% duty-cycle. RM can be cancelled via a Low pulse  $t_1$  at pin DATA.

The RM implies the following characteristics:

- $f_{RM}$  is lower than the lowest feasible frequency of a data signal. By this means, RM cannot be misinterpreted by the connected microcontroller.
- If the receiver is set back to polling mode via pin DATA, RM cannot be cancelled by accident if  $t_1$  is applied according to the proposal in the section “[Programming the Configuration Register](#)” on page 28.

By means of that mechanism the receiver cannot lose its register information without communicating that condition via the reset marker RM.

**Figure 6-24.** Generation of the Power-on Reset



## 6.6.2 Programming the Configuration Register

**Figure 6-25.** Timing of the Register Programming

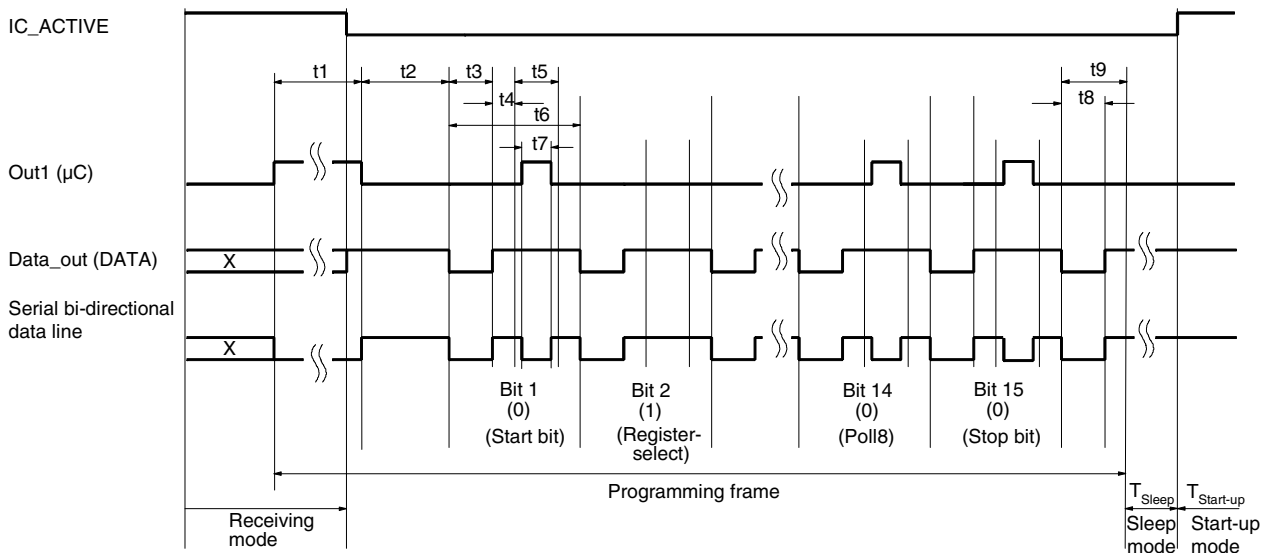
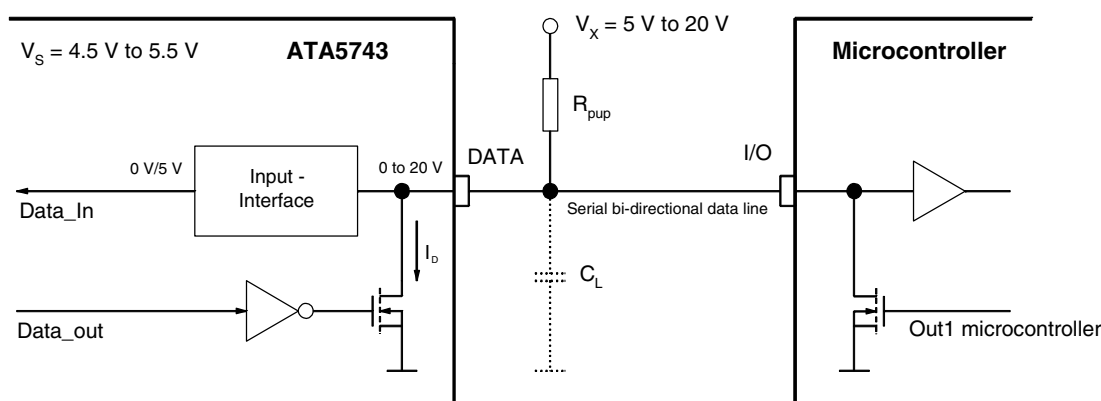


Figure 6-26. Data Interface



The configuration registers are programmed serially via the bi-directional data line as demonstrated in [Figure 6-25 on page 28](#) and [Figure 6-26](#).

To start programming, the microcontroller pulls the serial data line DATA to Low for the time period  $t_1$ . When DATA has been released, the receiver becomes the master device. When the programming delay period  $t_2$  has elapsed, it emits 15 subsequent synchronization pulses with the pulse length  $t_3$ . After each of these pulses, a programming window occurs. The delay until the program window starts is determined by  $t_4$ , the duration is defined by  $t_5$ . Within the programming window, the individual bits are set. If the microcontroller pulls down pin DATA for the time period  $t_7$  during  $t_5$ , the appropriate bit is set to "0". If no programming pulse  $t_7$  is issued, this bit is set to "1". All 15 bits are subsequently programmed this way. The time frame to program a bit is defined by  $t_6$ .

Bit 15 is followed by the equivalent time window  $t_9$ . During this window, the equivalent acknowledge pulse  $t_8$  (E\_Ack) occurs if the just programmed mode word is equivalent to the mode word that was already stored in that register. E\_Ack should be used to verify that the mode word was correctly transferred to the register; in order to do this, the register must be programmed twice.

Programming of a register is possible with the receiver in either sleep mode or in active mode.

During programming, the LNA, LO, low-pass filter IF-amplifier, and the FSK/ASK Manchester demodulator are disabled.

The programming start pulse  $t_1$  initiates the programming of the configuration registers. If bit 1 is set to "1", it represents the OFF command to set the receiver back to polling mode immediately. For the length of the programming start pulse  $t_1$ , the following convention should be considered:

- $t_1(\text{min}) < t_1 < 5632 \times T_{\text{Clk}}$ :  $t_1(\text{min})$  is the minimum specified value for the relevant BR\_Range

Similarly, programming the OFF command is initiated if the receiver is not in reset mode. If the receiver is in reset mode, programming the OFF command is not initiated and the reset marker (RM) is still present at pin DATA.

This period is generally used to switch the receiver to polling mode or to start the programming of a register. In reset condition, RM can not be cancelled by accident.

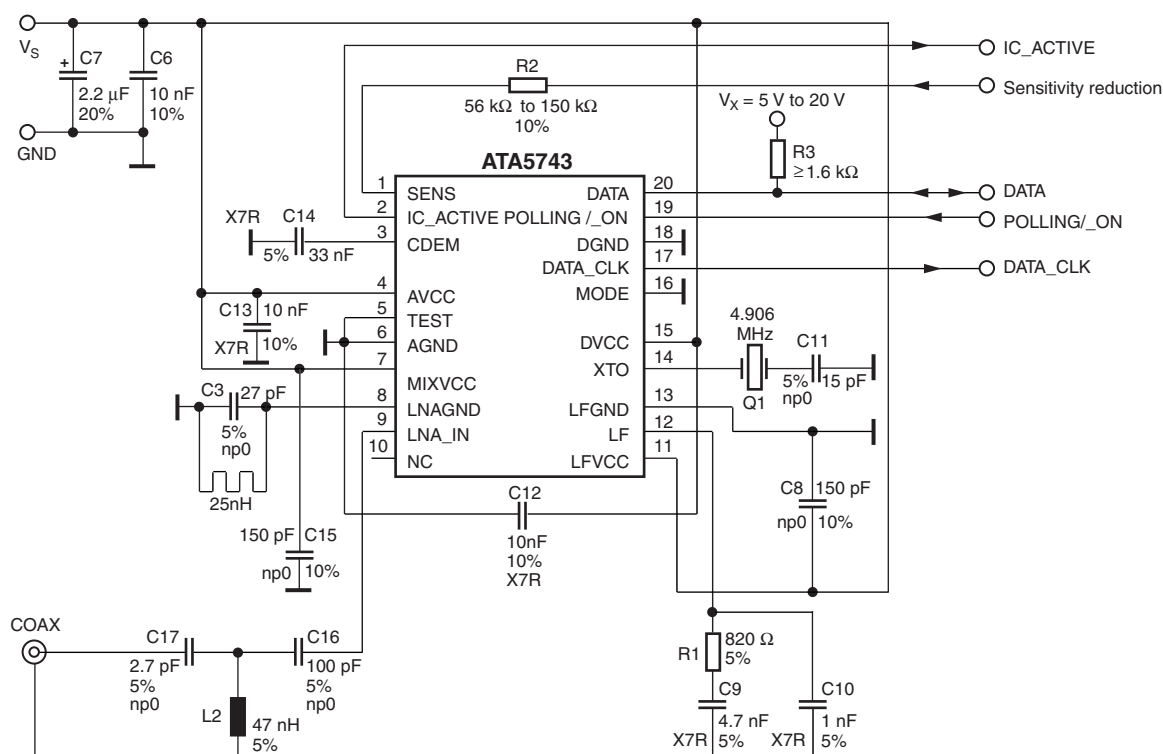
- $t_1 > 7936 \times T_{\text{Clk}}$

Programming registers or the OFF command is initiated in any case. The registers OPMODE and LIMIT are set to the default values. RM is cancelled if present.

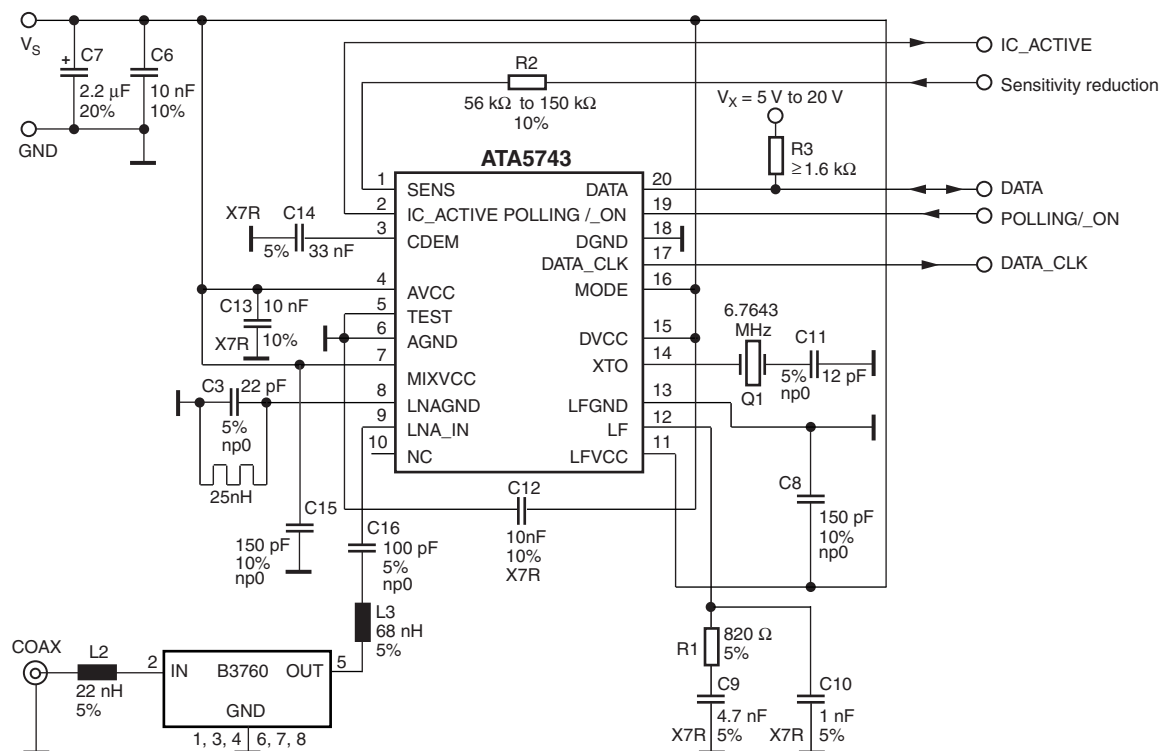


Note that the capacitive load at pin DATA is limited.

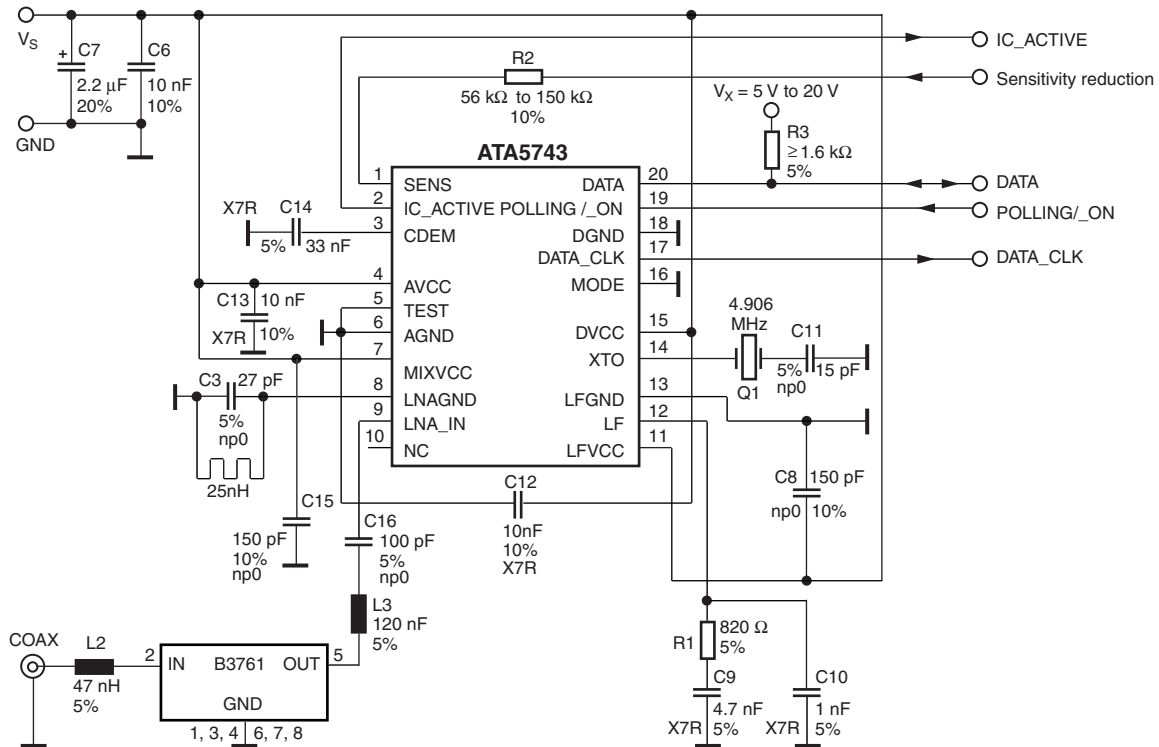
**Figure 6-28.** Application Circuit:  $f_{RF} = 315$  MHz without SAW Filter



**Figure 6-29.** Application Circuit:  $f_{RF} = 433.92$  MHz with SAW Filter



**Figure 6-30.** Application Circuit:  $f_{RF} = 315 \text{ MHz}$  with SAW Filter



## 7. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	$V_S$		6	V
Power dissipation	$P_{tot}$		1000	mW
Junction temperature	$T_j$		150	°C
Storage temperature	$T_{stg}$	-55	+125	°C
Ambient temperature	$T_{amb}$	-40	+105	°C
Maximum input level, input matched to 50Ω	$P_{in\_max}$		10	dBm

## 8. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	$R_{thJA}$	100	K/W

## 9. Electrical Characteristics

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{V}$  to  $5.5\text{V}$ ,  $f_0 = 433.92\text{ MHz}$  and  $f_0 = 315\text{ MHz}$ , unless otherwise specified.  
(For typical values:  $V_S = 5\text{V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

Parameter	Test Conditions	Symbol	6.76438 MHz Osc. (MODE: 1)			4.90625 MHz Osc. (MODE: 0)			Variable Oscillator			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Basic Clock Cycle of the Digital Circuitry												
Basic clock cycle	MODE = 0 (USA) MODE = 1 (Europe)	T <sub>Clk</sub>	2.0697		2.0697	2.0383		2.0383	1/f <sub>XTO</sub> /10 1/f <sub>XTO</sub> /14		1/f <sub>XTO</sub> /10 1/f <sub>XTO</sub> /14	μs μs
Extended basic clock cycle	BR_Range0	T <sub>XClk</sub>	16.6		16.6	16.3		16.3	8 × T <sub>Clk</sub>		8 × T <sub>Clk</sub>	μs
	BR_Range1		8.3		8.3	8.2		8.2	4 × T <sub>Clk</sub>		4 × T <sub>Clk</sub>	μs
	BR_Range2		4.1		4.1	4.1		4.1	2 × T <sub>Clk</sub>		2 × T <sub>Clk</sub>	μs
	BR_Range3		2.1		2.1	2.0		2.0	1 × T <sub>Clk</sub>		1 × T <sub>Clk</sub>	μs
Polling Mode												
Sleep time (see Figure 6-2, Figure 6-11, and Figure 6-25)	Sleep and X <sub>Sleep</sub> are defined in the OPMODE register	T <sub>Sleep</sub>	Sleep × X <sub>Sleep</sub> × 1024 × 2.0697		Sleep × X <sub>Sleep</sub> × 1024 × 2.0697	Sleep × X <sub>Sleep</sub> × 1024 × 2.0383		Sleep × X <sub>Sleep</sub> × 1024 × 2.0383	Sleep × X <sub>Sleep</sub> × 1024 × T <sub>Clk</sub>		Sleep × X <sub>Sleep</sub> × 1024 × T <sub>Clk</sub>	ms
Start-up time (see Figure 6-2 and Figure 6-3)	BR_Range0	T <sub>Startup</sub>	1855		1855	1827		1827	896.5		896.5	μs
	BR_Range1		1061		1061	1045		1045	512.5		512.5	μs
	BR_Range2		1061		1061	1045		1045	512.5		512.5	μs
	BR_Range3		663		663	653		653	320.5 × T <sub>Clk</sub>		320.5 × T <sub>Clk</sub>	μs
Time for bit check (see Figure 6-2)	Average bit-check time while polling, no RF applied (see Figure 6-6, and Figure 6-7)	T <sub>Bit-check</sub>										
	BR_Range0			0.45			0.45					ms
	BR_Range1			0.24			0.24					ms
	BR_Range2			0.14			0.14					ms
	BR_Range3		0.08			0.08					ms	
	Bit-check time for a valid input signal f <sub>Sig</sub> , (see Figure 6-3)	T <sub>Bit-check</sub>										
	N <sub>Bit-check</sub> = 0								1 × T <sub>XClk</sub>		1 × T <sub>Clk</sub>	ms
	N <sub>Bit-check</sub> = 3		3/f <sub>Sig</sub>		3.5/f <sub>Sig</sub>	3/f <sub>Sig</sub>		3.5/f <sub>Sig</sub>	3/f <sub>Sig</sub>		3.5/f <sub>Sig</sub>	ms
	N <sub>Bit-check</sub> = 6		6/f <sub>Sig</sub>		6.5/f <sub>Sig</sub>	6/f <sub>Sig</sub>		6.5/f <sub>Sig</sub>	6/f <sub>Sig</sub>		6.5/f <sub>Sig</sub>	ms
	N <sub>Bit-check</sub> = 9		9/f <sub>Sig</sub>		9.5/f <sub>Sig</sub>	9/f <sub>Sig</sub>		9.5/f <sub>Sig</sub>	9/f <sub>Sig</sub>		9.5/f <sub>Sig</sub>	ms
Receiving Mode												
Intermediate frequency	MODE = 0 (USA) MODE = 1 (Europe)	f <sub>IF</sub>		1.0			1.0		f <sub>XTO</sub> × 64/314 f <sub>XTO</sub> × 64/432.92			MHz MHz
Baud-rate range	BR_Range0	BR_Range	1.0		1.8	1.0		1.8	BR_Range0 × 2 μs/T <sub>Clk</sub>			kBaud
	BR_Range1		1.8		3.2	1.8		3.2	BR_Range1 × 2 μs/T <sub>Clk</sub>			kBaud
	BR_Range2		3.2		5.6	3.2		5.6	BR_Range2 × 2 μs/T <sub>Clk</sub>			kBaud
	BR_Range3		5.6		10.0	5.6		10.0	BR_Range3 × 2 μs/T <sub>Clk</sub>			kBaud
Minimum time period between edges at pin DATA (see Figure 5-1, Figure 6-9 and Figure 6-10, with the exception of parameter T <sub>Pulse</sub> )	BR_Range =	t <sub>DATA-min</sub>										
	BR_Range0		165		165	163		163	10 × T <sub>XClk</sub>		10 × T <sub>XClk</sub>	μs
	BR_Range1		83		83	81		81	10 × T <sub>XClk</sub>		10 × T <sub>XClk</sub>	μs
	BR_Range2		41.4		41.4	40.7		40.7	10 × T <sub>XClk</sub>		10 × T <sub>XClk</sub>	μs
	BR_Range3		20.7		20.7	20.4		20.4	10 × T <sub>XClk</sub>		10 × T <sub>XClk</sub>	μs



## 9. Electrical Characteristics (Continued)

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{V}$  to  $5.5\text{V}$ ,  $f_0 = 433.92\text{ MHz}$  and  $f_0 = 315\text{ MHz}$ , unless otherwise specified.  
(For typical values:  $V_S = 5\text{V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

Parameter	Test Conditions	Symbol	6.76438 MHz Osc. (MODE: 1)			4.90625 MHz Osc. (MODE: 0)			Variable Oscillator			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Maximum Low period at pin DATA (see Figure 5-1 and Figure 6-10)	BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3	$t_{\text{DATA\_L\_max}}$	2152 1076 538 270		2152 1076 538 270	2120 1060 530 265		2120 1060 530 265	$130 \times T_{\text{Clk}}$ $130 \times T_{\text{Clk}}$ $130 \times T_{\text{Clk}}$ $130 \times T_{\text{Clk}}$		$130 \times T_{\text{Clk}}$ $130 \times T_{\text{Clk}}$ $130 \times T_{\text{Clk}}$ $130 \times T_{\text{Clk}}$	$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$
Delay to activate the start-up mode (see Figure 6-13)		$T_{\text{on1}}$	19.7		21.8	19.4		21.5	$9.5 \times T_{\text{Clk}}$		$10.5 \times T_{\text{Clk}}$	$\mu\text{s}$
OFF command at pin POLLING/_ON (see Figure 6-12)		$T_{\text{on2}}$	16.6			16.4			$8 \times T_{\text{Clk}}$			$\mu\text{s}$
Delay to activate the sleep mode (see Figure 6-12)		$T_{\text{on3}}$	17.6		19.7	17.4		19.4	$8.5 \times T_{\text{Clk}}$		$9.5 \times T_{\text{Clk}}$	$\mu\text{s}$
Pulse on pin DATA at the end of a data stream (see Figure 6-22)	BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3	$T_{\text{Pulse}}$	16.6 8.3 4.1 2.1		16.6 8.3 4.1 2.1	16.3 8.2 4.1 2.0		16.3 8.2 4.1 2.0	$8 \times T_{\text{Clk}}$ $4 \times T_{\text{Clk}}$ $2 \times T_{\text{Clk}}$ $1 \times T_{\text{Clk}}$		$8 \times T_{\text{Clk}}$ $4 \times T_{\text{Clk}}$ $2 \times T_{\text{Clk}}$ $1 \times T_{\text{Clk}}$	$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$
<b>Configuration of the Receiver</b>												
Frequency of the reset marker	(see Figure 6-23)	$f_{\text{RM}}$	117.9		117.9	119.8		119.8	$\frac{1}{4096 \times T_{\text{Clk}}}$		$\frac{1}{4096 \times T_{\text{Clk}}}$	Hz
Programming start pulse (see Figure 6-11 and Figure 6-25)	BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3 after POR	$t_1$	3367 2277 1735 1464 16.43		11650 11650 11650 11650 16.18	3311 2243 1709 1442 16.18		11470 11470 11470 11470 16.18	$1624 \times T_{\text{Clk}}$ $1100 \times T_{\text{Clk}}$ $838 \times T_{\text{Clk}}$ $707 \times T_{\text{Clk}}$ $7936 \times T_{\text{Clk}}$		$5632 \times T_{\text{Clk}}$ $5632 \times T_{\text{Clk}}$ $5632 \times T_{\text{Clk}}$ $5632 \times T_{\text{Clk}}$ $5632 \times T_{\text{Clk}}$	$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$
Programming delay period	(see Figure 6-11 and Figure 6-25)	$t_2$	795		798	783		786	$384.5 \times T_{\text{Clk}}$		$385.5 \times T_{\text{Clk}}$	$\mu\text{s}$
Synchronization pulse		$t_3$	265		265	261		261	$128 \times T_{\text{Clk}}$		$128 \times T_{\text{Clk}}$	$\mu\text{s}$
Delay until the programming window starts		$t_4$	131		131	129		129	$63.5 \times T_{\text{Clk}}$		$63.5 \times T_{\text{Clk}}$	$\mu\text{s}$
Programming window		$t_5$	530		530	522		522	$256 \times T_{\text{Clk}}$		$256 \times T_{\text{Clk}}$	$\mu\text{s}$

## 9. Electrical Characteristics (Continued)

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{V}$  to  $5.5\text{V}$ ,  $f_0 = 433.92\text{ MHz}$  and  $f_0 = 315\text{ MHz}$ , unless otherwise specified.  
(For typical values:  $V_S = 5\text{V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

Parameter	Test Conditions	Symbol	6.76438 MHz Osc. (MODE: 1)			4.90625 MHz Osc. (MODE: 0)			Variable Oscillator			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Time frame of a bit (see Figure 6-25)		t6	1060		1060	1044		1044	$512 \times T_{Clk}$		$512 \times T_{Clk}$	$\mu\text{s}$
Programming pulse (see Figure 6-11 and Figure 6-25)		t7	132		529	130		521	$64 \times T_{Clk}$		$256 \times T_{Clk}$	$\mu\text{s}$
Equivalent acknowledge pulse: E_Ack (see Figure 6-25)		t8	265		265	261		261	$128 \times T_{Clk}$		$128 \times T_{Clk}$	$\mu\text{s}$
Equivalent time window (see Figure 6-25)		t9	534		534	526		526	$258 \times T_{Clk}$		$258 \times T_{Clk}$	$\mu\text{s}$
OFF bit programming window (see Figure 6-11)		t10	930		930	916		916	$449.5 \times T_{Clk}$		$449.5 \times T_{Clk}$	$\mu\text{s}$
<b>Data Clock</b>												
Minimum delay time between edge at DATA and DATA_CLK (see Figure 6-18 and Figure 6-19)	BR_Range =	t <sub>Delay2</sub>										
	BR_Range0		0		16.6	0		16.3	0		$1 \times T_{XClk}$	$\mu\text{s}$
	BR_Range1		0		8.3	0		8.2	0		$1 \times T_{XClk}$	$\mu\text{s}$
	BR_Range2		0		4.15	0		4.08	0		$1 \times T_{XClk}$	$\mu\text{s}$
Pulse width of negative pulse at pin DATA_CLK (see Figure 6-18 and Figure 6-19)	BR_Range =	t <sub>P_DATA_CLK</sub>										
	BR_Range0		66.2		66.2	65.2		65.2	$4 \times T_{XClk}$		$4 \times T_{XClk}$	$\mu\text{s}$
	BR_Range1		33.1		33.1	32.6		32.6	$4 \times T_{XClk}$		$4 \times T_{XClk}$	$\mu\text{s}$
	BR_Range2		16.56		16.56	16.3		16.3	$4 \times T_{XClk}$		$4 \times T_{XClk}$	$\mu\text{s}$
	BR_Range3		8.3		8.3	8.2		8.2	$4 \times T_{XClk}$		$4 \times T_{XClk}$	$\mu\text{s}$

## 9. Electrical Characteristics (Continued)

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{V}$  to  $5.5\text{V}$ ,  $f_0 = 433.92\text{ MHz}$  and  $f_0 = 315\text{ MHz}$ , unless otherwise specified.  
(For typical values:  $V_S = 5\text{V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Current consumption	Sleep mode (XTO and polling logic active)	$I_{S_{off}}$		170	276	$\mu\text{A}$
	IC active (start-up-, bit check-, receiving mode) pin DATA = H FSK ASK	$I_{S_{on}}$		7.5 7.1	9.1 8.7	mA mA
<b>LNA Mixer (Input Matched According to Figure 4-3)</b>						
Third-order intercept point	LNA/mixer/IF amplifier	IIP3		-28		dBm
LO spurious emission at $RF_{in}$	Required according to I-ETS 300220	$IS_{LORF}$		-73	-57	dBm
Noise figure LNA and mixer (DSB)		NF		7		dB
LNA_IN input impedance	at 433.92 MHz at 315 MHz	$Z_{i_{LNA\_IN}}$		1.0    1.56 1.3    1.0		$k\Omega    pF$ $k\Omega    pF$
1 dB compression point (LNA, mixer, IF amplifier)	Referred to $RF_{in}$	$IP_{1db}$		-40		dBm
Maximum input level	$BER \leq 10^{-3}$ FSK mode ASK mode	$P_{in\_max}$			-22 -20	dBm dBm
<b>Local Oscillator</b>						
Operating frequency range VCO		$f_{VCO}$	299		449	MHz
Phase noise VCO/LO	$f_{osc} = 432.92\text{ MHz}$ At 1 MHz At 10 MHz	$L(fm)$		-93 -113	-90 -110	dBc/Hz dBc/Hz
Spurs of the VCO	At $\pm f_{XTO}$			-55	-47	dBc
VCO gain		$K_{VCO}$		190		MHz/V
Loop bandwidth of the PLL	For best LO noise (design parameter) $R1 = 820\Omega$ $C9 = 4.7\text{ nF}$ $C10 = 1\text{ nF}$	$B_{Loop}$		100		kHz
Capacitive load at pin LF	The capacitive load at pin LF is limited if bit check is used. The limitation therefore also applies to self-polling.	$C_{LF\_tot}$			10	nF
XTO operating frequency	XTO crystal frequency appropriate load capacitance must be connected to XTAL $f_{XTAL} = 6.764375\text{ MHz (EU)}$ $f_{XTAL} = 4.90625\text{ MHz (US)}$	$f_{XTO}$	-30 ppm	$f_{XTAL}$	+30 ppm	MHz
Series resonance resistor of the crystal	$f_{XTO} = 6.764\text{ MHz}$ $f_{XTO} = 4.906\text{ MHz}$	$R_S$			150 220	$\Omega$ $\Omega$
Static capacitance at pin XTO to GND		$C_0$			6.5	pF

## 9. Electrical Characteristics (Continued)

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{V}$  to  $5.5\text{V}$ ,  $f_0 = 433.92\text{ MHz}$  and  $f_0 = 315\text{ MHz}$ , unless otherwise specified.  
(For typical values:  $V_S = 5\text{V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
<b>Analog Signal Processing</b>						
Input sensitivity ASK 300 kHz IF-filter	Input matched according to <a href="#">Figure 4-3</a> ASK (level of carrier) $BER \leq 10^{-3}$ , $BW = 300\text{ kHz}$ $f_{in} = 433.92\text{ MHz}/315\text{ MHz}$ $V_S = 5\text{V}$ , $T_{amb} = 25^{\circ}\text{C}$ , $f_{IF} = 1\text{ MHz}$ BR_Range0 BR_Range1 BR_Range2 BR_Range3	$P_{Ref\_ASK}$	-109 -107 -106 -104	-111 -109 -108 -106	-113 -111 -110 -108	dBm dBm dBm dBm
Input sensitivity ASK 600 kHz IF-filter	Input matched according to <a href="#">Figure 4-3</a> ASK (level of carrier) $BER \leq 10^{-3}$ , $BW = 600\text{ kHz}$ $f_{in} = 433.92\text{ MHz}/315\text{ MHz}$ $V_S = 5\text{V}$ , $T_{amb} = 25^{\circ}\text{C}$ , $f_{IF} = 1\text{ MHz}$ BR_Range0 BR_Range1 BR_Range2 BR_Range3	$P_{Ref\_ASK}$	-108 -106.5 -106 -104	-110 -108.5 -108 -106	-112 -110.5 -110 -108	dBm dBm dBm dBm
Sensitivity variation ASK for the full operating range compared to $T_{amb} = 25^{\circ}\text{C}$ , $V_S = 5\text{V}$	300 kHz and 600 kHz version $f_{in} = 433.92\text{ MHz}/315\text{ MHz}$ $f_{IF} = 1\text{ MHz}$ , $P_{ASK} = P_{Ref\_ASK} + \Delta P_{Ref}$	$\Delta P_{Ref}$	+2.5		-1.5	dB
Sensitivity variation ASK for full operating range including IF-filter compared to $T_{amb} = 25^{\circ}\text{C}$ , $V_S = 5\text{V}$	300 kHz version $f_{in} = 433.92\text{ MHz}/315\text{ MHz}$ $f_{IF} = 0.89\text{ MHz}$ to $1.11\text{ MHz}$ $f_{IF} = 0.86\text{ MHz}$ to $1.14\text{ MHz}$ $P_{ASK} = P_{Ref\_ASK} + \Delta P_{Ref}$	$\Delta P_{Ref}$	+5.5 +7.5		-1.5 -1.5	dB dB
	600 kHz version $f_{in} = 433.92\text{ MHz}/315\text{ MHz}$ $f_{IF} = 0.79\text{ MHz}$ to $1.21\text{ MHz}$ $f_{IF} = 0.73\text{ MHz}$ to $1.27\text{ MHz}$ $P_{ASK} = P_{Ref\_ASK} + \Delta P_{Ref}$	$\Delta P_{Ref}$	+5.5 +7.5		-1.5 -1.5	dB dB

## 9. Electrical Characteristics (Continued)

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{V}$  to  $5.5\text{V}$ ,  $f_0 = 433.92\text{ MHz}$  and  $f_0 = 315\text{ MHz}$ , unless otherwise specified.  
(For typical values:  $V_S = 5\text{V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Input sensitivity FSK 300 kHz IF-filter	Input matched according to <a href="#">Figure 4-3</a> $\text{BER} \leq 10^{-3}$ , $\text{BW} = 300\text{ kHz}$ $f_{in} = 433.92\text{ MHz}/315\text{ MHz}$ $V_S = 5\text{V}$ , $T_{amb} = 25^{\circ}\text{C}$ $f_{IF} = 1\text{ MHz}$					
	BR_Range0 $df = \pm 16\text{ kHz}$ $df = \pm 10\text{ kHz}$ to $\pm 30\text{ kHz}$	$P_{\text{Ref\_FSK}}$	-101 -99	-104	-105.5 -105.5	dBm dBm
	BR_Range1 $df = \pm 16\text{ kHz}$ $df = \pm 10\text{ kHz}$ to $\pm 30\text{ kHz}$	$P_{\text{Ref\_FSK}}$	-99 -97	-102	-103.5 -103.5	dBm dBm
	BR_Range2 $df = \pm 16\text{ kHz}$ $df = \pm 10\text{ kHz}$ to $\pm 30\text{ kHz}$	$P_{\text{Ref\_FSK}}$	-97.5 -95.5	-100.5	-102 -102	dBm dBm
	BR_Range3 $df = \pm 16\text{ kHz}$ $df = \pm 10\text{ kHz}$ to $\pm 30\text{ kHz}$	$P_{\text{Ref\_FSK}}$	-95.5 -93.5	-98.5	-100 -100	dBm dBm
Input sensitivity FSK 600 kHz IF-filter	Input matched according to <a href="#">Figure 4-3</a> $\text{BER} \leq 10^{-3}$ , $\text{BW} = 600\text{ kHz}$ $f_{in} = 433.92\text{ MHz}/315\text{ MHz}$ $V_S = 5\text{V}$ , $T_{amb} = 25^{\circ}\text{C}$ $f_{IF} = 1\text{ MHz}$					
	BR_Range0 $df = \pm 16\text{ kHz}$ $df = \pm 10\text{ kHz}$ to $\pm 100\text{ kHz}$	$P_{\text{Ref\_FSK}}$	-101 -99	-104	-105.5 -105.5	dBm dBm
	BR_Range1 $df = \pm 16\text{ kHz}$ $df = \pm 10\text{ kHz}$ to $\pm 100\text{ kHz}$	$P_{\text{Ref\_FSK}}$	-99 -97	-102	-103.5 -103.5	dBm dBm
	BR_Range2 $df = \pm 16\text{ kHz}$ $df = \pm 10\text{ kHz}$ to $\pm 100\text{ kHz}$	$P_{\text{Ref\_FSK}}$	-97.5 -95.5	-100.5	-102 -102	dBm dBm
	BR_Range3 $df = \pm 16\text{ kHz}$ $df = \pm 10\text{ kHz}$ to $\pm 100\text{ kHz}$	$P_{\text{Ref\_FSK}}$	-95.5 -93.5	-98.5	-100 -100	dBm dBm
Sensitivity variation FSK for the full operating range compared to $T_{amb} = 25^{\circ}\text{C}$ , $V_S = 5\text{V}$	300 kHz and 600 kHz version $f_{in} = 433.92\text{ MHz}/315\text{ MHz}$ $f_{IF} = 1\text{ MHz}$ $P_{\text{FSK}} = P_{\text{Ref\_FSK}} + \Delta P_{\text{Ref}}$	$\Delta P_{\text{Ref}}$	+3		-1.5	dB

## 9. Electrical Characteristics (Continued)

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{V}$  to  $5.5\text{V}$ ,  $f_0 = 433.92\text{ MHz}$  and  $f_0 = 315\text{ MHz}$ , unless otherwise specified.  
(For typical values:  $V_S = 5\text{V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Sensitivity variation FSK for the full operating range including IF-filter compared to $T_{amb} = 25^{\circ}\text{C}$ , $V_S = 5\text{V}$	300 kHz version $f_{in} = 433.92\text{ MHz}/315\text{ MHz}$ $f_{IF} = 0.89\text{ MHz}$ to $1.11\text{ MHz}$ $f_{IF} = 0.86\text{ MHz}$ to $1.14\text{ MHz}$ $f_{IF} = 0.82\text{ MHz}$ to $1.18\text{ MHz}$ $P_{FSK} = P_{Ref\_FSK} + \Delta P_{Ref}$	$\Delta P_{Ref}$	+6 +8 +11		-2 -2 -2	dB dB dB
	600 kHz version $f_{in} = 433.92\text{ MHz}/315\text{ MHz}$ $f_{IF} = 0.85\text{ MHz}$ to $1.15\text{ MHz}$ $f_{IF} = 0.80\text{ MHz}$ to $1.20\text{ MHz}$ $f_{IF} = 0.74\text{ MHz}$ to $1.26\text{ MHz}$ $P_{FSK} = P_{Ref\_FSK} + \Delta P_{Ref}$	$\Delta P_{Ref}$	+6 +8 +11		-2 -2 -2	dB dB dB
SNR to suppress inband noise signals. Noise signals may have any modulation scheme	ASK mode FSK mode	$SNR_{ASK}$ $SNR_{FSK}$			12 3	dB dB
Dynamic range RSSI ampl.		$DR_{RSSI}$		60		dB
Lower cut-off frequency of the data filter	$CDEM = 33\text{ nF}$ $f_{cu\_DF} = \frac{1}{2 \times \pi \times 30\text{ k}\Omega \times CDEM}$	$f_{cu\_DF}$	0.11	0.16	0.20	kHz
Recommended CDEM for best performance	BR_Range0 (default) BR_Range1 BR_Range2 BR_Range3	CDEM		39 22 12 8.2		nF nF nF nF
Edge-to-edge time period of the input data signal for full sensitivity	BR_Range0 (default) BR_Range1 BR_Range2 BR_Range3	$t_{ee\_sig}$	270 156 89 50		1000 560 320 180	$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$
Upper cut-off frequency data filter	Upper cut-off frequency programmable in 4 ranges via a serial mode word BR_Range0 (default) BR_Range1 BR_Range2 BR_Range3	$f_u$	2.8 4.8 8.0 15.0	3.4 6.0 10.0 19.0	4.0 7.2 12.0 23.0	kHz kHz kHz kHz
Reduced sensitivity	$R_{Sense}$ connected from pin SENS to $V_S$ , input matched according to <a href="#">Figure 4-3</a>					dBm (peak level)
	$R_{Sense} = 56\text{ k}\Omega$ , $f_{in} = 433.92\text{ MHz}$ , at BW = 300 kHz at BW = 600 kHz	$P_{Ref\_Red}$	-71 -67	-76 -72	-81 -77	dBm dBm
	$R_{Sense} = 100\text{ k}\Omega$ , $f_{in} = 433.92\text{ MHz}$ , at BW = 300 kHz at BW = 600 kHz		-80 -76	-85 -81	-90 -86	dBm dBm
	$R_{Sense} = 56\text{ k}\Omega$ , $f_{in} = 315\text{ MHz}$ , at BW = 300 kHz at BW = 600 kHz		-72 -68	-77 -73	-82 -78	dBm dBm
	$R_{Sense} = 100\text{ k}\Omega$ , $f_{in} = 315\text{ MHz}$ , at BW = 300 kHz at BW = 600 kHz		-81 -77	-86 -82	-91 -87	dBm dBm



## 9. Electrical Characteristics (Continued)

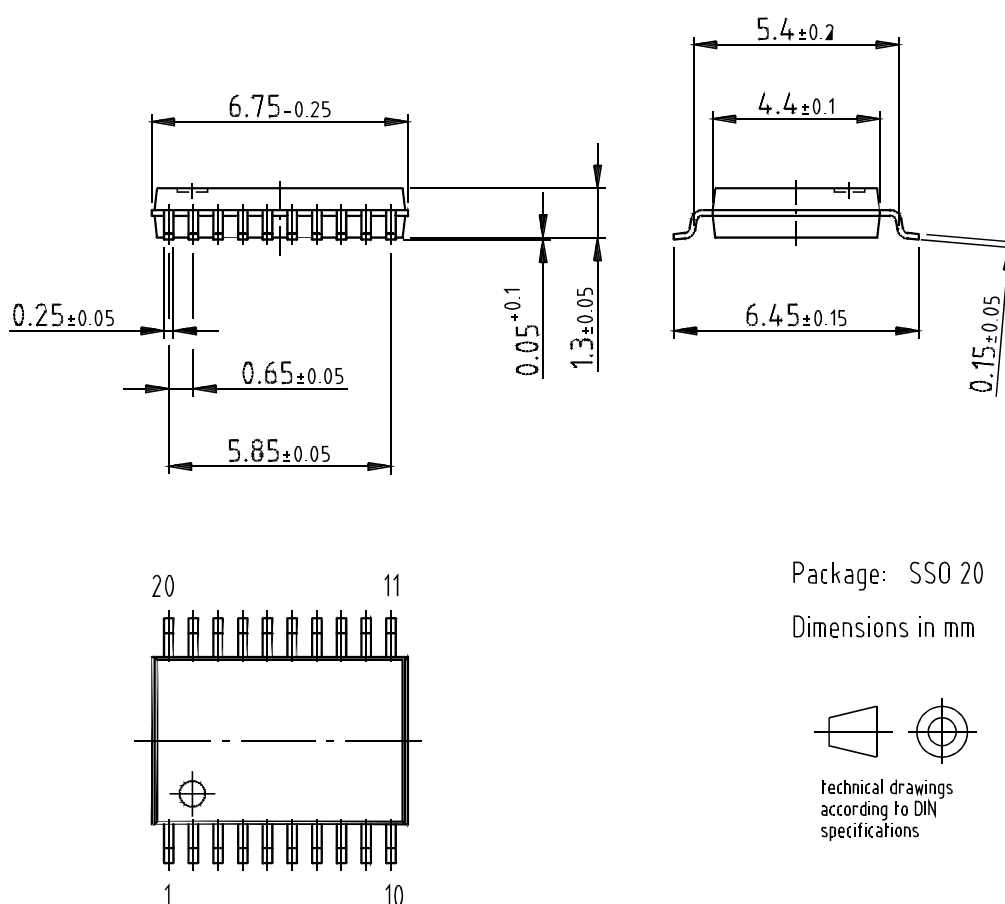
All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{V}$  to  $5.5\text{V}$ ,  $f_0 = 433.92\text{ MHz}$  and  $f_0 = 315\text{ MHz}$ , unless otherwise specified.  
(For typical values:  $V_S = 5\text{V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Reduced sensitivity variation over full operating range	$R_{Sense} = 56\text{ k}\Omega$ $R_{Sense} = 100\text{ k}\Omega$ $P_{Red} = P_{Ref\_Red} + \Delta P_{Red}$	$\Delta P_{Red}$	5 6	0 0	0 0	dB dB
Reduced sensitivity variation for different values of $R_{Sense}$	Values relative to $R_{Sense} = 56\text{ k}\Omega$  $R_{Sense} = 56\text{ k}\Omega$ $R_{Sense} = 68\text{ k}\Omega$ $R_{Sense} = 82\text{ k}\Omega$ $R_{Sense} = 100\text{ k}\Omega$ $R_{Sense} = 120\text{ k}\Omega$ $R_{Sense} = 150\text{ k}\Omega$ $P_{Red} = P_{Ref\_Red} + \Delta P_{Red}$	$\Delta P_{Red}$ $\Delta P_{Red}$ $\Delta P_{Red}$ $\Delta P_{Red}$ $\Delta P_{Red}$ $\Delta P_{Red}$	0 -3.5 -6.0 -9.0 -11.0 -13.5			dB dB dB dB dB dB
Threshold voltage for reset		$V_{ThRESET}$	1.95	2.8	3.75	V
<b>Digital Ports</b>						
Data output - Saturation voltage Low - maximum voltage at pin DATA - quiescent current - short-circuit current - ambient temperature in case of permanent short-circuit Data input - Input voltage Low - Input voltage High	$I_{ol} \leq 12\text{ mA}$ $I_{ol} = 2\text{ mA}$  $V_{oh} = 20\text{V}$ $V_{ol} = 0.8\text{V to } 20\text{V}$ $V_{oh} = 0\text{V to } 20\text{V}$	$V_{ol}$ $V_{ol}$ $V_{oh}$ $I_{qu}$ $I_{ol\_lim}$ $t_{amb\_sc}$  $V_{ll}$ $V_{ich}$		0.35 0.08  30	0.8 0.3 20 20 45 85	V V V $\mu\text{A}$ mA $^{\circ}\text{C}$  V V
DATA_CLK output - Saturation voltage Low - Saturation voltage High	IDATA_CLK = 1 mA IDATA_CLK = -1 mA	$V_{ol}$ $V_{oh}$	$V_S - 0.4\text{ V}$	0.1 $V_S - 0.15\text{ V}$	0.4	V V
IC_ACTIVE output - Saturation voltage Low - Saturation voltage High	IIC_ACTIVE = 1 mA IIC_ACTIVE = -1 mA	$V_{ol}$ $V_{oh}$	$V_S - 0.4\text{ V}$	0.1 $V_S - 0.15\text{ V}$	0.4	V V
POLLING/_ON input - Low level input voltage - High level input voltage	Receiving mode Polling mode	$V_{ll}$ $V_{lh}$	$0.8 \times V_S$		$0.2 \times V_S$	V V
MODE input - Low level input voltage - High level input voltage	Division factor = 10 Division factor = 14	$V_{ll}$ $V_{lh}$	$0.8 \times V_S$		$0.2 \times V_S$	V V
TEST input - Low level input voltage	Test input must always be set to Low	$V_{ll}$			$0.2 \times V_S$	V

## 10. Ordering Information

Extended Type Number	Package	Remarks
ATA5743P3-TKQY	SSO20	Taped and reeled, Pb-free, 300 kHz bandwidth
ATA5743P3-TKSY	SSO20	Tube, Pb-free, 300 kHz bandwidth
ATA5743P6-TKQY	SSO20	Taped and reeled, Pb-free, 600 kHz bandwidth
ATA5743P6-TKSY	SSO20	Tube, Pb-free, 600 kHz bandwidth
ATA5743P3-TGQY	SO20	Taped and reeled, Pb-free, 300 kHz bandwidth
ATA5743P3-TGSY	SO20	Tube, Pb-free, 300 kHz bandwidth
ATA5743P6-TGQY	SO20	Taped and reeled, Pb-free, 600 kHz bandwidth
ATA5743P6-TGSY	SO20	Tube, Pb-free, 600 kHz bandwidth

## 11. Package Information



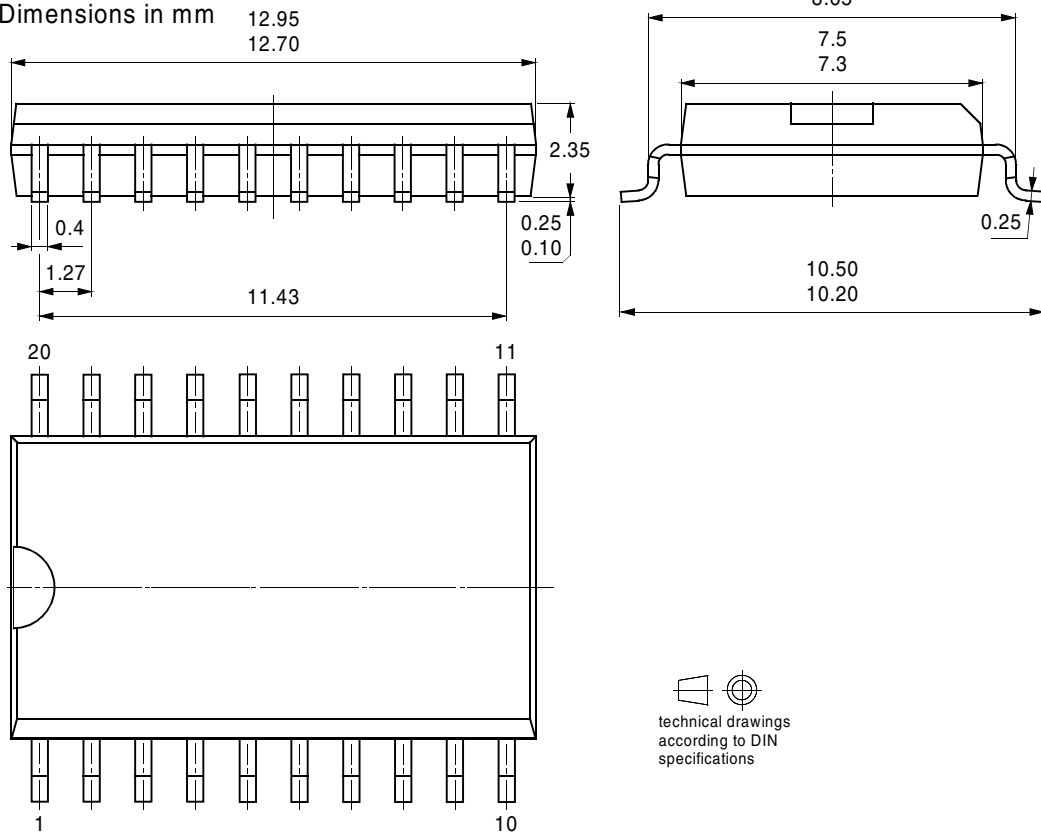
Drawing-No.: 6.543-5056.01-4

Issue: 1; 10.03.04



## Package SO20

Dimensions in mm



technical drawings  
according to DIN  
specifications

## 12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4839B-RKE-08/05	<ul style="list-style-type: none"> <li>Put datasheet in a new template</li> <li>First page: Pb-free logo added</li> <li>Page 41: Ordering Information changed</li> <li>Page 42: Drawing SO20 added</li> </ul>



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