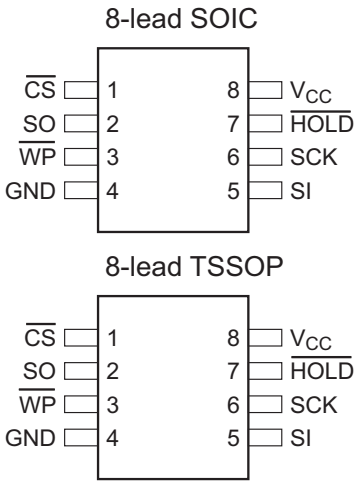
Figure 1. Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

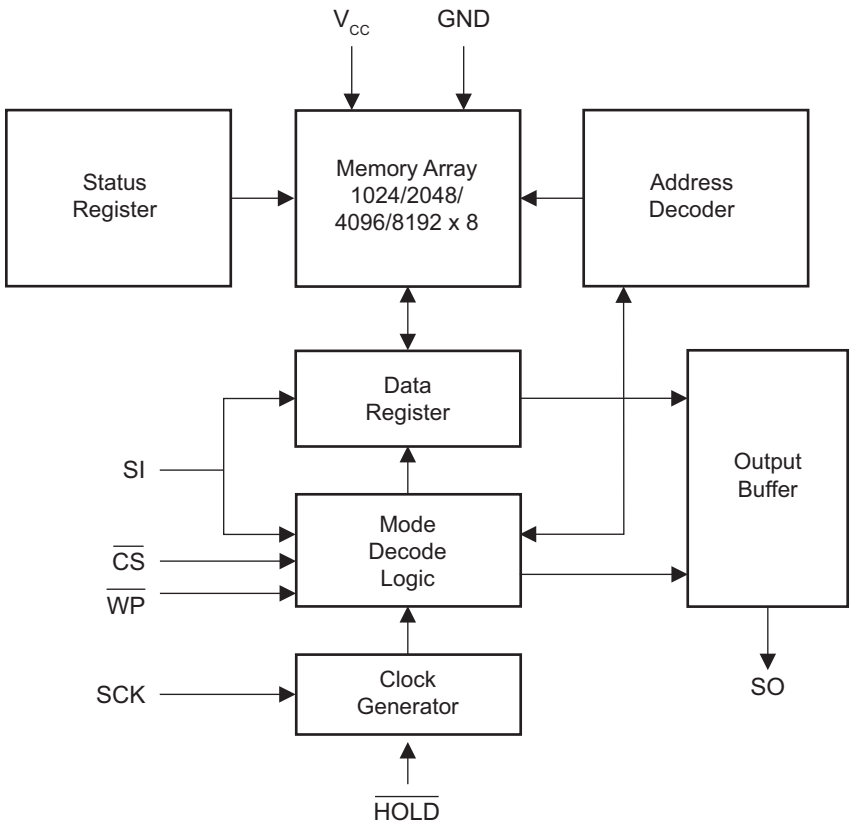


1. Absolute Maximum Ratings*

Operating Temperature	–40°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on any pin with respect to ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Block Diagram



3. Electrical Characteristics

3.1 Pin Capacitance[1]

Applicable at these conditions, unless otherwise noted. T_A = 25°C, f = 1.0MHz, V_{CC} = +5.0V.

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

3.2 DC Characteristics

Applicable over recommended operating range from: T_A = –40°C to +125°C, V_{CC} = +2.5V to +5.5V.

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			2.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V at 5MHz, SO = Open, Read				6.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V at 1MHz				3.0	mA
I_{CC3}	Supply Current	V_{CC} = 5.0V at 5MHz, SO = Open, Read, Write				7.0	mA
I_{SB1}	Standby Current	V_{CC} = 2.5V, $\overline{CS}$ = V_{CC}			0.2	10.0	µA
I_{SB2}	Standby Current	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}			2.0	13.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		–3.0			µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}		–3.0		3.0	µA
V_{IL}[1]	Input Low-voltage			–0.6		V_{CC} x 0.3	V
V_{IH}[1]	Input High-voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low-voltage	2.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 3.0mA			0.4	V
V_{OH1}	Output High-voltage		I_{OH} = –1.6mA	V_{CC} – 0.8			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

3.3 AC Characteristics

Applicable over recommended operating range from T_A = –40°C to +125°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	2.5–5.5	0	5.0	MHz
t_{RI}	Input Rise Time	2.5–5.5		2	µs
t_{FI}	Input Fall Time	2.5–5.5		2	µs
t_{WH}	SCK High Time	2.5–5.5	40		ns
t_{WL}	SCK Low Time	2.5–5.5	40		ns
t_{CS}	$\overline{CS}$ High Time	2.5–5.5	80		ns
t_{CSS}	$\overline{CS}$ Setup Time	2.5–5.5	80		ns
t_{CSH}	$\overline{CS}$ Hold Time	2.5–5.5	80		ns
t_{SU}	Data In Setup Time	2.5–5.5	5		ns
t_H	Data In Hold Time	2.5–5.5	20		ns
t_{HD}	$\overline{Hold}$ Setup Time	2.5–5.5	40		ns
t_{CD}	$\overline{Hold}$ Hold Time	2.5–5.5	40		ns
t_V	Output Valid	2.5–5.5	0	40	ns
t_{HO}	Output Hold Time	2.5–5.5	0		ns
t_{LZ}	$\overline{Hold}$ to Output Low Z	2.5–5.5	0	40	ns
t_{HZ}	$\overline{Hold}$ to Output High Z	2.5–5.5		80	ns
t_{DIS}	Output Disable Time	2.5–5.5		80	ns
t_{WC}	Write Cycle Time	2.5–5.5		5	ms
Endurance[1]	5.0V, 25°C, Page Mode		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

4. Serial Interface Description

Master: The device that generates the serial clock.

Slave: Because the Serial Clock pin (SCK) is always an input, AT25080B/160B/320B/640B always operates as a slave.

Transmitter/Receiver: AT25080B/160B/320B/640B has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

Serial Opcode: After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the opcode that defines the operations to be performed.

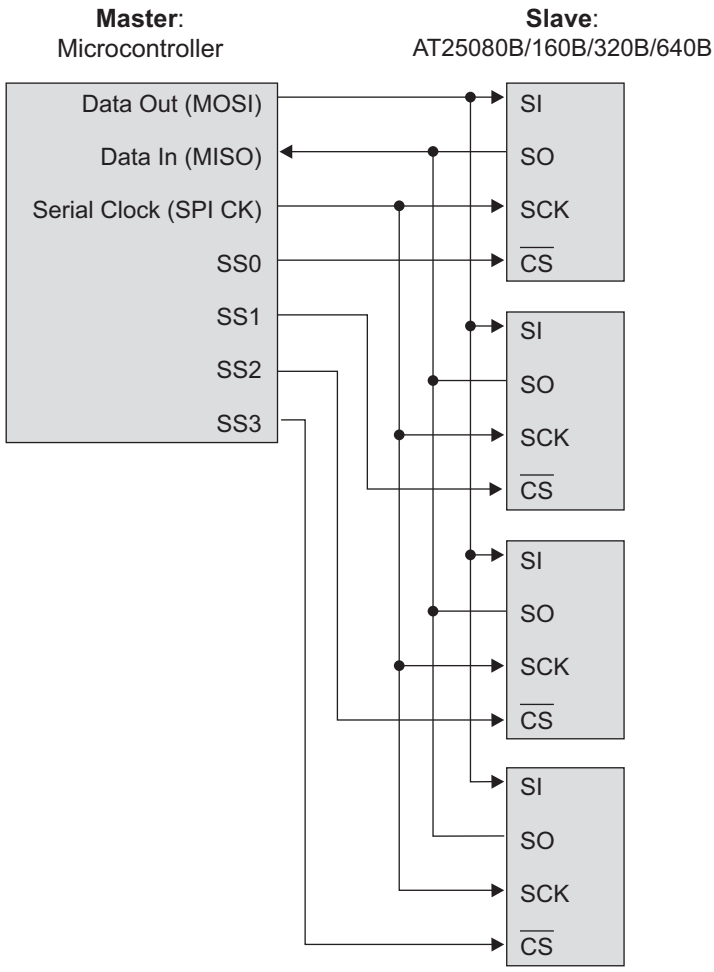
Invalid Opcode: If an invalid opcode is received, no data will be shifted into AT25080B/160B/320B/640B, and the Serial Output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

Chip Select: AT25080B/160B/320B/640B is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the Serial Output pin (SO) will remain in a high impedance state.

Hold: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select AT25080B/160B/320B/640B. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

Write Protect: The Write Protect pin ($\overline{WP}$) will allow normal read/write operations when held high. When the $\overline{WP}$ pin is brought low and WPEN bit is one, all write operations to the status register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the status register. The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is zero. This will allow the user to install AT25080B/160B/320B/640B in a system with the $\overline{WP}$ pin tied to ground and still be able to write to the status register. All $\overline{WP}$ pin functions are enabled when the WPEN bit is set to one.

Figure 4-1. SPI Serial Interface



5. Functional Description

AT25080B/160B/320B/640B is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of the 6805 and 68HC11 series of microcontrollers.

AT25080B/160B/320B/640B utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 5-1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low CS transition.

Table 5-1. Instruction Set for the Atmel AT25080B/160B/320B/640B

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data from Memory Array
WRITE	0000 X010	Write Data to Memory Array

Write Enable (WREN): The device will power up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

Write Disable (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

Read Status Register (RDSR): The Read Status Register instruction provides access to the status register. The Ready/Busy and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the block write protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 5-2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Table 5-3. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = 0 ($\overline{RDY}$) indicates the device is ready. Bit 0 = 1 indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1= 0 indicates the device is not write-enabled. Bit 1 = 1 indicates the device is write-enabled.
Bit 2 (BP0)	See Table 5-4 on page 9.
Bit 3 (BP1)	See Table 5-4 on page 9.
Bits 4 – 6 are zeros when device is not in an internal write cycle.	
Bit 7 (WPEN)	See Table 5-5 on page 9.
Bits 0 – 7 are ones during an internal write cycle.	

Write Status Register (WRSR): The WRSR instruction allows the user to select one of four levels of protection. AT25080B/160B/320B/640B is divided into four array segments; one-quarter, one-half, or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read-only. The block write protection levels and corresponding status register control bits are shown in Table 5-4.

Bits BP0, BP1, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., WREN, t_{WC}, RDSR).

Table 5-4. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected			
	BP1	BP0	Atmel AT25080B	Atmel AT25160B	Atmel AT25320B	Atmel AT25640B
0	0	0	None	None	None	None
1 (1/4)	0	1	0300 – 03FF	0600 – 07FF	0C00 – 0FFF	1800 – 1FFF
2 (1/2)	1	0	0200 – 03FF	0400 – 07FF	0800 – 0FFF	1000 – 1FFF
3 (All)	1	1	0000 – 03FF	0000 – 07FF	0000 – 0FFF	0000 – 1FFF

The WRSR instruction also allows the user to enable or disable the Write Protect ($\overline{WP}$) pin through the use of the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is one. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is zero. When the device is hardware write protected, writes to the status register, including the block protect bits and the WPEN bit, and the block-protected sections in the memory array are disabled. Writes are only allowed to sections of the memory that are not block-protected.

Note: When the WPEN bit is hardware write protected, it cannot be changed back to zero as long as the $\overline{WP}$ pin is held low.

Table 5-5. WPEN Operation

WPEN	$\overline{WP}$	WEN	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writeable	Writeable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writeable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writeable	Writeable

Read Sequence (Read): Reading AT25080B/160B/320B/640B via the Serial Output (SO) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the read opcode is transmitted via the SI line followed by the byte address to be read (A15–A0, see Table 5-6). Upon completion, any data on the SI line will be ignored. The data (D7–D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll-over to the lowest address, allowing the entire memory to be read in one continuous read cycle.

Write Sequence (Write): In order to program AT25080B/160B/320B/640B, two separate instructions must be executed. First, the device ***must be write enabled*** via the WREN instruction. Then a Write instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the Write opcode is transmitted via the SI line followed by the byte address (A15–A0) and the data (D7–D0) to be programmed (See Table 5-6). Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.

The Ready/Busy status of the device can be determined by initiating a Read Status Register (RDSR) instruction. If Bit 0 = one, the write cycle is still in progress. If Bit 0 = zero, the write cycle has ended. Only the RDSR instruction is enabled during the write programming cycle.

AT25080B/160B/320B/640B is capable of a 32-byte page write operation. After each byte of data is received, the five low-order address bits are internally incremented by one; the high-order bits of the address will remain constant. If more than 32 bytes of data are transmitted, the address counter will roll-over and the previously written data will be overwritten. AT25080B/160B/320B/640B is automatically returned to the write disable state at the completion of a write cycle.

Note: If the device is not Write Enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to reinitiate the serial communication.

Table 5-6. Address Key

Address	Atmel AT25080B	Atmel AT25160B	Atmel AT25320B	Atmel AT25640B
A_N	A_9–A_0	A_{10}–A_0	A_{11}–A_0	A_{12}–A_0
Don't Care Bits	A_{15}–A_{10}	A_{15}–A_{11}	A_{15}–A_{12}	A_{15}–A_{13}

6. Timing Diagrams

Figure 6-1. Synchronous Data Timing (for Mode 0)

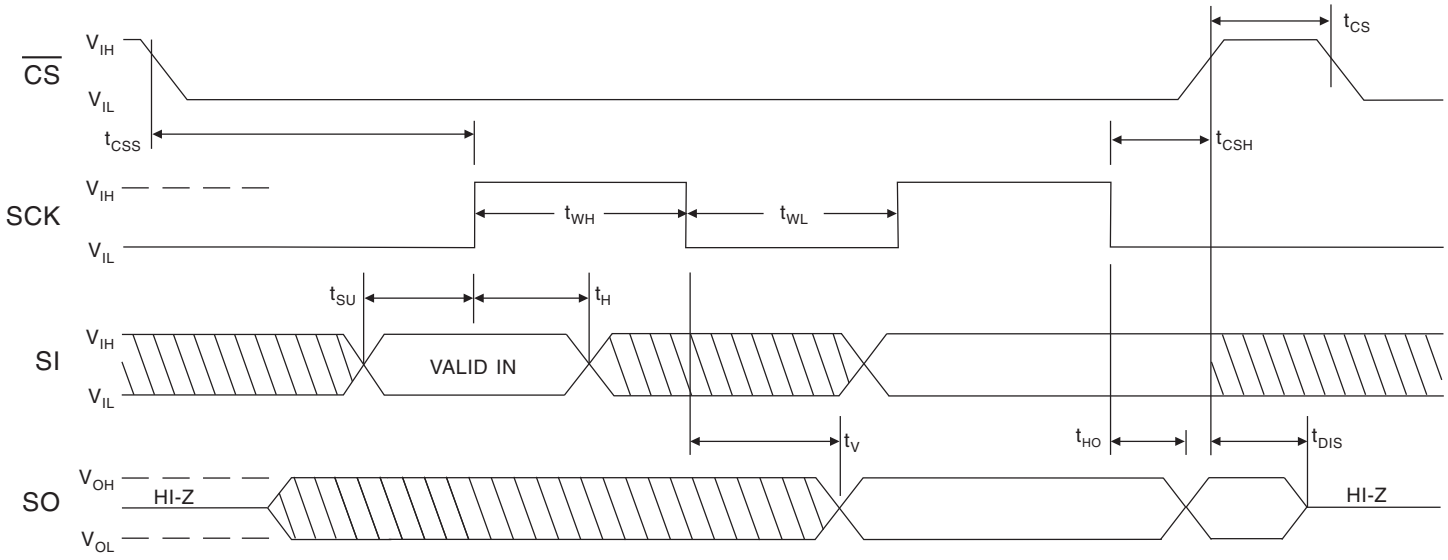


Figure 6-2. WREN Timing

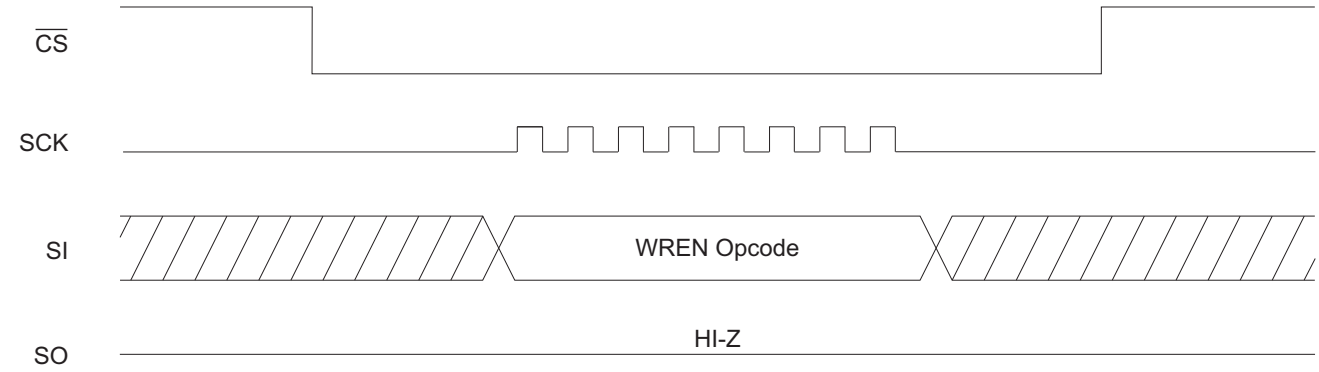


Figure 6-3. WRDI Timing

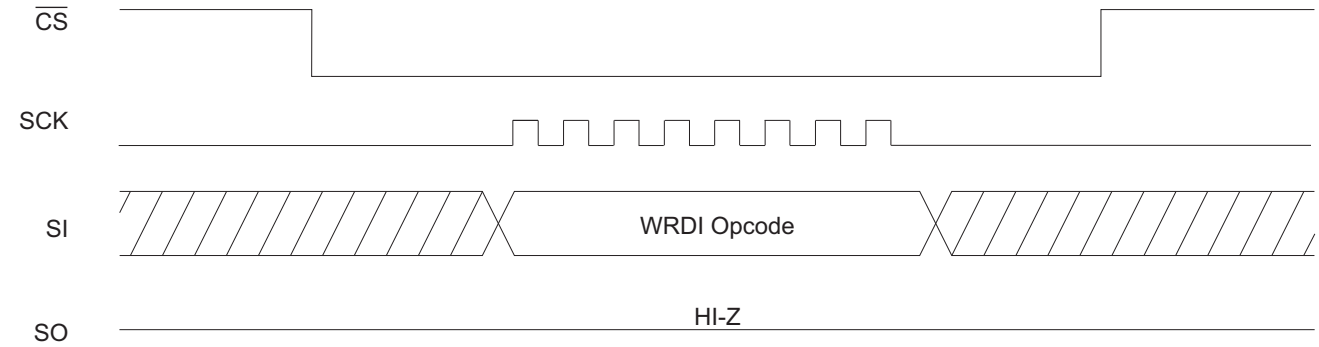


Figure 6-4. RDSR Timing

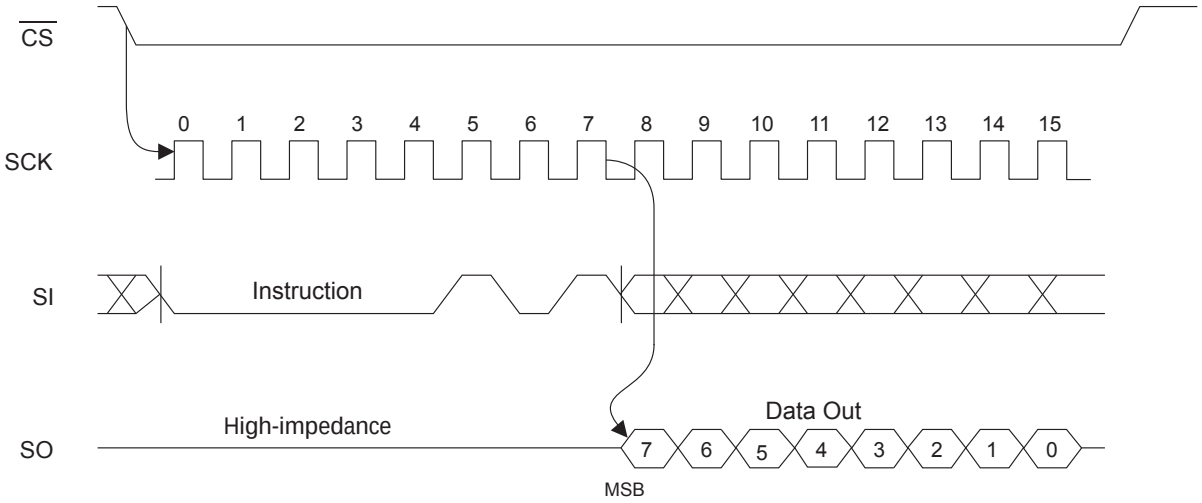


Figure 6-5. WRSR Timing

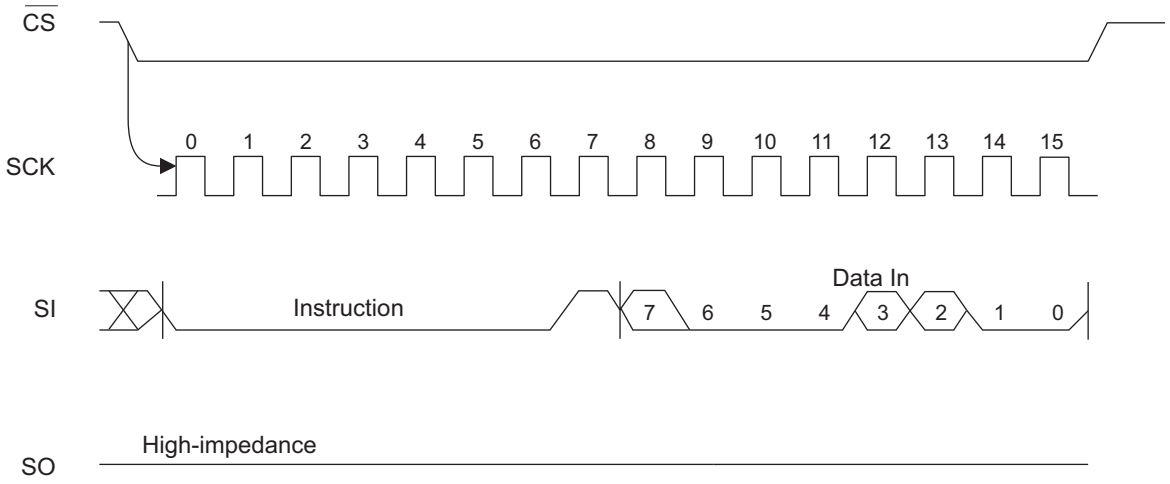


Figure 6-6. Read Timing

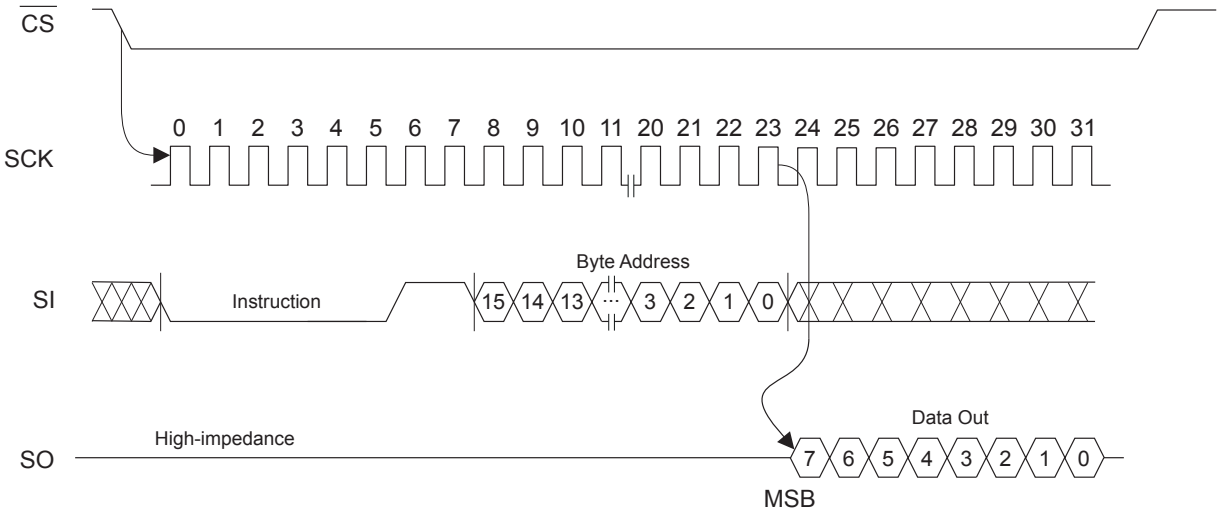


Figure 6-7. Write Timing

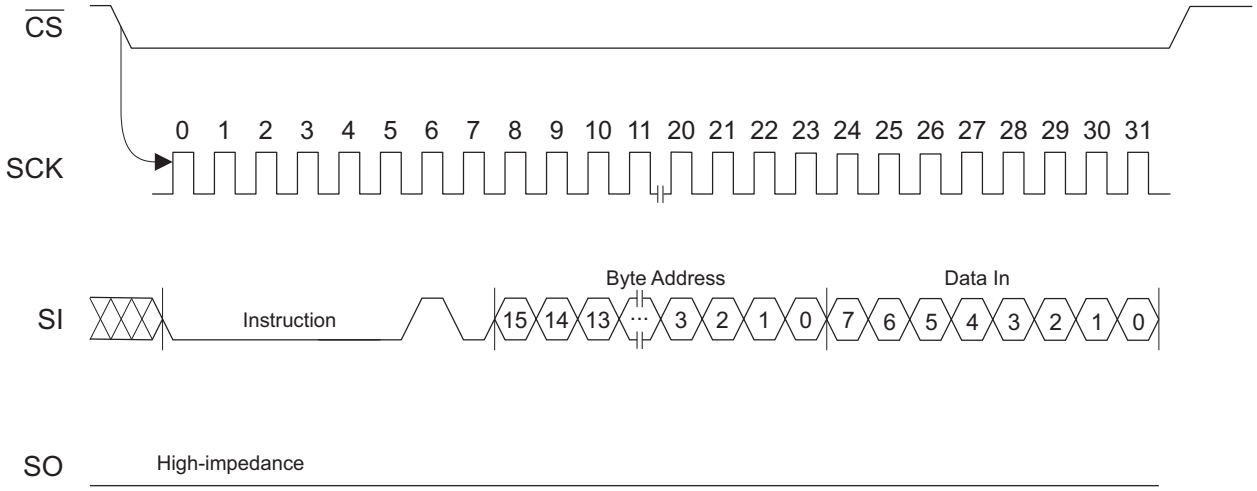
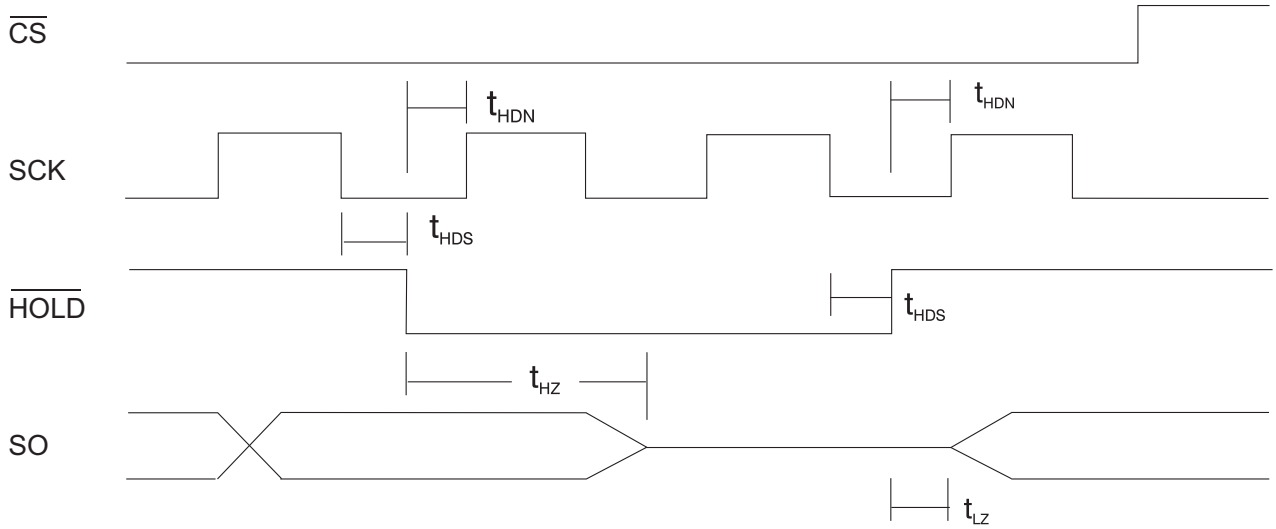


Table 6-1. $\overline{\text{HOLD}}$ Timing



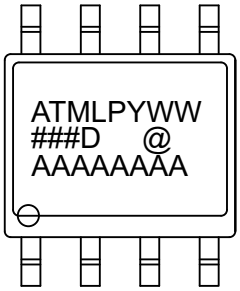
6.1 Power Recommendation

The device internal POR (Power-On Reset) threshold is just below the minimum device operating voltage. Power shall rise monotonically from 0.0Vdc to full V_{CC} in less than 1ms. Hold at full V_{CC} for at least 100µs before the first operation. Power shall drop from full V_{CC} to 0.0Vdc in less than 1ms. Power dropping to a non-zero level and then slowly going to zero is *not* recommended. Power shall remain off (0.0Vdc) for 0.5s minimum. Please consult Atmel if your power conditions do not meet the above recommendations.

7. Part Markings

8 lead SOIC

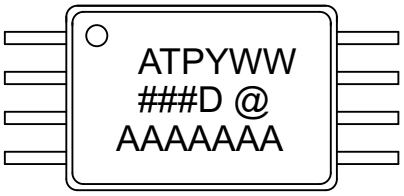
3 Rows of 8 Characters



8 lead TSSOP

3 Rows

2 of 6 and 1 of 7 Characters



Catalog Number: AT25080B
Catalog Number: AT25160B
Catalog Number: AT25320B
Catalog Number: AT25640B

Catalog Truncation: ### = 58B
Catalog Truncation: ### = 5AB
Catalog Truncation: ### = 5BB
Catalog Truncation: ### = 5CB

Date Codes			Voltages
Y = Year	M = Month	WW = Work Week of Assembly	D: 2.5v min
2: 2012 6: 2016 3: 2013 7: 2017 4: 2014 8: 2018 5: 2015 9: 2019	A: January B: February " " " L: December	02: Week 2 04: Week 4 " " " 52: Week 52	
Trace Code			Grade/Lead Finish Material
XX = Trace Code (ATMEL Lot Numbers to Correspond to Code) (e.g. XX: AA, AB...YZ, ZZ)			P: Automotive/NiPdAu
Lot Number			
AAAAAAA = ATMEL Wafer Lot Number			ATMEL Truncation
Country of Assembly			AT: ATMEL ATM: ATMEL ATML: ATMEL
@ = Country of Assembly			

2/2/12

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE 25080-16-32-64BAM, AT25080B/AT25160B/ AT25320B/AT25640B Automotive Marking Information for Package Offering	DRAWING NO. 25080-16-32-64BAM	REV. A

8. Ordering Code Information

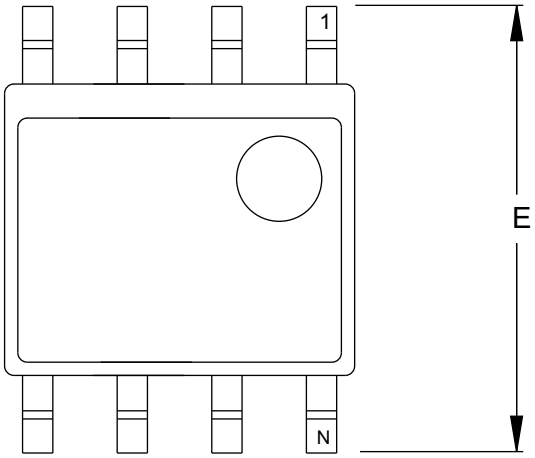
Atmel Ordering Code	Lead Finish	Package	Voltage	Operation Range
AT25080B-SSPD-T[1]	NiPdAu (Lead-free/Halogen-free)	8S1	2.5V to 5.5V	Automotive Temperature (–40°C to 125°C)
AT25080B-XPD-T[1]		8X		
AT25160B-SSPD-T[1]	NiPdAu (Lead-free/Halogen-free)	8S1	2.5V to 5.5V	Automotive Temperature (–40°C to 125°C)
AT25160B-XPD-T[1]		8X		
AT25320B-SSPD-T[1]	NiPdAu (Lead-free/Halogen-free)	8S1	2.5V to 5.5V	Automotive Temperature (–40°C to 125°C)
AT25320B-XPD-T[1]		8X		
AT25640B-SSPD-T[1]	NiPdAu (Lead-free/Halogen-free)	8S1	2.5V to 5.5V	Automotive Temperature (–40°C to 125°C)
AT25640B-XPD-T[1]		8X		

Note: 1. Tape and reel delivery:
- SOIC 4k/reel
- TSSOP 5k/reel

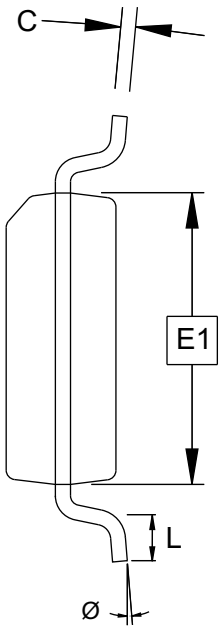
Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)

9. Packaging Information

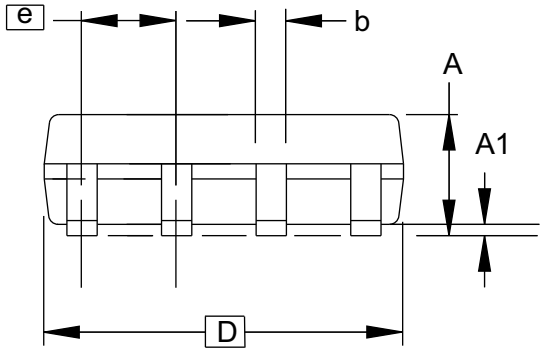
8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

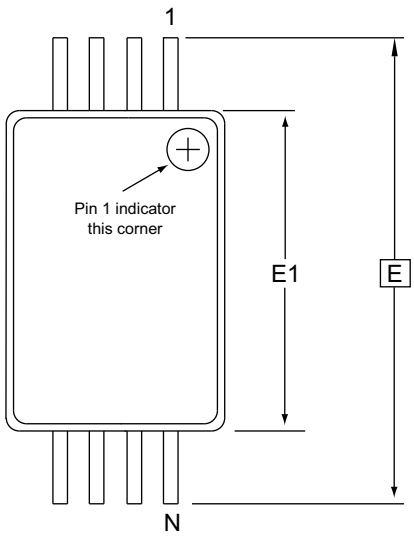
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

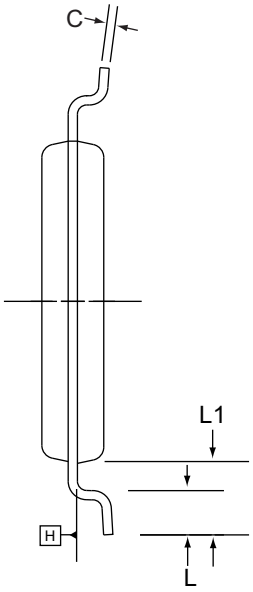
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	GPC SWB	DRAWING NO. 8S1	REV. G

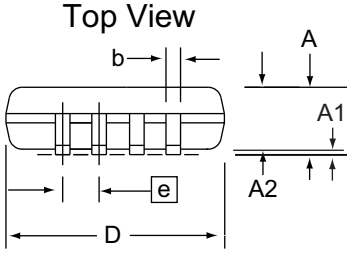
8X — 8-lead TSSOP



Top View



End View



Side View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

12/8/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**GPC** TNR	**DRAWING NO.** 8X	**REV.** E

10. Revision History

Doc. Rev.	Date	Comments
8803C	12/2012	Condense and update ordering code table.
8803B	08/2012	Remove preliminary status. Update Atmel logos and disclaimer/copy page.
8803A	02/2012	Inital document release.

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