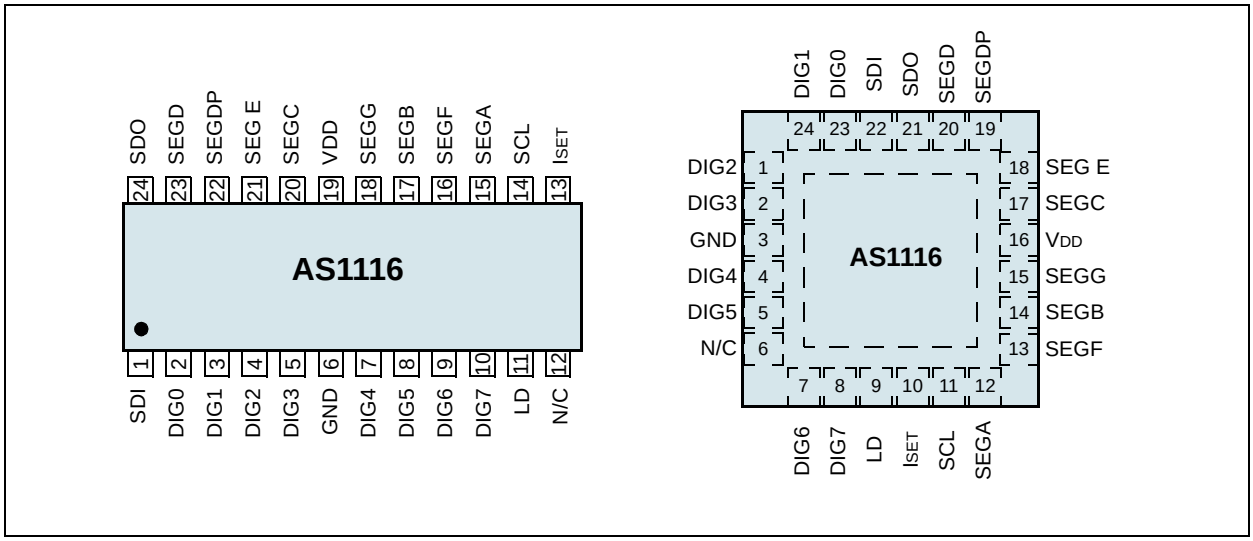
4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Name	QSOP-24	TQFN(4x4)-24	Description
SDI	1	22	**Serial-Data Input**. Data is loaded into the internal 16-bit shift register on the rising edge of pin SCL.
DIG0:DIG7	2-5, 7-10	1, 2, 4, 5, 7, 8, 23, 24	**Digit Drive Lines**. Eight digit drive lines that sink current from the display cathode.
GND	6	3	**Ground**.
LD	11	9	**Load.** Serial Data is loaded into the shift register while this pin is low. The last 16 bits of serial data are latched on the rising edge of this pin.
N/C	12	6	**Not Connected.**
ISET	13	10	**Set Segment Current**. Connect to VDD or a reference voltage through RSET to set the peak segment current (see Selecting RSET Resistor Value and Using External Drivers on page 17).
SCL	14	11	**Serial-Clock Input**. 10MHz maximum rate. Data is shifted into the internal shift register on the rising edge of this pin. Data is clocked out of pin SDO on the rising edge of this pin.
SEGA:SEGG, SEGDP	15-18, 20-23	12-15, 17-20	**Seven Segment and Decimal Point Drive Lines**. 8 seven-segment drives and decimal point drive that source current to the display.
VDD	19	16	**Positive Supply Voltage**. Connect to +2.7 to +5.5V supply.
SDO	24	21	**Serial-Data Output**. The data into pin SDI is valid at pin SDO 16 clock cycles later. This pin is used to daisy-chain several devices and is never high-impedance.
	-	Exposed Pad	**Exposed Pad.** This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Min	Max	Units	Notes
Electrical Parameters					
Input Voltage Range	V_{DD} to GND	-0.3	7	V	
	All other pins to GND	-0.3	7 or V_{DD} + 0.3	V	
Current	DIG0:DIG7 Sink Current		500	mA	
	SEGA:SEGG, SEGDP		100	mA	
Input Current (latch-up immunity)		±100		mA	Norm: JEDEC 78
Electrostatic Discharge					
Electrostatic Discharge	Digital outputs		1000	V	Norm: MIL 833 E method 3015
	All other pins		1000	V	
Thermal Information					
Thermal Resistance Θ_{JA}			88	°C/W	on PCB, QSOP-24 package
			30.5	°C/W	on PCB, TQFN(4x4)-24 package
Temperature Ranges and Storage Conditions					
Junction Temperature			+150	°C	
Storage Temperature		-55	+150	°C	
Package Body Temperature			+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing		5	85	%	
Moisture Sensitive Level	QSOP-24 package	1		%	Represents a max. floor life time of unlimited
	TQFN(4x4)-24 package	3		%	Represents a max. floor life time 168h

6 Electrical Characteristics

VDD = 2.7 to 5.5V, RSET = 9.53kΩ, Typical values are at *TAMB* = +25°C, *VDD* = 5.0V *(unless otherwise specified)*. All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TAMB	Operating Temperature Range		-40		+85	°C
TJ	Operating Junction Temperature		-40		+125	°C
VDD	Operating Supply Voltage		2.7		5.5	V
IDDSD	Shutdown Supply Current	All digital inputs at VDD or GND, TAMB = +25ºC		0.2	2	µA
IDD	Operating Supply Current	RSET = open circuit.		0.35	0.6	mA
		All segments and decimal point on; ISEG = -40mA.		335		
fOSC	Display Scan Rate	8 digits scanned	0.6	0.8	1.2	kHz
IDIGIT	Digit Drive Sink Current	VOUT = 0.65V	320			mA
ISEG	Segment Drive Source Current	VDD = 5.0V, VOUT = (VDD -1V)	-37	-42	-47	mA
ΔISEG	Segment Drive Current Matching			3		%
ISEG	Segment Drive Source Current	Average Current			47	mA

Table 4. Logic Inputs/Outputs Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IIH, IIL	Input Current SDI, SCL, LD	VIN = 0V or VDD	-1		1	µA
VIH	Logic High Input Voltage	4.5V < VDD < 5.5V	0.6 x VDD			V
		2.7V < VDD < 4.5V	0.7 x VDD			V
VIL	Logic Low Input Voltage	VDD = 5.0V			0.8	V
		VDD = 3.0V			0.6	
VOH	Output High Voltage	SDO, ISOURCE = -1mA, VDD = 5.0V	VDD - 1			V
		SDO, ISOURCE = -1mA, VDD = 3.0V	VDD - 0.5			
VOL	Output Low Voltage	SDO, ISINK = 1mA			0.4	V
ΔVI	Hysteresis Voltage	SDI, SCL, LD		1		V
	Open Detection Level Threshold		0.7x VDD	0.75x VDD	0.8x VDD	V
	Short Detection Level Threshold		0.05x VDD	0.1x VDD	0.15x VDD	V

Table 5. SPI Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CP}	SCL Clock Period		100			ns
t_{CH}	SCL Pulse Width High		20			ns
t_{CL}	SCL Pulse Width Low		20			ns
t_{CSS}	LD to SCL Rise Setup Time		25			ns
t_{CSH}	SCL Rise to LD Rise Hold Time		10			ns
t_{DS}	SDI Setup Time		0			ns
t_{DH}	SDI Hold Time		5			ns
t_{DO}	Output Data Propagation Delay	C_{LOAD} = 50pF			25	ns
t_{LDCK}	LD Rising Edge to SCL Rising Edge		20			ns
t_{CSW}	Minimum LD Pulse High		20			ns
t_{DSPD}	Data-to-Segment Delay				2.25	ms

See Figure 19 on page 10 for more information.

7 Typical Operating Characteristics

R_{SET} = 9.53kΩ, V_{Rset} = V_{DD};

Figure 3. Display Scan Rate vs. Supply Voltage;

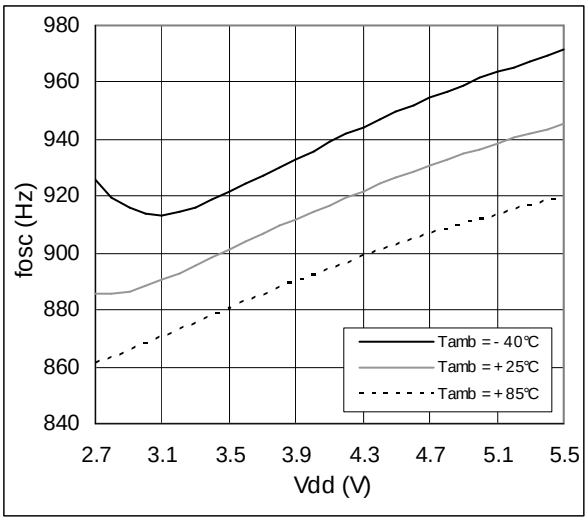


Figure 4. Display Scan Rate vs. Temperature;

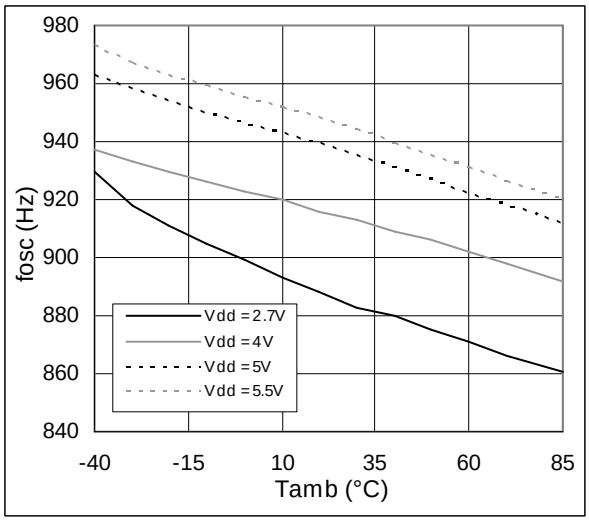


Figure 5. Segment Current vs. Temperature;

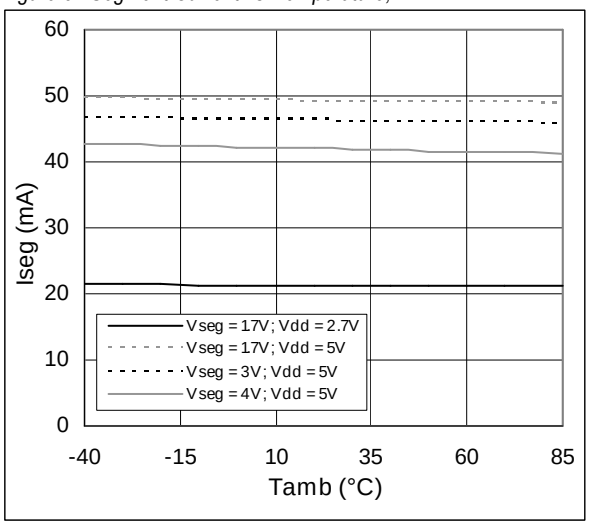


Figure 6. Segment Current vs. R_{SET};

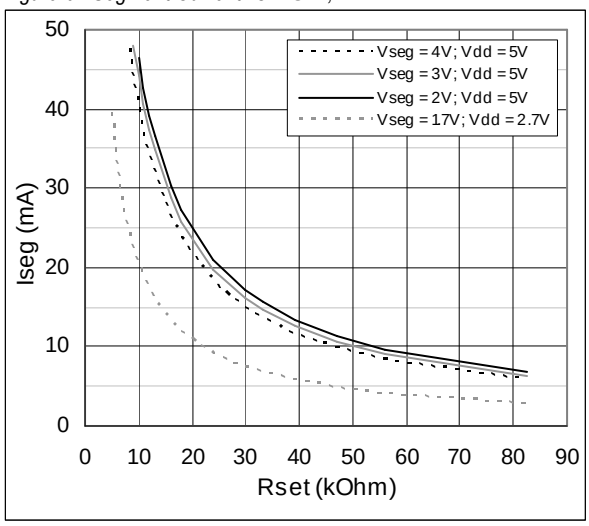


Figure 7. Segment Current vs. Supply Voltage;

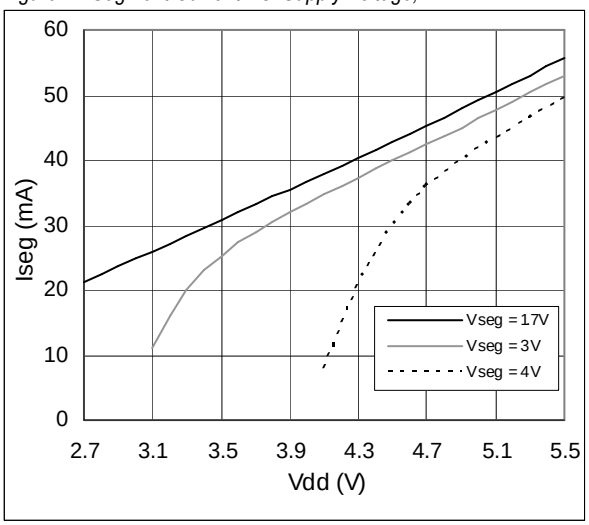


Figure 8. Segment Current vs. V_{DD}; V_{Rset} = 2.8V

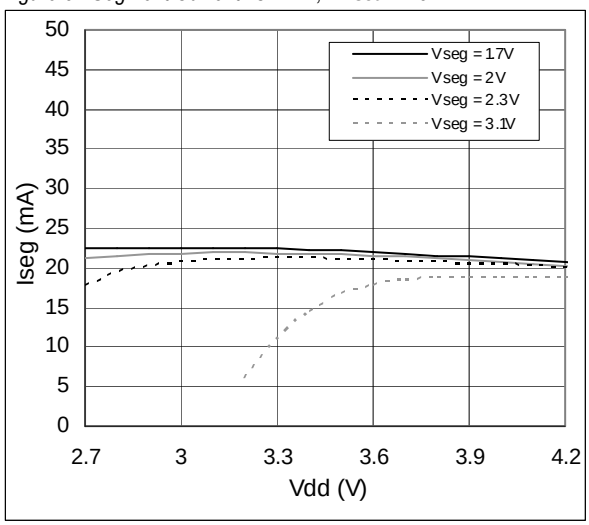


Figure 9. VDIGIT vs. IDIGIT

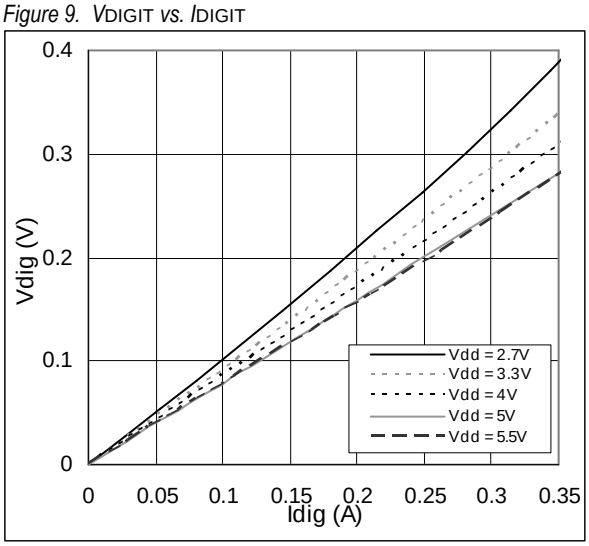


Figure 10. Input High Level vs. Supply Voltage

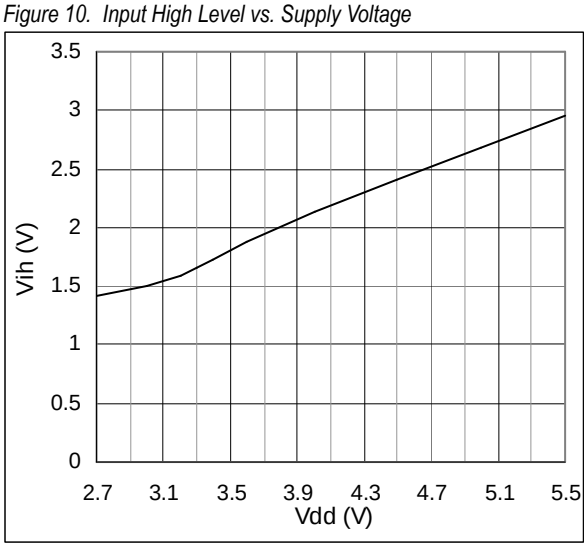


Figure 11. ISEG vs. VSEG; VDD = 5V

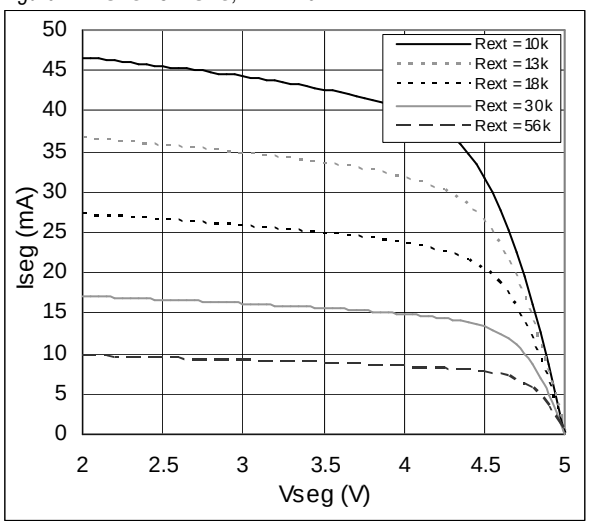


Figure 12. ISEG vs. VSEG; VDD = 4V

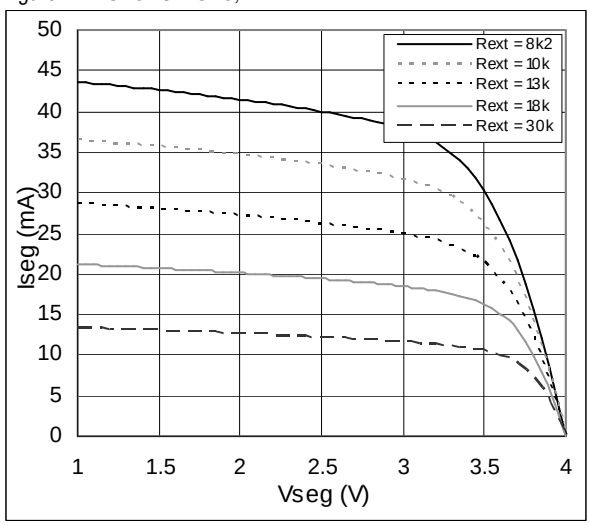


Figure 13. ISEG vs. VSEG; VDD = 3.3V

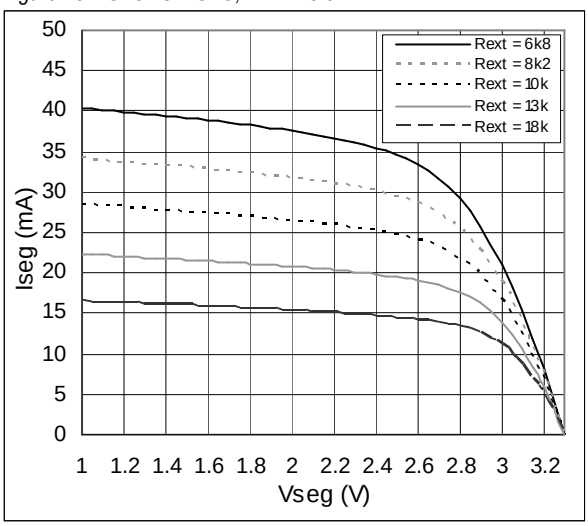
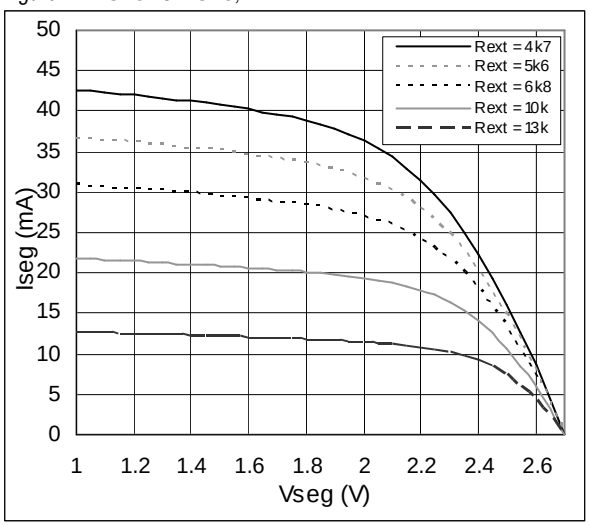


Figure 14. ISEG vs. VSEG; VDD = 2.7V



8 Detailed Description

Block Diagram

Figure 15. Block Diagram (QSOP-24 Package)

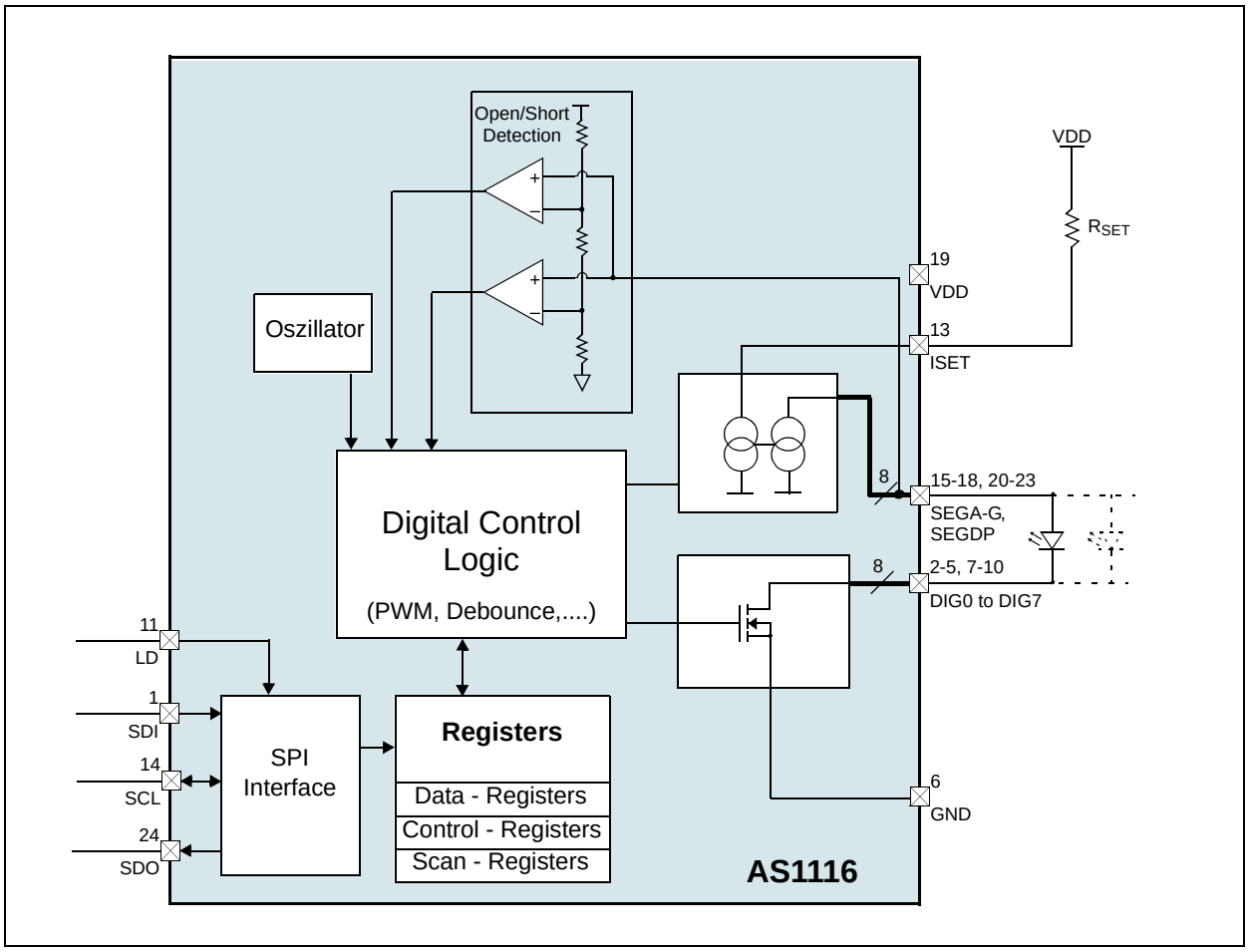
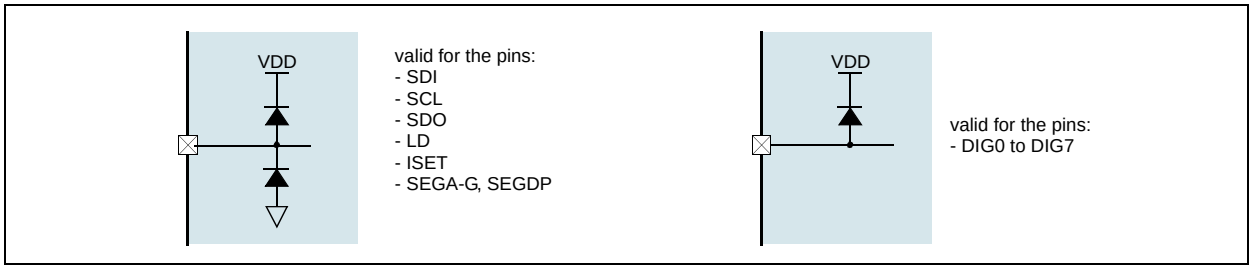


Figure 16. ESD Structure



Serial Interface

The AS1116 contains a 16bit SPI interface to access the internal data and control registers of the device (see Digit- and Control-Registers on page 11). The SPI interface is driven with the rising edge of SCL. A falling edge on LD signal indicates the beginning of an access on the SPI interface, the rising edge on LD determines an access on SPI. An access must consist of exactly 16bits for write operation and 8bits for read operation. Timing restrictions on the SPI interface pins are defined in Figure 19.

Table 6 shows the structure of the 16bit command word for writing data. The bits D0 to D7 are the data information, bits D8 to D12 are the address bits, D13 is set to '0', bit D14 is defining the read (D14 = '1') or the write (D14 = '0') configuration and bit D15 is a don't care bit.

In Table 7 on page 11 the 8bit command word for the read operation can be found.

Bit D0 (write operation) or bit D8 (read operation) is the first bit to shift into the SPI interface after the falling edge of LD. Bit D15 is the last bit to write to SPI before rising edge of LD.

At a read operation an 8bit operation is executed (see Figure 18). At the first rising edge of SCL after the rising edge of LD D7 of addressed register is written to SDO pin. At the next rising edge of SCL D6 is written to SDO pin. LD must be kept high during reading data from a internal data or control register of AS1116.

Table 6. 16-Bit Serial Data Format

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
LSB				Data			MSB	Register Address (see Table 7)					0	R/W	X

Figure 17. Write operation

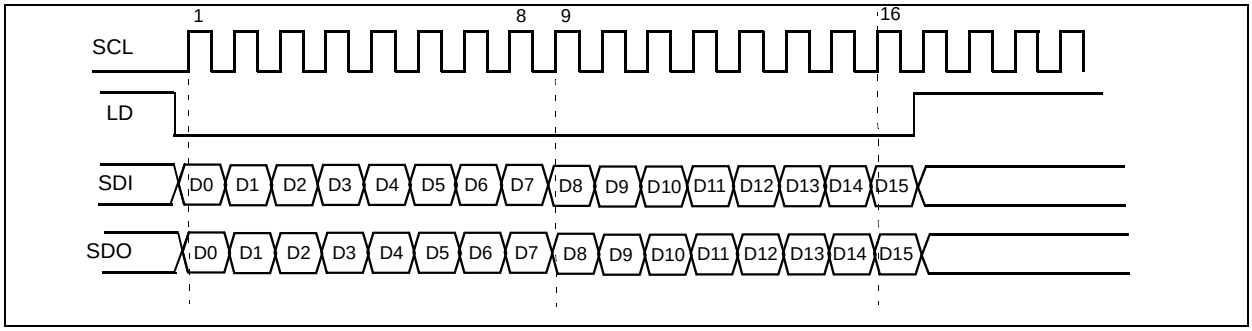


Figure 18. Read operation

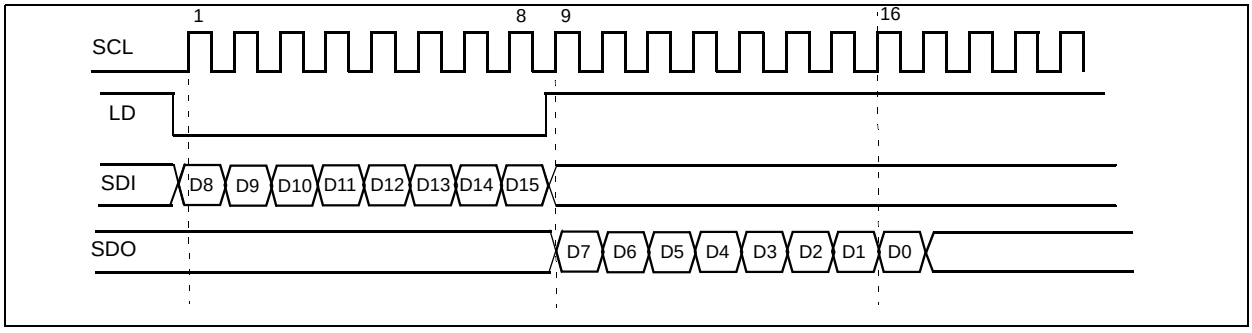
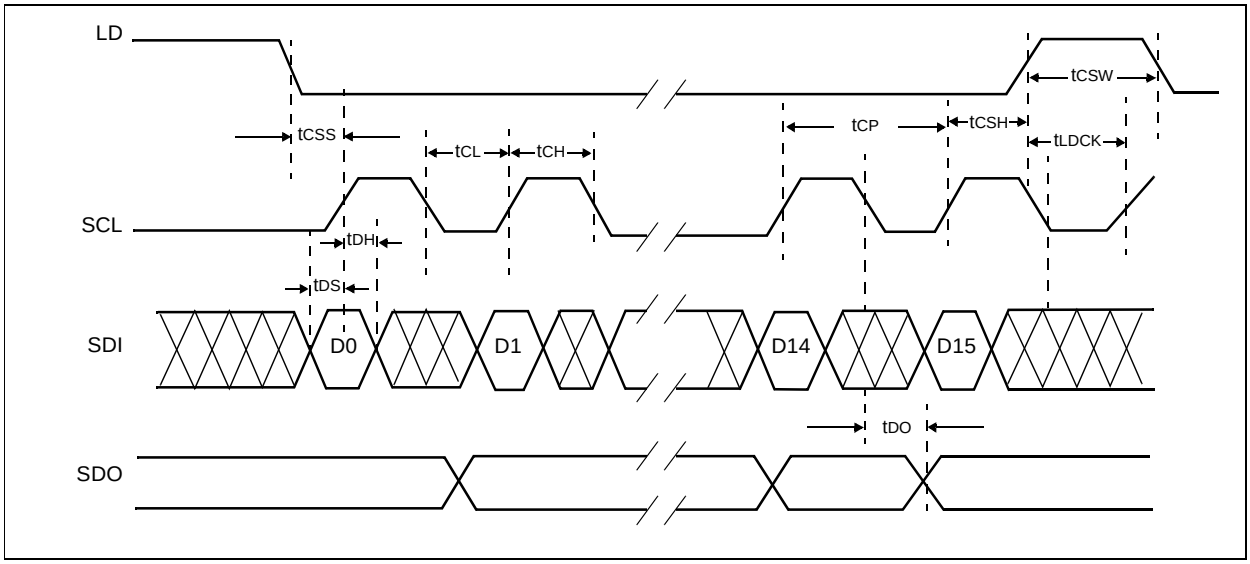


Figure 19. Interface Timing



Initial Power-Up

On initial power-up, the AS1116 registers are reset to their default values, the display is blanked, and the device goes into shutdown mode. At this time, all registers should be programmed for normal operation.

Note: The default settings enable only scanning of one digit; the internal decoder is disabled and the Intensity Control Register (see page 15) is set to the minimum values.

Shutdown Mode

The AS1116 devices feature a shutdown mode, where they consume only 200nA (typ) current. Shutdown mode is entered via a write to the Shutdown Register (see Table 8). For the AS1116, at that point, all segment current sources and digital drivers are switched off, so that all segments are blanked.

Note: During shutdown mode the Digit-Registers maintain their data.

Shutdown mode can either be used as a means to reduce power consumption or for generating a flashing display (repeatedly entering and leaving shutdown mode). For minimum supply current in shutdown mode, logic input should be at GND or V_{DD} (CMOS logic level).

When entering or leaving shutdown mode, the Feature Register is reset to its default values (all 0s) when Shutdown Register bit D7 (page 12) = 0.

Note: When Shutdown Register bit D7 = 1, the Feature Register is left unchanged when entering or leaving shutdown mode. If the AS1116 is used with an external clock, Shutdown Register bit D7 should be set to 1 when writing to the Shutdown Register.

Digit- and Control-Registers

The AS1116 devices contain 8 Digit-Registers,11 control-registers and 8 diagnostic-registers, which are listed in Table 7. All registers are selected using a 8-bit address word, and communication is done via the serial interface.

- Digit Registers – These registers are realized with an on-chip 64-bit memory. Each digit can be controlled directly without rewriting the whole register contents.
- Control Registers – These registers consist of decode mode, display intensity, number of scanned digits, shutdown, display test and features selection registers.

Table 7. Register Address Map

Type	Register	Address									Page
		D15	D14	D13	D12	D11	D10	D9	D8	D7:D0	
	No-Op	X	0	0	0	0	0	0	0		16
Digit Register	Digit 0	X	0	0	0	0	0	0	1	(see Table 10 on page 12, Table 11 on page 13 and Table 12 on page 13)	N/A
	Digit 1	X	0	0	0	0	0	1	0		N/A
	Digit 2	X	0	0	0	0	0	1	1		N/A
	Digit 3	X	0	0	0	0	1	0	0		N/A
	Digit 4	X	0	0	0	0	1	0	1		N/A
	Digit 5	X	0	0	0	0	1	1	0		N/A
	Digit 6	X	0	0	0	0	1	1	1		N/A
	Digit 7	X	0	0	0	1	0	0	0		N/A
Control Register	Decode-Mode	X	0	0	0	1	0	0	1	(see Table 9 on page 12)	12
	Global Intensity	X	0	0	0	1	0	1	0	(see Table 16 on page 15)	15
	Scan Limit	X	0	0	0	1	0	1	1	(see Table 18 on page 15)	15
	Shutdown	X	0	0	0	1	1	0	0	(see Table 8 on page 12)	12
	Not Used	X	0	0	0	1	1	0	1		N/A
	Feature	X	0/1	0	0	1	1	1	0	(see Table 19 on page 16)	16
	Display Test Mode	X	0	0	0	1	1	1	1	(see Table 13 on page 14)	12
	DIG0:DIG1 Intensity	X	0	0	1	0	0	0	0	(see Table 17 on page 15)	
	DIG2:DIG3 Intensity	X	0	0	1	0	0	0	1	(see Table 17 on page 15)	
	DIG4:DIG5 Intensity	X	0	0	1	0	0	1	0	(see Table 17 on page 15)	
	DIG6:DIG7 Intensity	X	0	0	1	0	0	1	1	(see Table 17 on page 15)	
Diagnostic Register	Diagnostic Digit 0	X	1	0	1	0	1	0	0		N/A
	Diagnostic Digit 1	X	1	0	1	0	1	0	1		N/A
	Diagnostic Digit 2	X	1	0	1	0	1	1	0		N/A
	Diagnostic Digit 3	X	1	0	1	0	1	1	1		N/A
	Diagnostic Digit 4	X	1	0	1	1	0	0	0		N/A
	Diagnostic Digit 5	X	1	0	1	1	0	0	1		N/A
	Diagnostic Digit 6	X	1	0	1	1	0	1	0		N/A
	Diagnostic Digit 7	X	1	0	1	1	0	1	1		N/A

Note: Write operation: D14=0; Read operation: D14=1.

The Shutdown Register controls AS1116 shutdown mode.

Table 8. Shutdown Register Format (Address (HEX) = 0x0C))

Mode	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Mode, Reset Feature Register to Default Settings	0x00	0	X	X	X	X	X	X	0
Shutdown Mode, Feature Register Unchanged	0x80	1	X	X	X	X	X	X	0
Normal Operation, Reset Feature Register to Default Settings	0x01	0	X	X	X	X	X	X	1
Normal Operation, Feature Register Unchanged	0x81	1	X	X	X	X	X	X	1

Decode Enable Register (0x09)

The Decode Enable Register sets the decode mode. BCD/HEX decoding (either BCD code – characters 0:9, E, H, L, P, and -, or HEX code – characters 0:9 and A:F) is selected by bit D2 (page 16) of the Feature Register. The Decode Enable Register is used to select the decode mode or no-decode for each digit. Each bit in the Decode Enable Register corresponds to its respective display digit (i.e., bit D0 corresponds to digit 0, bit D1 corresponds to digit 1 and so on). Table 10 lists some examples of the possible settings for the Decode Enable Register bits.

Note: A logic high enables decoding and a logic low bypasses the decoder altogether.

When decode mode is used, the decoder looks only at the lower-nibble (bits D3:D0) of the data in the Digit-Registers, disregarding bits D6:D4. Bit D7 sets the decimal point (SEG DP) independent of the decoder and is positive logic (bit D7 = 1 turns the decimal point on). Table 10 lists the code-B font; Table 11 lists the HEX font.

When no-decode mode is selected, data bits D7:D0 of the Digit-Registers correspond to the segment lines of the AS1116. Table 12 shows the 1:1 pairing of each data bit to the appropriate segment line.

Table 9. Decode Enable Register Format Examples

Decode Mode	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
No decode for digits 7:0	0x00	0	0	0	0	0	0	0	0
Code-B/HEX decode for digit 0. No decode for digits 7:1	0x01	0	0	0	0	0	0	0	1
Code-B/HEX decode for digit 0:2. No decode for digits 7:3	0x07	0	0	0	0	0	1	1	1
Code-B/HEX decode for digits 0:5. No decode for digits 7:6	0x3F	0	0	1	1	1	1	1	1
Code-B/HEX decode for digits 0,2,5. No decode for digits 1, 3, 4, 6, 7	0x25	0	0	1	0	0	1	0	1

Table 10. Code-B Font

Char-acter	Register Data						Char-acter	Register Data						Char-acter	Register Data					
	D7	D6:D4	D3	D2	D1	D0		D7	D6: D4	D3	D2	D1	D0		D7	D6:D4	D3	D2	D1	D0
0		X	0	0	0	0	6		X	0	1	1	0	H		X	1	1	0	0
1		X	0	0	0	1	7		X	0	1	1	1	L		X	1	1	0	1
2		X	0	0	1	0	8		X	1	0	0	0	P		X	1	1	1	0
3		X	0	0	1	1	9		X	1	0	0	1			X	1	1	1	1
4		X	0	1	0	0	-		X	1	0	1	0	.	1*	X	X	X	X	X
5		X	0	1	0	1	E		X	1	0	1	1							

* The decimal point can be enabled with every character by setting bit D7 = 1.

Table 11. HEX Font

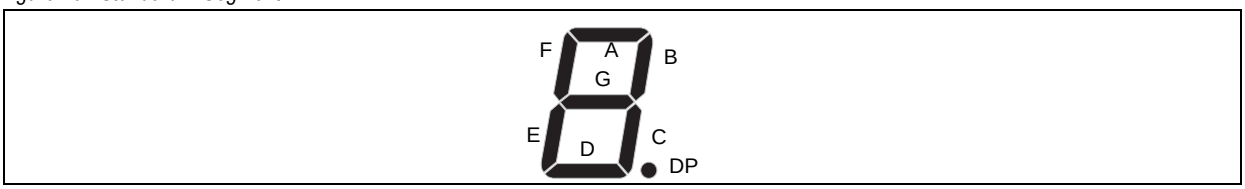
Char-acter	Register Data						Char-acter	Register Data						Char-acter	Register Data					
	D7	D6:D4	D3	D2	D1	D0		D7	D6: D4	D3	D2	D1	D0		D7	D6:D4	D3	D2	D1	D0
0		X	0	0	0	0	6		X	0	1	1	0	C		X	1	1	0	0
1		X	0	0	0	1	7		X	0	1	1	1	d		X	1	1	0	1
2		X	0	0	1	0	8		X	1	0	0	0	E		X	1	1	1	0
3		X	0	0	1	1	9		X	1	0	0	1	F		X	1	1	1	1
4		X	0	1	0	0	A		X	1	0	1	0		1*	X	X	X	X	X
5		X	0	1	0	1	b		X	1	0	1	1							

* The decimal point can be enabled with every character by setting bit D7 = 1.

Table 12. No-Decode Mode Data Bits and Corresponding Segment Lines

	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding Segment Line	DP	A	B	C	D	E	F	G

Figure 20. Standard 7-Segment LED



Display-Test Mode

The AS1116 can detect open or shorted LEDs. Readout of either open LEDs (D2=1) or short LEDs (D1=1) is possible, as well as a OR relation of open and short (D1=D2=1). After a diagnostic run bit D4 can be read to clarify if an error occurred before reading out detailed diagnostic data.

Note: All settings of the digit- and control-registers are maintained.

Table 13. Testmode Register *Summary*

D7	D6	D5	D4	D3	D2	D1	D0
X	REXT_short	REXT_open	LED_global	LED_test	LED_open	LED_short	DISP_test

Table 14. Testmode Register Bit Description (Address (HEX) = 0x0F))

Addr: 0x0F		Address		
Bit	**Bit Name**	**Default**	**Access**	**D7:D0**
D0	DISP_test	0	W	Optical display test. (Testmode for external visual test.) 0: Normal operation; 1: Run display test (All digits are tested independently from scan limit & shutdown register.)
D1	LED_short	0	W	Starts a test for shorted LEDs. (Can be set together with D2) 0: Normal operation; 1: Activate testmode
D2	LED_open	0	W	Starts a test for open LEDs. (Can be set together with D1) 0: Normal operation; 1: Activate testmode
D3	LED_test	0	R	Indicates an ongoing open/short LED test 0: No ongoing LED test; 1: LED test in progress
D4	LED_global	0	R	Indicates that the last open/short LED test has detected an error 0: No error detected; 1: Error detected
D5	REXT_open	0	R	Checks if external resistor REXT is open 0: REXT correct; 1: REXT is open
D6	REXT_short	0	R	Checks if external resistor REXT is shorted 0: REXT correct; 1: REXT is shorted
D7		0	-	Not used

LED Diagnostic Registers

These eight registers contain the result of the LED open/short test for the individual LED of each digit.

Table 15. LED Diagnostic Register Address

Register HEX Address		Segment								Register HEX Address		Segment							
	Digit	D7	D6	D5	D4	D3	D2	D1	D0		Digit	D7	D6	D5	D4	D3	D2	D1	D0
0x14	DIG0	DP	A	B	C	D	E	F	G	*0x18*	DIG4	DP	A	B	C	D	E	F	G
0x15	DIG1									*0x19*	DIG5								
0x16	DIG2									*0x1A*	DIG6								
0x17	DIG3									*0x1B*	DIG7								

Note: If more than 2 shorts occure in the LED array, detection of individual LED fault could become limited to blocs.

Intensity Control Register (0x0A)

The brightness of the display can be controlled by digital means using the Intensity Control Registers and by analog means using RSET (see Selecting RSET Resistor Value and Using External Drivers on page 17). The intensity can be controlled globally for all digits, or for each digit individually. The global intensity command will write intensity data to all four individual brightness registers, while the individual intesity command will only write to the associated individual intensity register.

Display brightness is controlled by an integrated pulse-width modulator which is controlled by the lower-nibble of the Intensity Control Register. The modulator scales the average segment-current in 16 steps from a maximum of 15/16 down to 1/16 of the peak current set by RSET.

Table 16. Intensity Register Format

Duty Cycle	HEX Code	Register Data					Duty Cycle	HEX Code	Register Data			
		MSB	D2	D1	LSB				MSB	D2	D1	LSB
1/16 (min on)	0xX0	0	0	0	0		9/16	0xX8	1	0	0	0
2/16	0xX1	0	0	0	1		10/16	0xX9	1	0	0	1
3/16	0xX2	0	0	1	0		11/16	0xXA	1	0	1	0
4/16	0xX3	0	0	1	1		12/16	0xXB	1	0	1	1
5/16	0xX4	0	1	0	0		13/16	0xXC	1	1	0	0
6/16	0xX5	0	1	0	1		14/16	0xXD	1	1	0	1
7/16	0xX6	0	1	1	0		15/16	0xXE	1	1	1	0
8/16	0xX7	0	1	1	1		15/16 (max on)	0xXF	1	1	1	1

Table 17. Intensity Register Address

Register HEX Address		Register Data	
	Type	D7:D4	D3:D0
0x0A	Global	X	Global Intensity
0x10	Digit	Digit 1 Intensity	Digit 0 Intensity
0x11	Digit	Digit 3 Intensity	Digit 2 Intensity
0x12	Digit	Digit 5 Intensity	Digit 4 Intensity
0x13	Digit	Digit 7 Intensity	Digit 6 Intensity

Scan-Limit Register (0x0B)

The Scan-Limit Register controls which of the digits are to be displayed. When all 8 digits are to be displayed, the update frequency is typically 0.8kHz. If the number of digits displayed is reduced, the update frequency is increased. The frequency can be calculated using 8fOSC/N, where N is the number of digits. Since the number of displayed digits influences the brightness, RSET should be adjusted accordingly.

Note: To avoid differences in brightness this register should not be used to blank parts of the display (leading zeros).

Table 18. Scan-Limit Register Format (Address (HEX) = 0x0B))

Scan Limit	HEX Code	Register Data					Scan Limit	HEX Code	Register Data			
		D7:D3	D2	D1	D0				D7:D3	D2	D1	D0
Display digit 0 only	0xX0	X	0	0	0		Display digits 0:4	0xX4	X	1	0	0
Display digits 0:1	0xX1	X	0	0	1		Display digits 0:5	0xX5	X	1	0	1
Display digits 0:2	0xX2	X	0	1	0		Display digits 0:6	0xX6	X	1	1	0
Display digits 0:3	0xX3	X	0	1	1		Display digits 0:7	0xX7	X	1	1	1

Feature Register (0x0E)

The Feature Register is used for enabling various features including switching the device into external clock mode, applying an external reset, selecting code-B or HEX decoding, enabling or disabling blinking, enabling or disabling the SPI-compatible interface, setting the blinking rate, and resetting the blink timing.

Note: At power-up the Feature Register is initialized to 0.

Table 19. Feature Register Summary

D7	D6	D5	D4	D3	D2	D1	D0
blink_start	sync	blink_freq_sel	blink_en	NU	decode_sel	reg_res	clk_en

Table 20. Feature Register Bit Descriptions (Address (HEX) = 0xXE)

Addr: 0xXE		Feature Register		
		Enables and disables various device features.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
D0	clk_en	0	R/W	External clock active. 0 = Internal oscillator is used for system clock. 1 = Pin CLK of the serial interface operates as system clock input.
D1	reg_res	0	R/W	Resets all control registers except the Feature Register. 0 = Reset Disabled. Normal operation. 1 = All control registers are reset to default state (except the Feature Register) identically after power-up. **Note:** The Digit Registers maintain their data.
D2	decode_sel	0	R/W	Selects display decoding for the selected digits (Table 9 on page 12). 0 = Enable Code-B decoding (see Table 10 on page 12). 1 = Enable HEX decoding (see Table 11 on page 13).
D3	NU			Not used
D4	blink_en	0	R/W	Enables blinking. 0 = Disable blinking. 1 = Enable blinking.
D5	blink_freq_sel	0	R/W	Sets blink with low frequency (with the internal oscillator enabled): 0 = Blink period typically is 1 second (0.5s on, 0.5s off). 1 = Blink period is 2 seconds (1s on, 1s off).
D6	sync	0	R/W	Synchronizes blinking on the rising edge of pin LD. The multiplex and blink timing counter is cleared on the rising edge of pin LD. By setting this bit in multiple devices, the blink timing can be synchronized across all the devices.
D7	blink_start	0	R/W	Start Blinking with display enabled phase. When bit D4 (blink_en) is set, bit D7 determines how blinking starts. 0 = Blinking starts with the display turned off. 1 = Blinking starts with the display turned on.

No-Op Register (0xX0)

The No-Op Register is used when multiple AS1116 devices are cascaded in order to support displays with more than 8 digits. The cascading must be done in such a way that all SDO pins are connected to SDI of the next AS1116 (see Figure 21 on page 18). The LD and SCL signals are connected to all devices.

For example, if five devices are cascaded, in order to perform a write operation to the fifth device, the write-command must be followed by four no-operation commands. When the LD signal goes high, all shift registers are latched. The first four devices will receive no-operation commands and only the fifth device will receive the intended operation command, and subsequently update its register.

9 Typical Application

Selecting R_{SET} Resistor Value and Using External Drivers

Brightness of the display segments is controlled via RSET. The current that flows between VDD and ISET defines the current that flows through the LEDs.

Segment current is about 200 times the current in ISET. Typical values for RSET for different segment currents, operating voltages, and LED voltage drop (VLED) are given in Table 21 & Table 22. The maximum current the AS1116 can drive is 47mA. If higher currents are needed, external drivers must be used, in which case it is no longer necessary that the devices drive high currents.

Note: The display brightness can also be logically controlled (see Intensity Control Register (0x0A) on page 15).

Table 21. RSET vs. Segment Current and LED Forward Voltage, VDD = 2.7V & 3.3V & 3.6V

ISEG (mA)		VLED			VLED				VLED			
		1.5V	2.0V		1.5V	2.0V	2.5V		1.5V	2.0V	2.5V	3.0V
40	VDD = 2.7V	5kΩ	4.4kΩ	VDD = 3.3V	6.7kΩ	6.4kΩ	5.7kΩ	VDD = 3.6V	7.5kΩ	7.2kΩ	6.6kΩ	5.5kΩ
30		6.9kΩ	5.9kΩ		9.1kΩ	8.8kΩ	8.1kΩ		10.18kΩ	9.8kΩ	9.2kΩ	7.5kΩ
20		10.7kΩ	9.6kΩ		13.9kΩ	13.3kΩ	12.6kΩ		15.6kΩ	15kΩ	14.3kΩ	13kΩ
10		22.2kΩ	20.7kΩ		28.8kΩ	27.7kΩ	26kΩ		31.9kΩ	31kΩ	29.5kΩ	27.3kΩ

Table 22. RSET vs. Segment Current and LED Forward Voltage, VDD = 4.0V & 5.0V

ISEG (mA)		VLED						VLED					
		1.5V	2.0V	2.5V	3.0V	3.5V		1.5V	2.0V	2.5V	3.0V	3.5V	4.0V
40	VDD = 4.0V	8.6kΩ	8.3kΩ	7.9kΩ	7.6kΩ	5.2kΩ	VDD = 5.0V	11.35kΩ	11.12kΩ	10.84kΩ	10.49kΩ	10.2kΩ	9.9kΩ
30		11.6kΩ	11.2kΩ	10.8kΩ	9.9kΩ	7.8kΩ		15.4kΩ	15.1kΩ	14.7kΩ	14.4kΩ	13.6kΩ	13.1kΩ
20		17.7kΩ	17.3kΩ	16.6kΩ	15.6kΩ	13.6kΩ		23.6kΩ	23.1kΩ	22.6kΩ	22kΩ	21.1kΩ	20.2kΩ
10		36.89kΩ	35.7kΩ	34.5kΩ	32.5kΩ	29.1kΩ		48.9kΩ	47.8kΩ	46.9kΩ	45.4kΩ	43.8kΩ	42kΩ

Calculating Power Dissipation

The upper limit for power dissipation (PD) for the AS1116 is determined from the following equation:

$$PD = (V_{DD} \times 5mA) + (V_{DD} - V_{LED})(DUTY \times I_{SEG} \times N) \quad (EQ\ 1)$$

Where:

VDD is the supply voltage.
DUTY is the duty cycle set by intensity register (page 15).
N is the number of segments driven (worst case is 8)
VLED is the LED forward voltage
ISEG = segment current set by RSET

Dissipation Example:

$$I_{SEG} = 40mA,\ N = 8,\ DUTY = 15/16,\ V_{LED} = 2.2V \text{ at } 40mA,\ V_{DD} = 5V \quad (EQ\ 2)$$

$$PD = 5V(5mA) + (5V - 2.2V)(15/16 \times 40mA \times 8) = 0.865W \quad (EQ\ 3)$$

Thus, for a QSOP-24 package Θ_{JA} = +88°C/W, the maximum allowed TAMB is given by:

$$T_{J,MAX} = T_{AMB} + PD \times \Theta_{JA} = 150°C = T_{AMB} + 0.865W \times 88°C/W \quad (EQ\ 4)$$

In this example the maximum ambient temperature must stay below 73.88°C.

8x8 Dot Matrix Mode

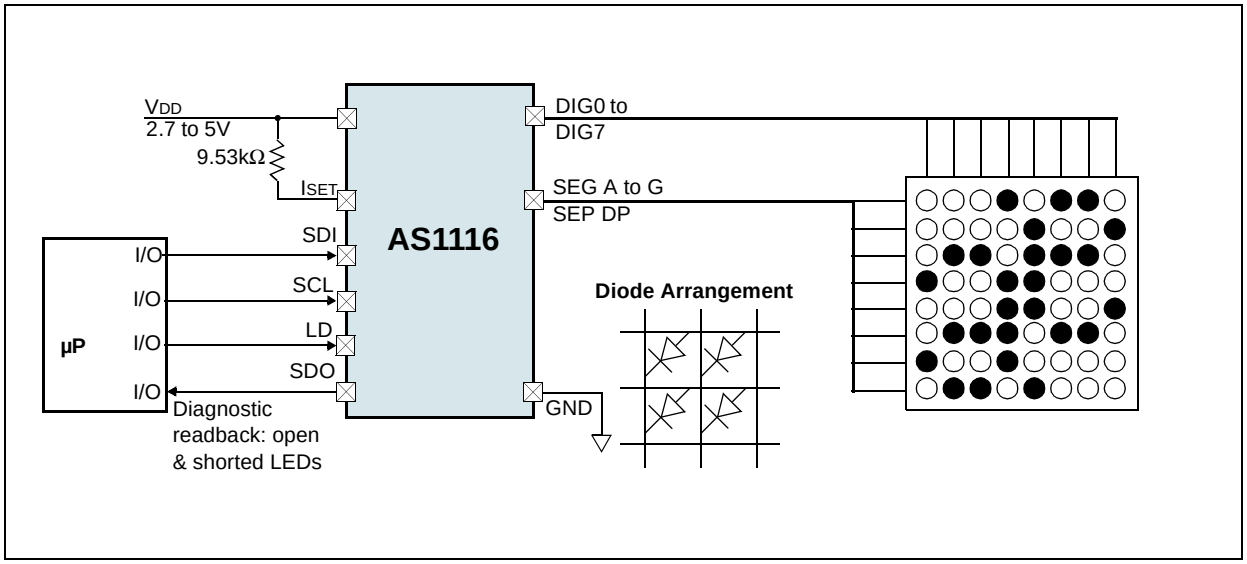
The application example in Figure 21 shows the AS1116 in the 8x8 LED dot matrix mode.

The LED columns have common cathodes and are connected to the DIG0:7 outputs. The rows are connected to the segment drivers. Each of the 64 LEDs can be addressed separately. The columns are selected via the digits as listed in Table 7 on page 11.

The Decode Enable Register (see page 12) must be set to '00000000' as described in Table 9 on page 12. Single LEDs in a column can be addressed as described in Table 12 on page 13, where bit D0 corresponds to segment G and bit D7 corresponds to segment DP.

Note: For a multiple-digit dot matrix, multiple AS1116 devices can be cascaded easily.

Figure 21. Application Example as LED Dot Matrix Driver



Supply Bypassing and Wiring

In order to achieve optimal performance the AS1116 should be placed very close to the LED display to minimize effects of electromagnetic interference and wiring inductance.

Furthermore, it is recommended to connect a 10µF electrolytic and a 0.1µF ceramic capacitor between pins VDD and GND to avoid power supply ripple (see Figure 21 on page 18).

10 Package Drawings and Markings

Figure 22. QSOP-24 Marking

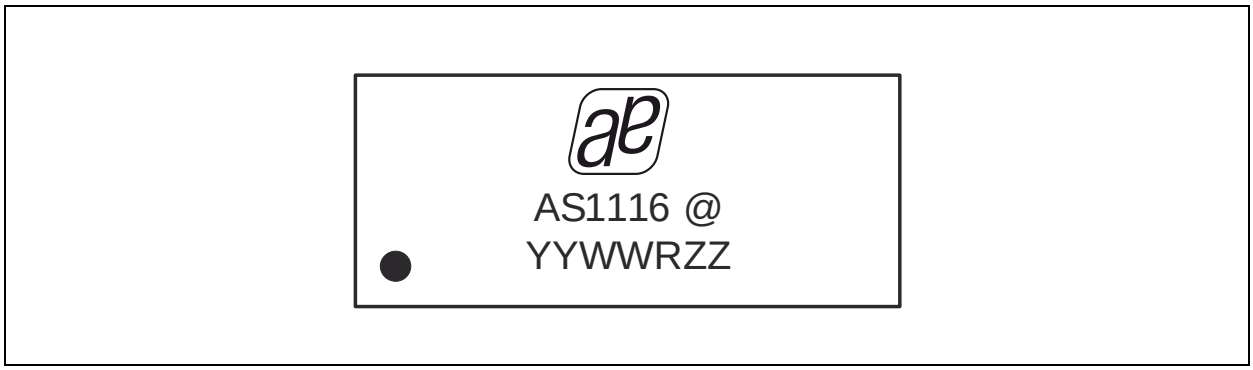
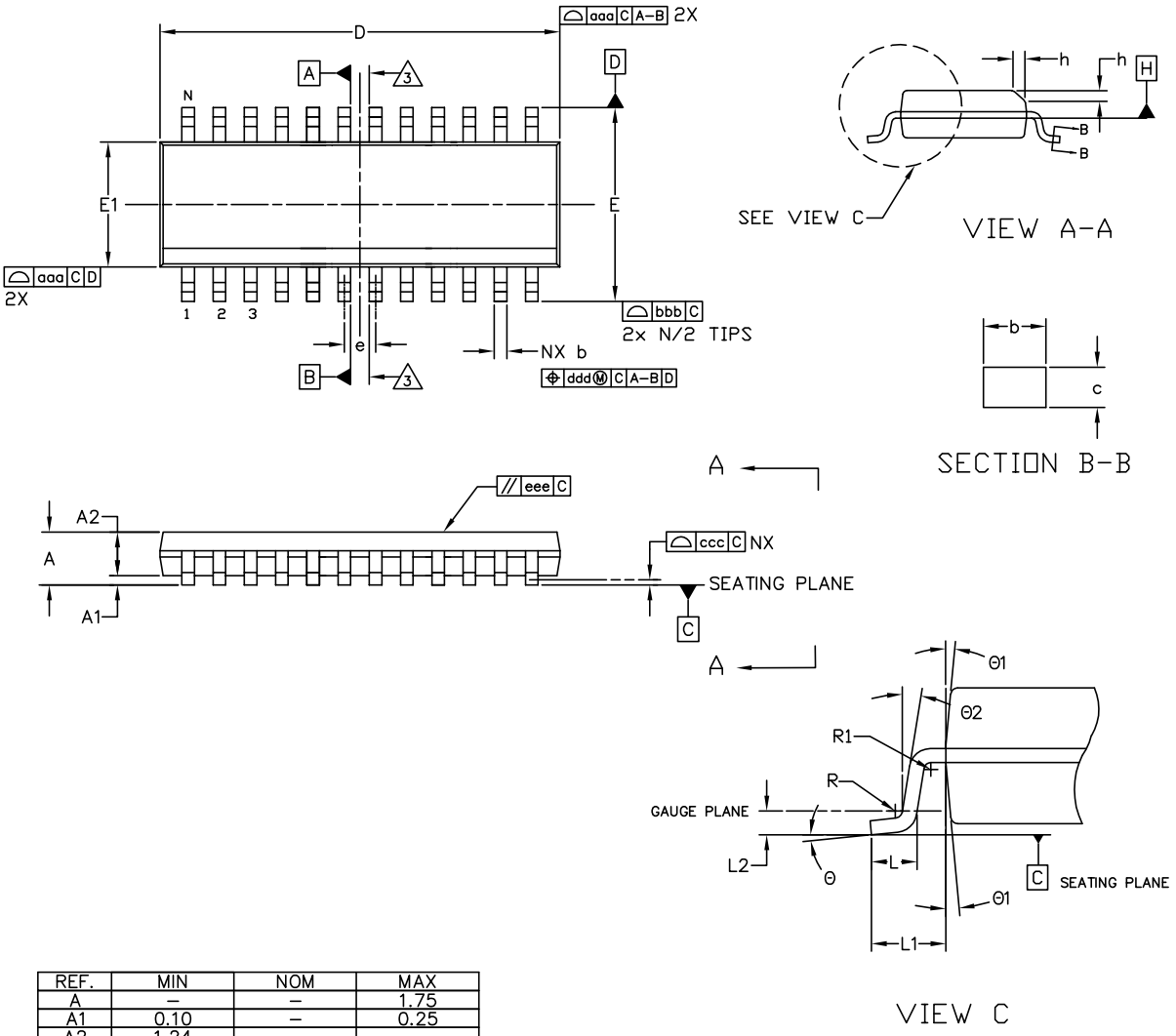


Figure 23. TQFN(4x4)-24 Marking

Table 23. Packaging Code

YY	WW	R / X	ZZ	AS1116 / ASR9	@
manufacturing year	manufacturing week	plant identifier	free choice / traceability code	marketing code	sublot identifier

Figure 24. QSOP-24 Package



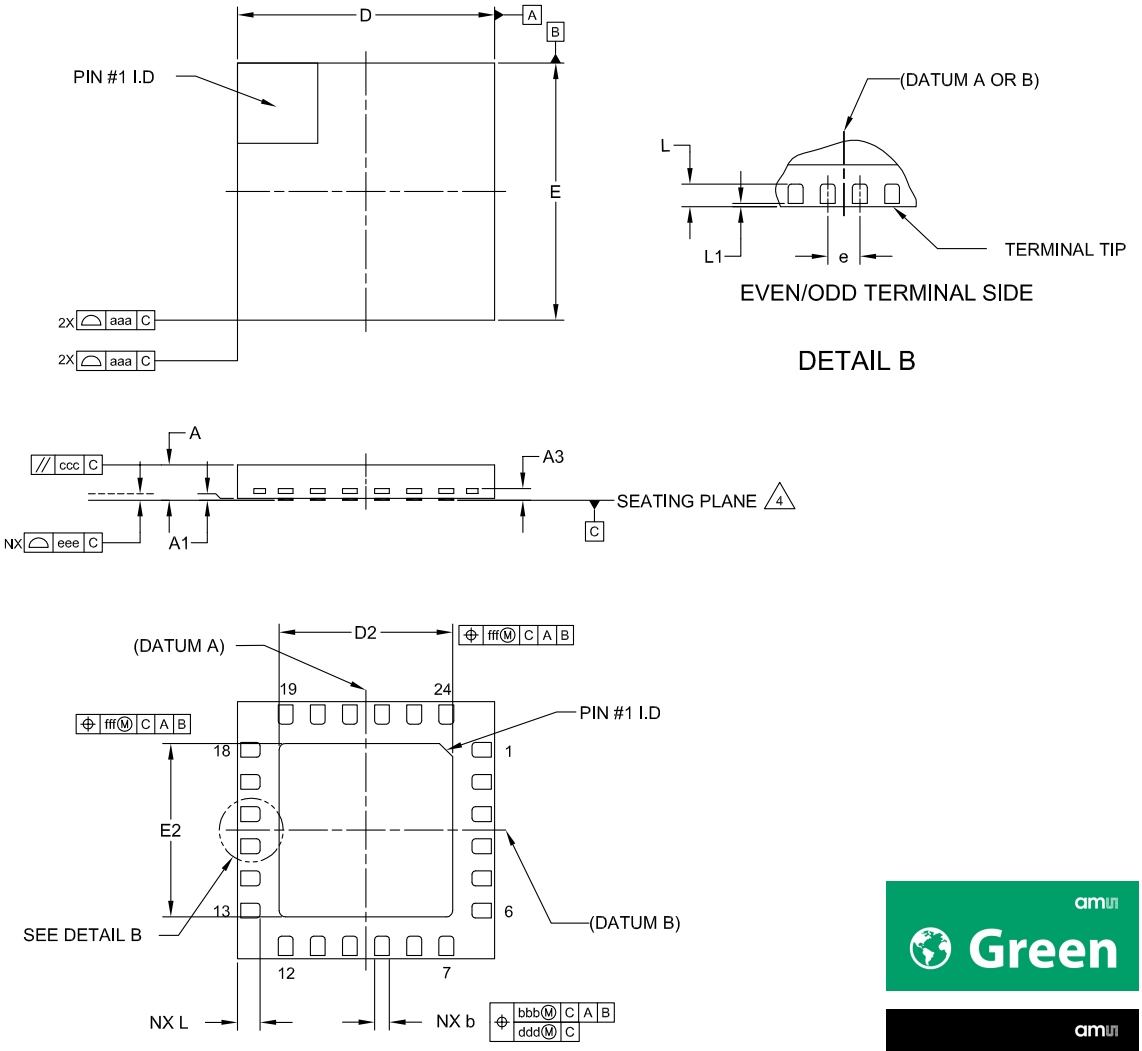
REF.	MIN	NOM	MAX
A	–	–	1.75
A1	0.10	–	0.25
A2	1.24	–	–
b	0.20	–	0.30
c	0.15	–	0.25
D		8.66 BSC	
E		6.00 BSC	
E1		3.91 BSC	
e		0.635 BSC	
L	0.41	–	1.27
L1		1.04 REF	
L2		0.25 BSC	
R	0.08	–	–
R1	0.08	–	–
h	0.25	–	0.51
θ	0°	–	8°
θ1	5°	–	15°
θ2	0°	–	–
aaa	–	0.10	–
bbb	–	0.20	–
ccc	–	0.10	–
ddd	–	0.18	–
eee	–	0.10	–
fff	–	0.15	–
N		24	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.

3 DATUMS A & B TO BE DETERMINED AT DATUM H.

Figure 25. TQFN(4x4)-24 Package



REF.	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	-	0.05
A3		0.152 REF	
L	0.30	0.35	0.40
L1	0	-	0.15
b	0.18	0.25	0.35
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
D2	2.70	2.80	2.90
E2	2.70	2.80	2.90
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		24	

NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.15mm IS ACCEPTABLE.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
5. RADIUS ON TERMINAL IS OPTIONAL.
6. N IS THE TOTAL NUMBER OF TERMINALS.

11 Ordering Information

The devices are available as the standard products shown in Table 24.

Table 24. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS1116-BSST	AS1116	64 LED Driver with Detailed Error Detection	Tape and Reel	QSOP-24
AS1116-BQFT	ASR9	64 LED Driver with Detailed Error Detection	Tape and Reel	TQFN(4x4)-24

Note: All products are RoHS compliant and ams green.
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For further information and requests, please contact us mailto:sales@ams.com
or find your local distributor at http://www.ams.com/distributor

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