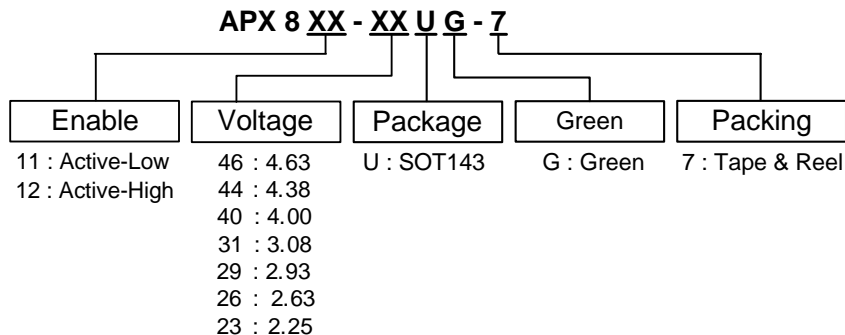


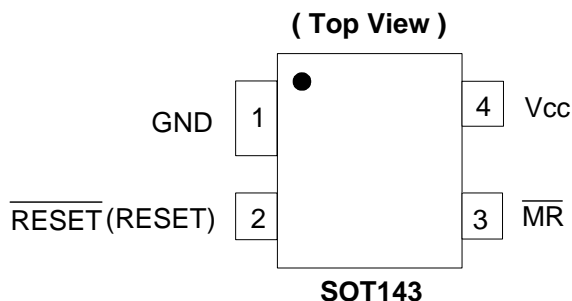
### Ordering Information



Device	Package Code	Packaging (Note 2)	7" Tape and Reel	
			Quantity	Part Number Suffix
APX811-XXUG-7	U	SOT143	3000/Tape & Reel	-7
APX812-XXUG-7	U	SOT143	3000/Tape & Reel	-7

- Notes:
1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at [http://www.diodes.com/products/lead\\_free.html](http://www.diodes.com/products/lead_free.html).
  2. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

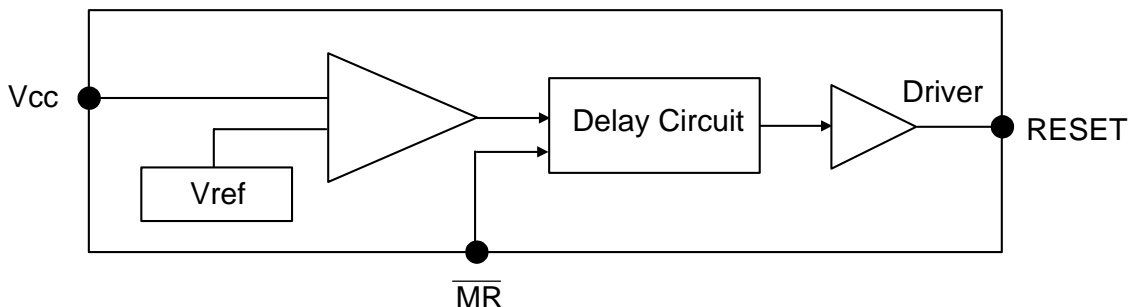
### Pin Assignments



### Pin Descriptions

Pin Name	Description
GND	Ground
RESET (RESET)	Reset output Pin L: for APX811 H: for APX812
VCC	Operating Voltage Input
MR	Manual reset (Active Low)

## Block Diagram



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD protection	3	kV
ESD MM	Machine Model ESD Protection	500	V
$V_{CC}$	Supply voltage	-0.3~7	V
$V_{RESET}$	RESET	-0.3 to ( $V_{CC}+0.3$ )	V
$I_{CC}$	Input Current, $V_{CC}$	20	mA
$I_O$	Output current	20	mA
$P_D$	Power dissipation	320	mW

## Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Supply Voltage	1.1	5.5	V
$V_{IN}$	Input Voltage	0	( $V_{CC}+0.3$ )	V
$T_A$	Operating Ambient Temperature	-40	85	°C

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$ )

$T_A = -40$  to  $85^\circ\text{C}$  unless otherwise note. Typical values are at  $T_A = +25^\circ\text{C}$ .

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{CC}$	$V_{CC}$ Range		1.0		5.5	V
$I_{CC}$	Supply Current	$V_{th} + 0.2\text{V}$		30	40	$\mu\text{A}$
$V_{th}$	Reset threshold	$T_A = 25^\circ\text{C}$ .	2.22	2.25	2.28	V
			2.59	2.63	2.67	V
			2.89	2.93	2.98	V
			3.03	3.08	3.13	V
			3.94	4.00	4.06	V
			4.31	4.38	4.45	V
			4.56	4.63	4.70	V
$t_s$	Set-up Time	$V_{CC} = V_{th}$ to $(V_{th} - 100\text{mV})$		20		$\mu\text{s}$
$V_{OL}$	RESET Output Voltage Low (APX811)	$V_{CC} = V_{th} - 0.2$ , $I_{SINK} = 1.2\text{mA}$			0.3	V
		$V_{CC} = V_{th} - 0.2$ , $I_{SINK} = 3.2\text{mA}$			0.4	
		$V_{CC} > 1.0\text{V}$ , $I_{SINK} = 50\mu\text{A}$			0.3	
$V_{OH}$	RESET Output Voltage-High (APX811)	$V_{CC} > V_{th} + 0.2$ , $I_{SOURCE} = 500\mu\text{A}$	$0.8V_{CC}$			V
		$V_{CC} > V_{th} + 0.2$ , $I_{SOURCE} = 800\mu\text{A}$	$V_{CC} - 1.5$			
$V_{OL}$	RESET Output Voltage-Low (APX812)	$V_{CC} = V_{th} + 0.2$ , $I_{SINK} = 1.2\text{mA}$			0.3	V
		$V_{CC} = V_{th} + 0.2$ , $I_{SINK} = 3.2\text{mA}$			0.4	
$V_{OH}$	RESET Output Voltage-High (APX812)	$1.8\text{V} < V_{CC} < V_{th} - 0.2$ , $I_{SOURCE} = 150\mu\text{A}$	$0.8 V_{CC}$			V
$\theta_{JA}$	Thermal Resistance Junction-to-Ambient	SOT143 (Note 3)		240		$^\circ\text{C/W}$
$\theta_{JC}$	Thermal Resistance Junction-to-Case	SOT143 (Note 3)		71		$^\circ\text{C/W}$

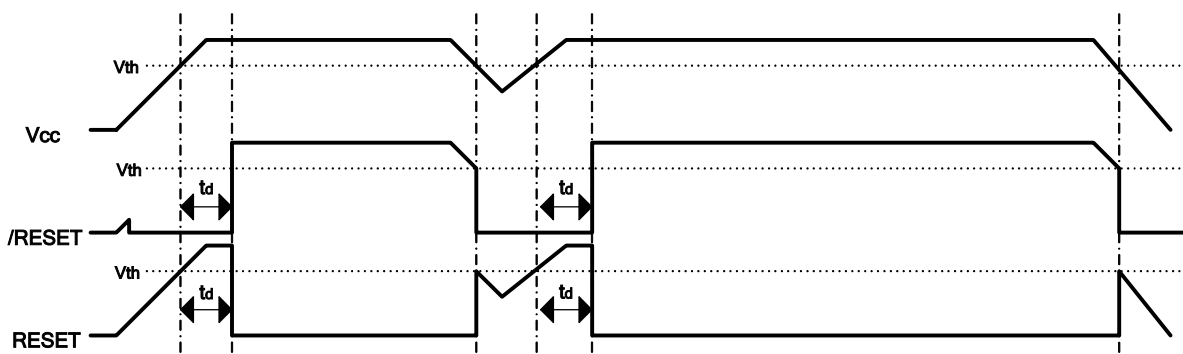
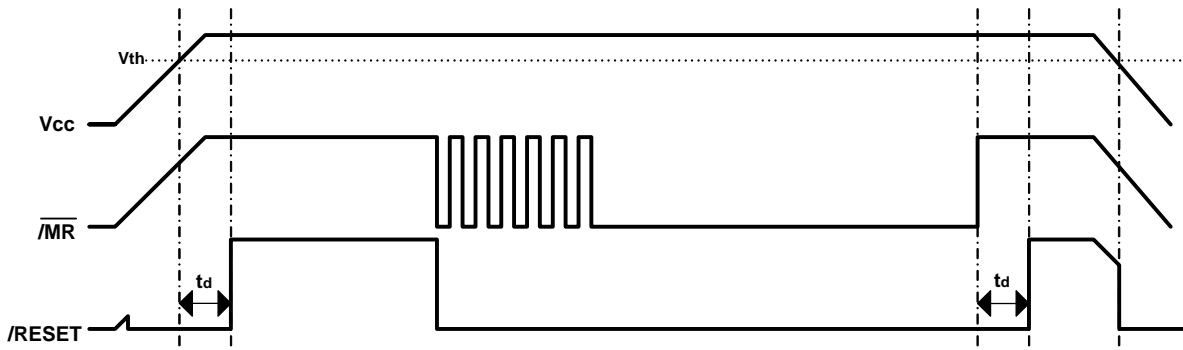
Notes: 3. Test condition for SOT143: Device mounted on FR-4 substrate, 1"×1", 2oz, copper, single-sided, PC boards.

**Timing requirements** ( $T_A = 25^\circ\text{C}$ )

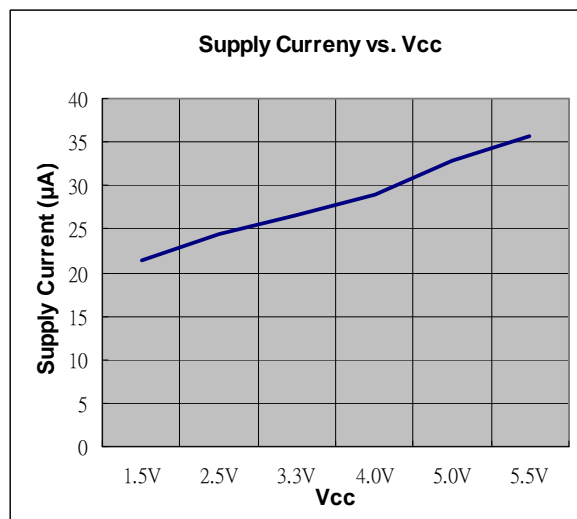
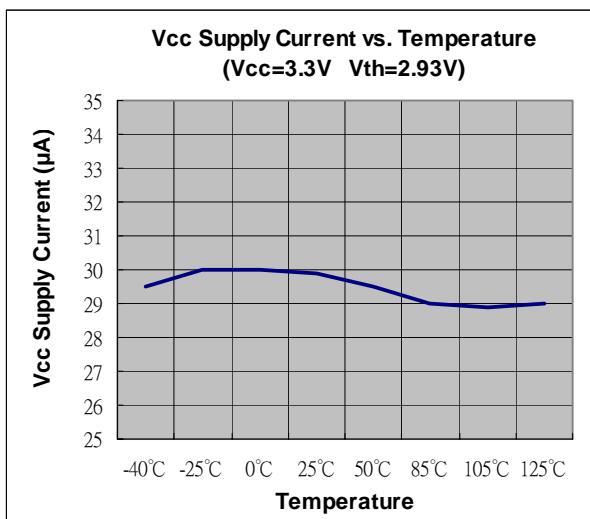
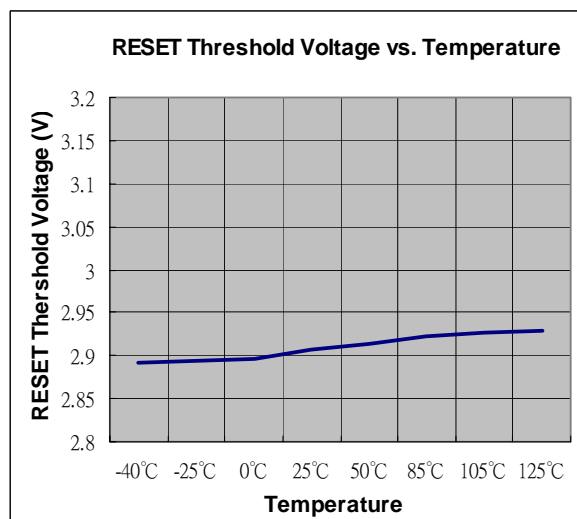
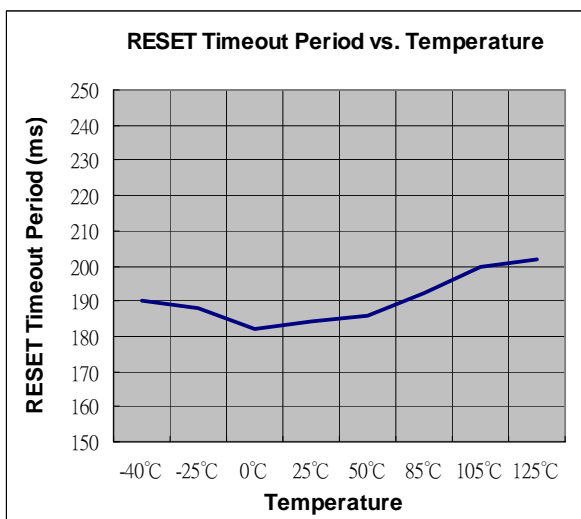
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$t_w$	Pulse Width at MR	$V_{CC} > V_{th} + 0.2\text{V}$ , $V_{IL} = 0.3 \times V_{CC}$ , $V_{IH} = 0.7 \times V_{CC}$	100	-	-	ns

**Switching Characteristics** ( $T_A=25^\circ\text{C}$ )

Symbol	Parameter		Test Conditions	Min	Typ.	Max	Unit
$t_d$	Delay Time	APX811/812	$V_{CC} > V_{th} + 0.2V$ , See timing diagram	140	200	280	ms
$t_{PHL}$	Propagation (Delay) Time, High-to-low-level Output	$\overline{MR}$ to $\overline{RESET}$ delay (APX811/812)	$V_{CC} > V_{th} + 0.2V$ , $V_{IL} = 0.3 \times V_{CC}$ , $V_{IH} = 0.7 \times V_{CC}$	-	-	0.1	$\mu\text{s}$
		$V_{CC}$ to $\overline{RESET}$ delay	$V_{IL} = V_{th} - 0.2V$ , $V_{IH} = V_{th} + 0.2V$	-	-	25	$\mu\text{s}$
$t_{PLH}$	Propagation (Delay) Time, Low-to-high-level Output	$\overline{MR}$ to $\overline{RESET}$ delay (APX811/812)	$V_{CC} > V_{th} + 0.2V$ , $V_{IL} = 0.3 \times V_{CC}$ , $V_{IH} = 0.7 \times V_{CC}$	-	-	0.1	$\mu\text{s}$
		$V_{CC}$ to $\overline{RESET}$ delay (APX811/812)	$V_{IL} = V_{th} - 0.2V$ , $V_{IH} = V_{th} + 0.2V$	-	-	25	$\mu\text{s}$

**Timing Diagram**
**RESET vs. Vcc Timing Diagram**

**RESET vs.  $\overline{MR}$  Timing Diagram**


## Typical Performance Characteristics



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### Application Information

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A microprocessor's ( $\mu$ P's) reset input starts the  $\mu$ P in a known state. The APX811/812 asserts reset to prevent code-execution errors during power-up, power-down, or brownout conditions. They assert a reset signal whenever the  $V_{CC}$  supply voltage declines below a preset threshold or the  $\overline{MR}$  pin is brought low, keeping it asserted for at least 240ms after  $V_{CC}$  has risen above the reset threshold. The APX811/812 have a push-pull output stage.

The APX811/812 reset output is guaranteed to be logic low for the APX811 and high the APX812 for  $V_{CC} > 1V$ . Once  $V_{CC}$  exceeds the reset threshold, an internal timer keeps  $\overline{RESET}$  output low (and RESET high for the APX812) for the reset timeout period. After this interval, the APX811's  $\overline{RESET}$  output goes high (APX812's RESET output goes low). If a brownout condition occurs ( $V_{CC}$  dips below the reset threshold), the APX811's  $\overline{RESET}$  output goes low (APX812's RESET output goes high). Any time  $V_{CC}$  goes below the reset threshold, the internal timer resets to zero, and  $\overline{RESET}$  goes low (RESET goes high). The internal timer starts after  $V_{CC}$  returns above the reset threshold, and  $\overline{RESET}$  remains low (RESET remains high) for the reset timeout period.

#### Ensuring a Valid Reset Output Down to $V_{CC} = 0$

When  $V_{CC}$  falls below 1V, the APX811  $\overline{RESET}$  no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to  $\overline{RESET}$  can drift to undetermined voltages. This presents no problem in most applications since most  $\mu$ P and other circuitry is inoperative with  $V_{CC}$  below 1V. However, in applications where  $\overline{RESET}$  must be valid down to 0V, adding a pull down resistor to  $\overline{RESET}$  causes any stray leakage currents to flow to ground, holding  $\overline{RESET}$  low. R1's value is not critical; 100k is large enough not to load  $\overline{RESET}$  and small enough to pull  $\overline{RESET}$  to ground.

For the APX812 if RESET is required to remain valid for  $V_{CC} < 1V$  then a 100k $\Omega$  pull-up resistor between RESET and  $V_{CC}$  is recommended.

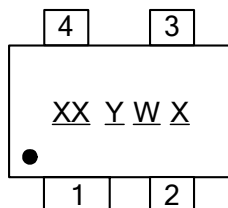
#### Benefits of Highly Accurate Reset Threshold

Most  $\mu$ P supervisor ICs has reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when the supply is 10% below nominal. When using ICs rated at only the nominal supply  $\pm 5\%$ , this leaves a zone of uncertainty where the supply is between 5% and 10% low, and where the reset may or may not be asserted.

## Marking Information

### (1) SOT143

( Top View )



XX : Identification code

Y : Year 0~9

W : Week : A~Z : 1~26 week;  
a~z : 27~52 week; z represents  
52 and 53 week

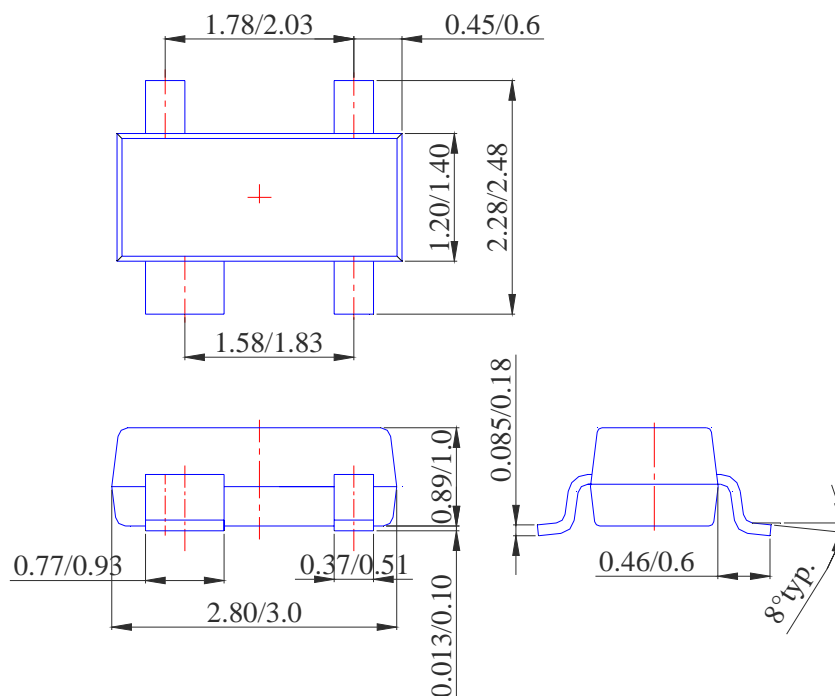
X : A~Z : Green

Device	Package	Identification Code
APX811-46U	SOT143	C2
APX811-44U	SOT143	C3
APX811-40U	SOT143	C4
APX811-31U	SOT143	C5
APX811-29U	SOT143	C6
APX811-26U	SOT143	C7
APX811-23U	SOT143	C8
APX812-46U	SOT143	C9
APX812-44U	SOT143	CA
APX812-40U	SOT143	CB
APX812-31U	SOT143	CC
APX812-29U	SOT143	CD
APX812-26U	SOT143	CE
APX812-23U	SOT143	CF

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**Package Information** (All Dimensions in mm)

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**(1) Package Type: SOT143**



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