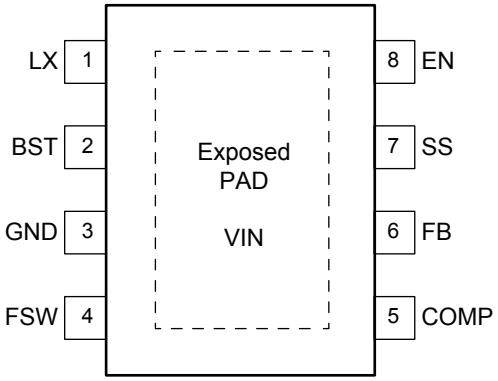
Ordering Information

Part Number	Temperature Range	Package	Environmental
AOZ1284PI	-40°C to +85°C	EPAD SO-8	Green Product
AOZ1284PI-1			

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

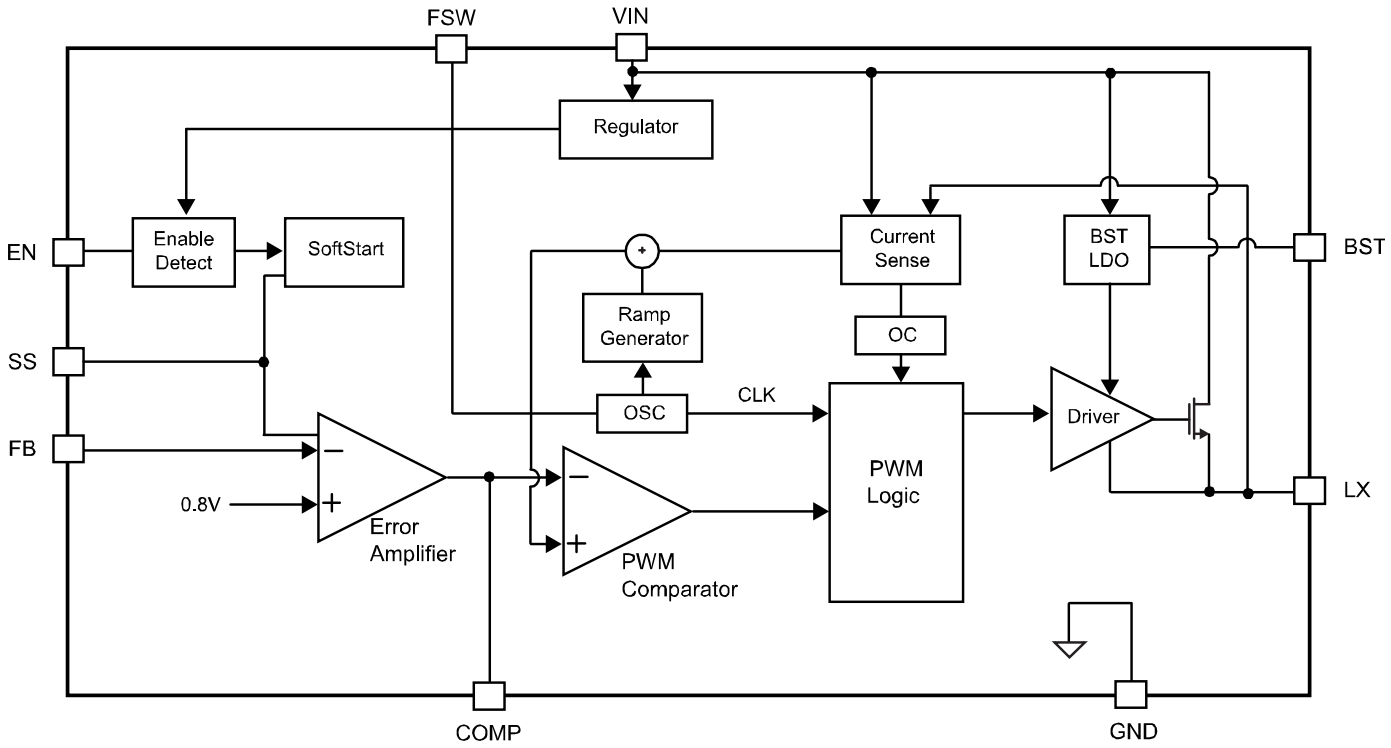


EPAD SO-8
(Top View)

Pin Description

Part Number	Pin Name	Pin Function
1	LX	PWM Output Pin. Connect to inductor.
2	BST	Bootstrap Voltage Pin. Driver supply for High Side NMOS. Connected to 100nF capacitor between BST and LX.
3	GND	Ground Pin.
4	FSW	Frequency Bias Pin. Connect to resistor to determine switching frequency.
5	COMP	Compensation Pin. Connect to Resistor and Capacitor for system stability.
6	FB	Feedback Pin. It is regulated to 0.8V. The FB pin is used to determine the PWM output voltage via a resistor divider between the Output and Ground.
7	SS	Soft Start Pin.
8	EN	Enable Pin.
Exposed PAD	VIN	Supply Voltage Pin.

Functional Block



Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
Supply Voltage (V_{IN})	40V
LX to GND	-0.7V to V_{IN}+0.3V
EN, SS, FB and COMP to GND	-0.3V to +6V
BST to GND	-0.3V to V_{LX}+6V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating HB Model[1]	2kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Ratings

This device is not guaranteed to operate beyond the Recommended Operating Ratings.

Parameter	Rating
Supply Voltage (V_{IN})	3.0V to 36V
Output Voltage (V_{OUT})	0.8V to V_{IN}*0.85V
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance	
EPAD SO-8 (θ_{JA})	50°C/W

Electrical Characteristics

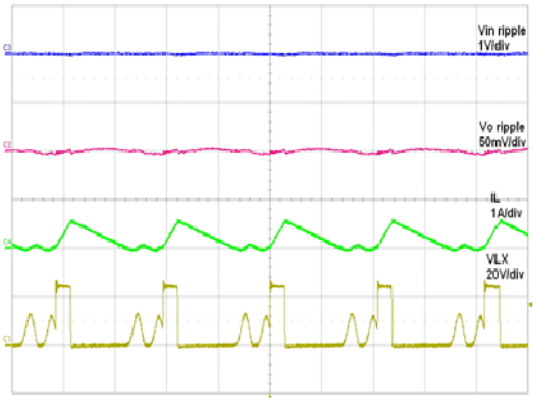
T_A = 25°C, V_{IN} = 12V, V_{EN} = 3V, V_{OUT} = 3.3V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40 °C to +85 °C.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IN}	Supply Voltage		**3**		**36**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	V_{IN} rising V_{IN} falling	 2.3		2.9	V
I_{IN}	Supply Current (Quiescent)	I_{OUT} = 0, V_{FB} = 1V, V_{EN} >1.2V		**1**	**1.5**	mA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0V			10	µA
V_{FB}	Feedback Voltage	T_A=25°C	788	800	812	mV
V_{FB_LOAD}	Load Regulation	0.4A < Load < 3.6A		0.5		**%**
V_{FB_LINE}	Line Regulation	Io=2A		0.03		**%**/V
I_{FB}	Feedback Voltage Input Current	V_{FB} = 800mV		0.5	1	µA
Enable						
V_{EN_OFF} V_{EN_ON}	EN Input Threshold	Off threshold On threshold	 **1.2**		**0.4**	V
V_{EN_HYS}	EN Input Hysteresis			200		mV
Current Limit						
	Peak Current Limit	1284	5	6		A
		1284-1	5.5	6.5		
Soft Start (SS)						
I_{SS}	Soft Start Source Current		2	2.5	3	µA
Modulator						
f_O	Frequency	RF = 270kΩ RF = 46.6kΩ	160 0.8	200 1	240 1.2	kHz MHz
D_{MAX}	Maximum Duty Cycle	f_O = 1MHz		87		%
T_{ON_MIN}	Minimum On Time			150		ns
G_{VEA}	Error Amplifier Voltage Gain			500		V/V
G_{EA}	Error Amplifier Transconductance			170		µA/V
G_{CS}	Current Sense Circuit Transconductance,			4.5		A/V
Power Stage Output						
$I_{LEAKAGE}$	NMOS Leakage	V_{EN}=0V, V_{LX}=0V			10	µA
R_{DSON1}	NMOS On- Resistance			50	70	mΩ
Thermal Protection						
T_{SD}	Thermal Shutdown Threshold			145		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			45		°C

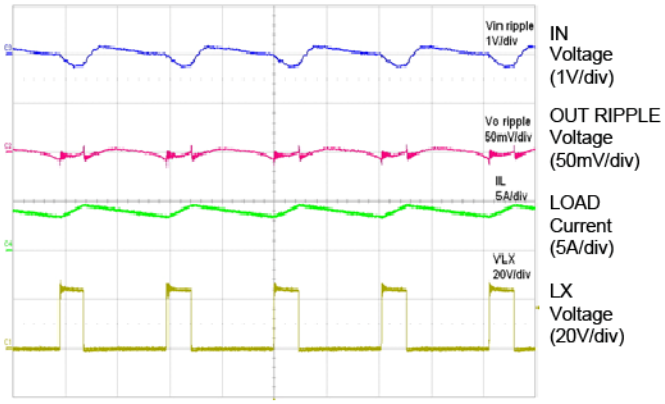
Typical Performance Characteristics

T_A = 25°C, V_{IN} = 24V, V_{EN} = 5V, V_{OUT} = 5V, unless otherwise specified.

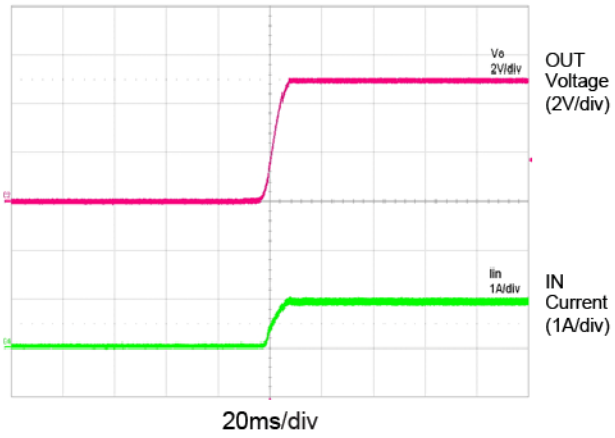
Light Load Operation



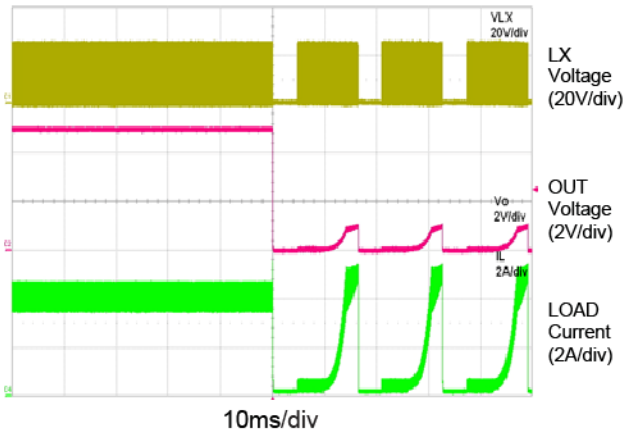
Full Load Operation



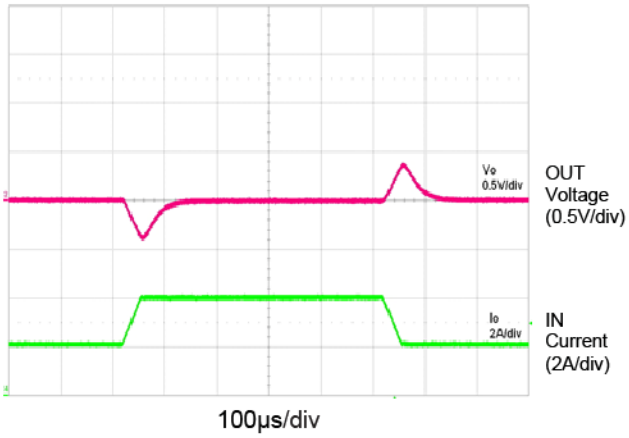
Start Up to Full Load



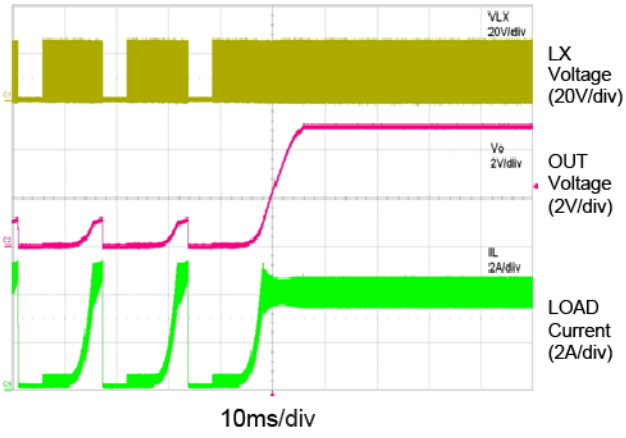
Short Circuit Protection



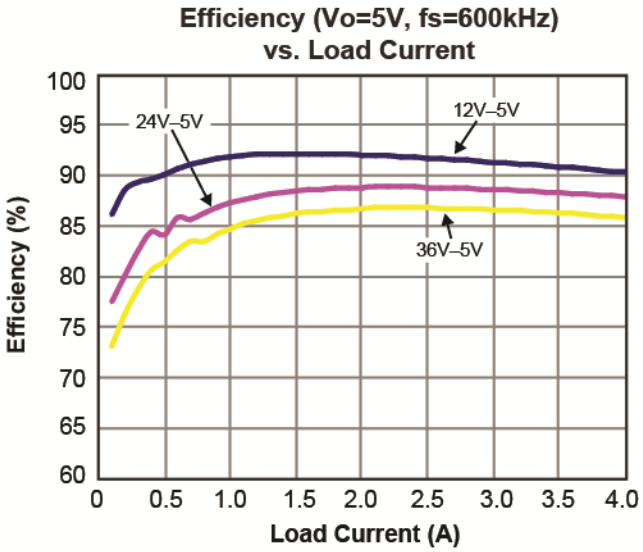
50% to 100% Load Transient

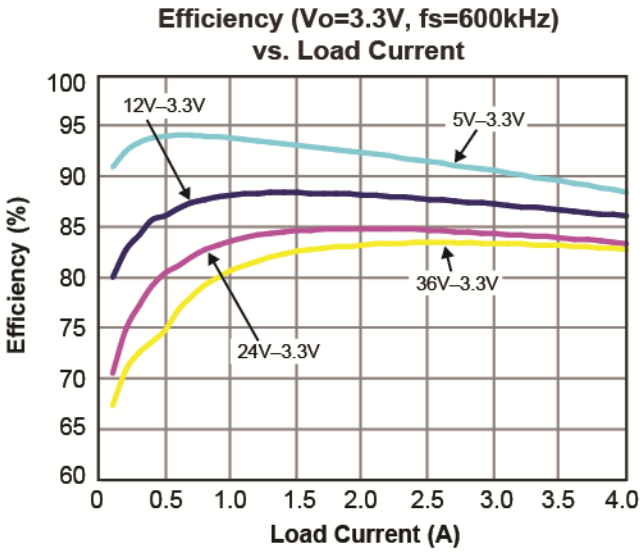


Short Circuit Recovery



Efficiency Curves





Detailed Description

The AOZ1284 is a current-mode step down regulator with integrated high side NMOS switch. It operates from a 3V to 36V input voltage range and supplies up to 4A of load current. Features include enable control, Power-On Reset, input under voltage lockout, external soft-start and thermal shut down.

The AOZ1284 is available in EPAD SO-8 package.

Enable and Soft Start

The AOZ1284 has external soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 3V and voltage on EN pin is HIGH. In soft start process, a 2.5μA internal current source charges the external capacitor at SS. As the SS capacitor is charged, the voltage at SS rises. The SS voltage clamps the reference voltage of the error amplifier, therefore output voltage rising time follows the SS pin voltage. With the slow ramping up output voltage, the inrush current can be prevented. Minimum external soft-start capacitor 850pF is required, and the corresponding soft-start time is about 200μs.

The EN pin of the AOZ1284 is active high. Connect the EN pin to a voltage between 1.2V to 5V if enable function is not used. Pull it to ground will disable the AOZ1284. Do not leave it open. The voltage on EN pin must be above 1.2V to enable the AOZ1284. When voltage on EN pin falls below 0.4V, the AOZ1284 is disabled. If an application circuit requires the AOZ1284 to be disabled, an open drain or open collector circuit should be used to interface to EN pin.

Steady-State Operation

Under steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ1284 integrates an internal N-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Since the N-MOSFET requires a gate voltage higher than the input voltage, a boost capacitor connected between LX pin and BST pin drives the gate. The boost capacitor is charged while LX is low. An internal 10Ω switch from LX to GND is used to insure that LX is pulled to GND even in the light load. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the Schottky diode to output.

Switching Frequency

The AOZ1284 switching frequency can be programmed by external resistor. External resistor value can be calculated by following formula.

$$RF(k\Omega) = \frac{50000}{f_O(kHz)} - 5k\Omega$$

Some standard values of RF for most commonly used switching frequency are listed in Table 1.

f_O(Hz)	RF (kΩ)
200k	270
500k	100
1M	46.6

Table 1

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin with a resistor divider network. In the application circuit shown in Figure 1 (Typical Application). The resistor divider network includes R_2 and R_3. Usually, a design is started by picking a fixed R_3 value and calculating the required R_2 with equation below.

$$V_O = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Some standard value of R_1, R_2 for most commonly used output voltage values are listed below in Table 2.

V_O (V)	R1 (kΩ)	R2 (kΩ)
0.8	1.0	Open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.6	10
5.0	52.3	10

Table 2

Combination of R_1 and R_2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Protection Features

The AOZ1284 has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1284 employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0.4V and 2.5V internally. The peak inductor current is automatically limited cycle by cycle.

The cycle by cycle current limit threshold is internally set. When the load current reaches the current limit threshold, the cycle by cycle current limit circuit turns off the high side switch immediately to terminate the current duty cycle. The inductor current stop rising. The cycle by cycle current limit protection directly limits inductor peak current. The average inductor current is also limited due to the limitation on peak inductor current. When cycle by cycle current limit circuit is triggered, the output voltage drops as the duty cycle decreasing.

The AOZ1284 has internal short circuit protection to protect itself from catastrophic failure under output short circuit conditions. The FB pin voltage is proportional to the output voltage. Whenever FB pin voltage is below 0.2V, the short circuit protection circuit is triggered.

Power-On Reset (POR)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds 2.9V, the converter starts operation. When input voltage falls below 2.3V, the converter will stop switching.

Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and high side NMOS if the junction temperature exceeds 145ºC. The regulator will restart automatically under the control of soft-start circuit when the junction temperature decreases to 100ºC.

Application Information

The basic AOZ1284 application circuit is shown in Figure 1. Component selection is explained below.

Input capacitor

The input capacitor (C_1 in Figure 1) must be connected to the V_{IN} pin and GND pin of the AOZ1284 to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

if let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown below in Figure 2. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_O$.

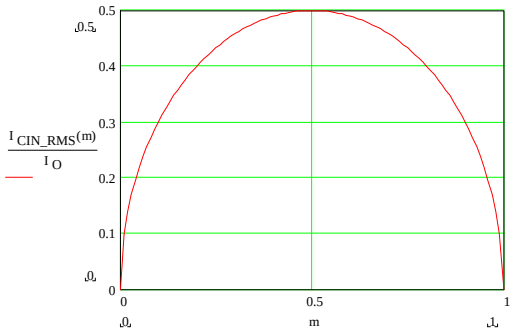


Figure 2. I_{CIN} vs. Voltage conversion ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN-RMS}$ at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{LPEAK} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Wurth, Sumida, Coilcraft, and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O}\right)$$

where;

C_O is output capacitor value and

ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Schottky Diode Selection

The external freewheeling diode supplies the current to the inductor when the high side NMOS switch is off. To reduce the losses due to the forward voltage drop and recovery of diode, Schottky diode is recommended to use. The maximum reverse voltage rating of the chosen Schottky diode should be greater than the maximum input voltage, and the current rating should be greater than the maximum load current.

Low Input operation

When V_{IN} is lower than 4.5V, such as 3.0V, an external 5V is required to add into the BST pin for proper operation.

Loop Compensation

The AOZ1284 employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole and can be calculated by:

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where;

C_O is the output filter capacitor;

R_L is load resistor value and

ESR_{CO} is the equivalent series resistance of output capacitor.

The compensation design is actually to shape the converter close loop transfer function to get desired gain and phase. Several different types of compensation network can be used for AOZ1284. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1284, FB pin and COMP pin are the inverting input and the output of internal transconductance error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

where;

G_{EA} is the error amplifier transconductance, which is $200 \cdot 10^{-6}$ A/V;

G_{VEA} is the error amplifier voltage gain, which is 500 V/V and

C_C is compensation capacitor.

The zero given by the external compensation network, capacitor C_C (C_5 in Figure 1) and resistor R_C (R_1 in Figure 1), is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover frequency is also called the converter bandwidth. Generally a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high due to system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be less than 1/10 of switching frequency.

The strategy for choosing R_C and C_C is to set the cross over frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_O}{G_{EA} \times G_{CS}}$$

where;

f_C is desired crossover frequency;

V_{FB} is 0.8V;

G_{EA} is the error amplifier transconductance, which is $200 \cdot 10^{-6}$ A/V and

G_{CS} is the current sense circuit transconductance, which is 4.5 A/V.

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected crossover frequency. C_C can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{P1}}$$

Equation above can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

Easy to use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Thermal management and layout consideration

In the AOZ1284 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the GND pin of the AOZ1284, to the LX pins of the AOZ1284. Current flows in the second loop when the low side diode is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is recommended to connect input capacitor, output capacitor, and GND pin of the AOZ1284.

In the AOZ1284 buck regulator circuit, the three major power dissipating components are the AOZ1284, external diode and output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \cdot I_{IN} - V_O \cdot I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor.

$$P_{inductor\_loss} = I_O^2 \cdot R_{inductor} \cdot 1.1$$

The power dissipation of diode is

$$P_{diode\_loss} = I_O \cdot V_F \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$$

The actual AOZ1284 junction temperature can be calculated with power dissipation in the AOZ1284 and thermal impedance from junction to ambient.

$$T_{junction} = \frac{\left(P_{total\_loss} - P_{inductor\_loss} - P_{diode\_loss}\right)}{\Theta_{JA}} + T_{ambient}$$

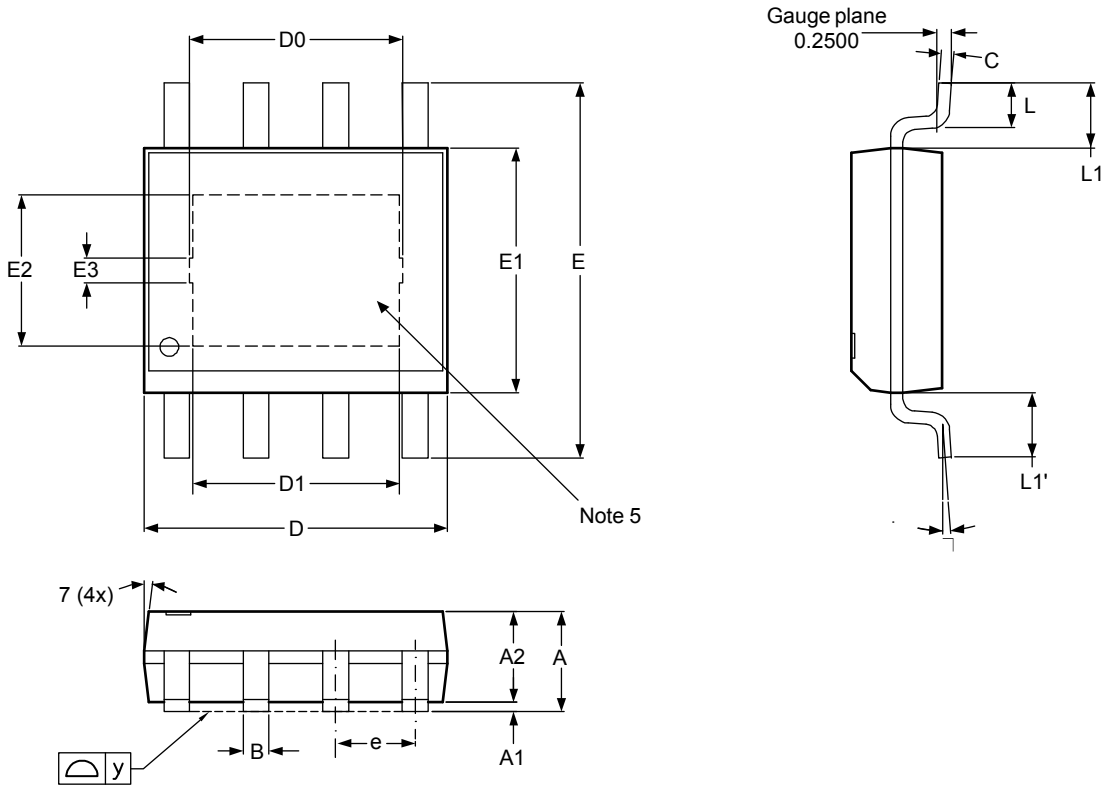
The maximum junction temperature of AOZ1284 is 145ºC, which limits the maximum load current capability.

The thermal performance of the AOZ1284 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

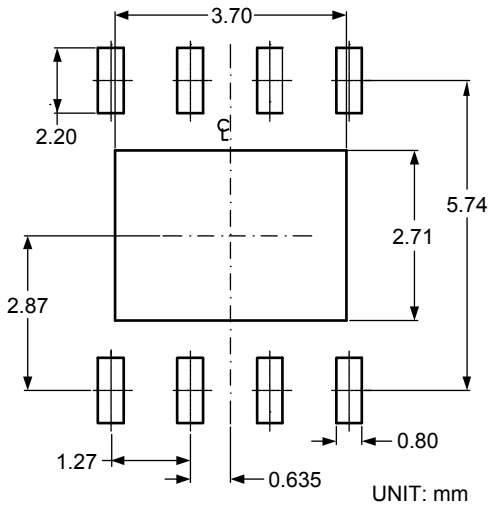
Several layout tips are listed below for the best electric and thermal performance. The Figure 3 (a) and (b) give the example of layout for AOZ1284A and AOZ1284D respectively.

1. Do not use thermal relief connection to the VIN and the GND pin. Pour a maximized copper area to the GND pin and the VIN pin to help thermal dissipation.
2. Input capacitor should be connected to the VIN pin and the GND pin as close as possible.
3. Make the current trace from LX pins to L to Co to the GND as short as possible.
4. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
5. Keep sensitive signal trace such as trace connected with FB pin and COMP pin far away from the LX pins.

Package Dimensions, SO-8 EP1



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.40	1.55	1.70
A1	0.00	0.05	0.10
A2	1.40	1.50	1.60
B	0.31	0.406	0.51
C	0.17	—	0.25
D	4.80	4.96	5.00
D0	3.20	3.40	3.60
D1	3.10	3.30	3.50
E	5.80	6.00	6.20
e	—	1.27	—
E1	3.80	3.90	4.00
E2	2.21	2.41	2.61
E3	0.40 REF		
L	0.40	0.95	1.27
y	—	—	0.10
⌟	0°	3°	8°
| L1–L1' |	—	0.04	0.12
L1	1.04 REF		

Dimensions in inches

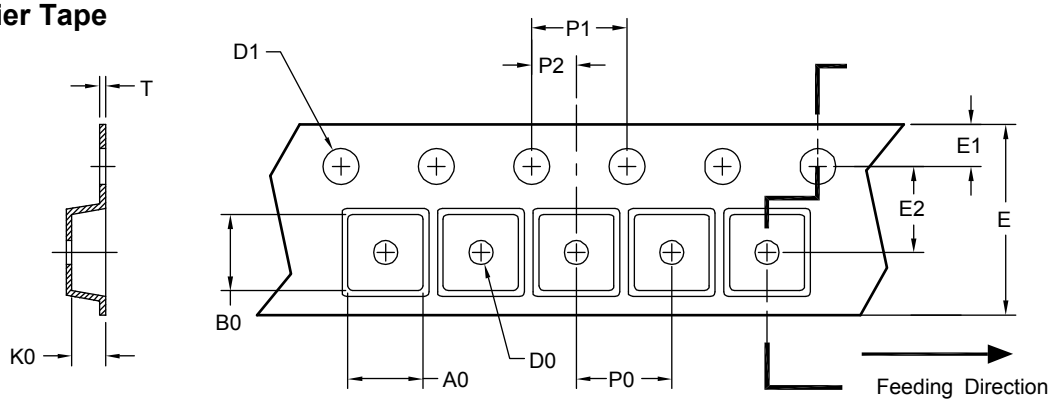
Symbols	Min.	Nom.	Max.
A	0.055	0.061	0.067
A1	0.000	0.002	0.004
A2	0.055	0.059	0.063
B	0.012	0.016	0.020
C	0.007	—	0.010
D	0.189	0.195	0.197
D0	0.126	0.134	0.142
D1	0.122	0.130	0.138
E	0.228	0.236	0.244
e	—	0.050	—
E1	0.150	0.153	0.157
E2	0.087	0.095	0.103
E3	0.016 REF		
L	0.016	0.037	0.050
y	—	—	0.004
⌟	0°	3°	8°
| L1–L1' |	—	0.002	0.005
L1	0.041 REF		

Notes:

1. Package body sizes exclude mold flash and gate burrs.
2. Dimension L is measured in gauge plane.
3. Tolerance 0.10mm unless otherwise specified.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
5. Die pad exposure size is according to lead frame design.
6. Followed from JEDEC MS-012

Tape and Reel Dimensions, SO-8 EP1

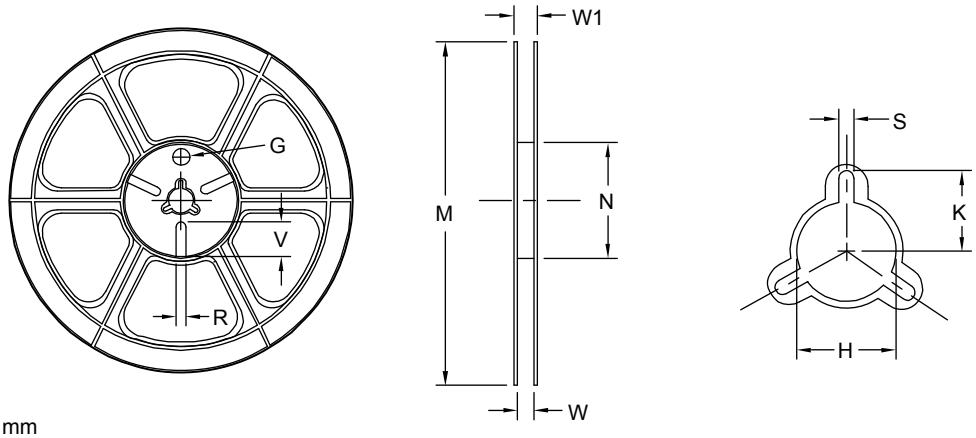
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SO-8 (12mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 ±0.10	12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.10

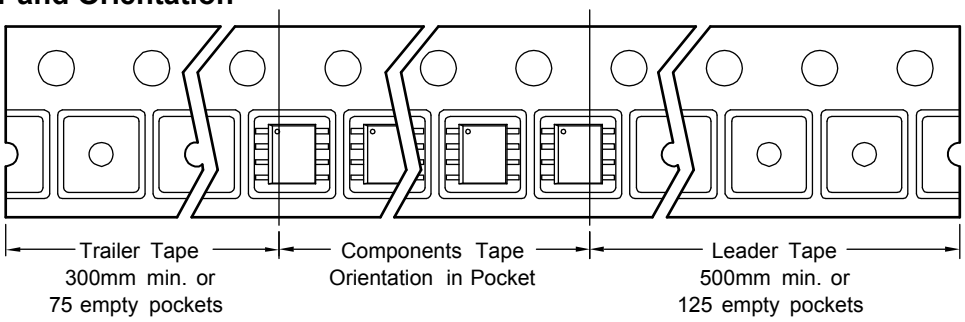
Reel



UNIT: mm

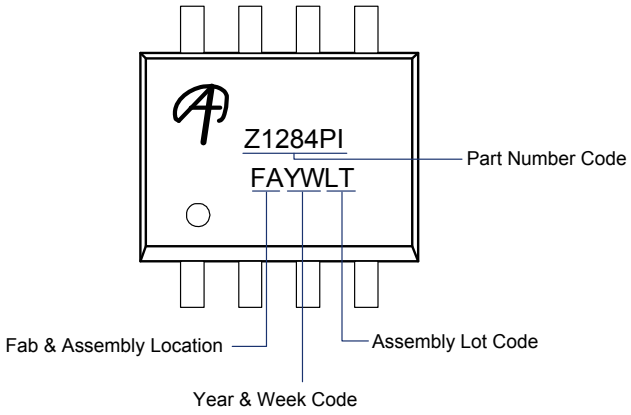
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

Leader/Trailer and Orientation

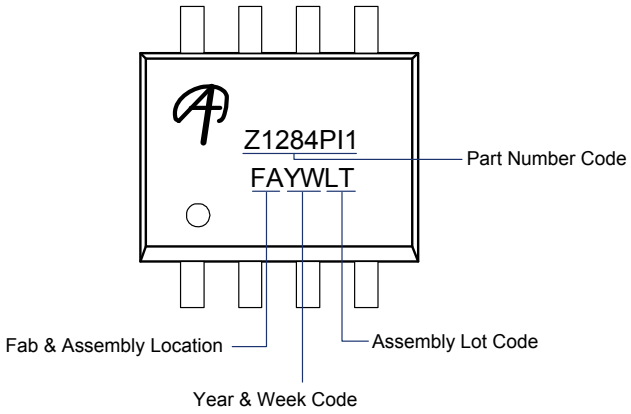


Part Marking

AOZ1284PI
(SO-8)



AOZ1284PI-1
(SO-8)



This datasheet contains preliminary data; supplementary data may be published at a later date.
Alpha and Omega Semiconductor reserves the right to make changes at any time without notice.

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.