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REVISION HISTORY

12/06—Rev. 0 to Rev. A

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Added Table 3 ... 5
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7/06—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 5 V, R_{FREQ} = 100 kΩ, f_{OSC} = 200 kHz, T_J = −40°C to 125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
MAIN CONTROL LOOP						
Internal Soft Start Time	t_{SS}			2048		Cycles
PIN Supply Voltage[1]	V_{PIN}		2.9		V_{SHUNT}	V
IN Supply Voltage[1]	V_{IN}		2.9		V_{SHUNT}	V
Shunt Regulation Voltage	V_{SHUNT}	I_{IN} = 3 mA, I_{PIN} = 3 mA, T_A = 25°C	5.4	5.6	5.7	V
		I_{IN} = 3 mA, I_{PIN} = 3 mA	5.2	5.6	6.0	V
Shunt Resistance	R_{SHUNT}	Current into IN = 8 mA to 12 mA		13		Ω
		Current into PIN = 8 mA to 12 mA		7		Ω
IN Quiescent Current	I_{IN}	V_{IN} = 2.9 V to 5.5 V, V_{FB} = 1.215 V		1.8	3	mA
IN Shutdown Current		V_{IN} = 2.9 V to 5.5 V, SDSN = GND		1	10	µA
PIN Supply Current	I_{PIN}					
Static Mode, No Switching		V_{FB} = 1.3 V, V_{COMP} < $V_{COMP,ZCT}$, GATE = 0 V		1	10	µA
Shutdown Mode		SDSN = GND		1	10	µA
Undervoltage Lockout Threshold at IN Pin	V_{UVLO}	V_{UVLO} rising	2.2	2.5	2.8	V
		V_{UVLO} hysteresis		−80		mV
FB Regulation Voltage	V_{FB}	T_A = 25°C	1.203	1.215	1.227	V
			1.197	1.215	1.233	V
FB Input Current	I_{FB}	V_{FB} = 1.215 V, T_A = 25°C	−75	+25	+75	nA
Line Regulation[2]	$\Delta V_{FB}/\Delta V_{IN}$	2.9 V ≤ V_{IN} ≤ 5 V, T_J = −40°C to +85°C		0.02	0.06	%/V
		2.9 V ≤ V_{IN} ≤ 5 V, T_J = −40°C to +125°C		0.02	0.072	%/V
Load Regulation[3]	$\Delta V_{FB}/\Delta V_{COMP}$	V_{COMP} = 1.4 V to 1.5 V	−1	−0.1		%
Error Amplifier Transconductance	g_m			300		µS
COMP Zero-Current Threshold	$V_{COMP,ZCT}$		0.85	1.0	1.15	V
COMP Clamp High Voltage	$V_{COMP,CLAMP}$	T_J = −40°C to +85°C	1.9	2.0	2.1	V
		T_J = −40°C to +125°C	1.9	2.0	2.2	V
Current-Sense Amplifier Gain	n		7.5	9.5	11.5	V/V
Peak Slope-Compensation Current at CS Pin[4]	$I_{SC,PK}$	V_{CS} = 0 V to 100 mV maximum across R_S (GATE high)	55	70	85	µA
CS Pin Leakage Current	$I_{CS,LEAK}$	V_{CS} = 30 V (GATE low)			5	µA
Shutdown Time	t_{SD}	SDSN pin from high to low or left floating		50		µs
Thermal Shutdown Threshold[5]	T_{TMSD}			150		°C
Thermal Shutdown Hysteresis[5]				−10		°C
OSCILLATOR						
Oscillator Frequency Range[6]	f_{OSC}		100		1500	kHz
Oscillator Frequency	f_{OSC}	R_{FREQ} = 65 kΩ, T_A = 25°C	255	325	395	kHz
Oscillator Frequency Tempco	$f_{OSC,TC}$			±0.06		%/°C
SDSN Input Level Threshold	$V_{SDSN,THRESH}$	V_{IN} = V_{PIN} = 5 V	1.5	1.7	1.9	V
SDSN Threshold Hysteresis				−0.19		V
SDSN Internal Pull-Down Resistor	R_{SDSN}			100		kΩ
Synchronization Minimum Pulse Width	$t_{SYNC,MIN}$	V_{SDSN} = 0 V to V_{IN}		45	100	ns
Synchronization Maximum Pulse Width	$t_{SYNC,MAX}$	V_{SDSN} = 0 V to V_{IN}		0.8/f_{SYNC}		ns
Synchronization Frequency	f_{SYNC}		110		1800	kHz
GATE Minimum On Time	$t_{ON,MIN}$	V_{FB} = 1.215 V, V_{COMP} = 1.0 V		180	215	ns
GATE Minimum Off Time	$t_{OFF,MIN}$	V_{FB} = 1.215 V, V_{COMP} = 2.0 V		190	230	ns
Maximum Duty Cycle[6, 7]	D_{MAX}	f_{SW} = 200 kHz, R_{FREQ} = 100 kΩ	93		97	%
Recommended Maximum Synchronized Frequency Ratio[6, 8]	f_{SYNC}/f_{OSC}	f_{OSC} = 200 kHz, R_{FREQ} = 100 kΩ, f_{SYNC} = f_{SW}	1.1	1.2	1.4	

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GATE DRIVER						
GATE Rise Time[9]	t_R	C_{GATE} = 3.3 nF		17		ns
GATE Fall Time[9]	t_F	C_{GATE} = 3.3 nF		13		ns

[1] The maximum input voltage is the shunt regulation voltage, which is typically 5.5 V and can range from 5.3 V to 6.0 V over the specified temperature range.
[2] The ADP1621 is tested in a feedback servo loop, which servos V_{FB} to the internal reference voltage. The voltage change in FB is measured while V_{IN} is changed from 2.9 V to 5 V. The line regulation is calculated by $(\Delta V_{FB}/V_{FB}) \times 100\%/\Delta V_{IN}$.
[3] The ADP1621 is tested in a feedback servo loop, which servos V_{FB} to the internal reference voltage, and V_{COMP} is forced from 1.4 V to 1.5 V. The V_{COMP} range is $(1.0\ V \le V_{COMP} \le 2.0\ V)$.
[4] The peak slope-compensation current at the CS pin is typically 70 µA, and effectively clamped at 116 mV. Thus, R_S should not exceed 1.6 kΩ (116 mV/70 µA).
[5] Guaranteed by design for thermal shutdown. When the thermal junction temperature of the ADP1621 reaches approximately 150°C, the ADP1621 goes into thermal shutdown and the GATE voltage is pulled low. When the junction temperature drops below about 140°C, the soft start sequence is initiated and the ADP1621 resumes normal operation.
[6] f_{OSC} is the natural oscillation frequency, f_{SYNC} is the synchronization frequency, and f_{SW} is the switching frequency. If synchronization is used, then $f_{SW} = f_{SYNC}$; otherwise, $f_{SW} = f_{OSC}$.
[7] Guaranteed by design and bench characterization.
[8] To ensure proper synchronization operation, set the synchronization frequency, f_{SYNC}, to 1.2× of the free-running frequency, f_{OSC}. Although the switching frequency can be synchronized to as high as 1.8 MHz, the peak slope-compensation current decreases at higher synchronization frequencies. It is recommended that the maximum f_{SYNC} be less than 1.4× of f_{OSC} and should not exceed 1.8 MHz. The slope-compensation resistor, R_S, should be chosen for the synchronization frequency (see the Slope Compensation section in the Application Information: Boost Converter section).
[9] GATE rise and fall times are measured from 10% to 90% levels.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
IN to GND	−0.3 V to V_{SHUNT}
FB, COMP, SDSN, FREQ, GATE to GND	−0.3 V to (V_{IN} + 0.3 V)
CS to GND	−5 V to +33 V
PIN to PGND	−0.3 V to V_{SHUNT}
Supply Current into IN	25 mA
Supply Current into PIN	35 mA
Storage Temperature Range	−55°C to +150°C
Junction Operating Temperature Range[1]	−55°C to +150°C
Junction Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Package Power Dissipation[1]	($T_{J,MAX}$ − T_A)/θ_{JA}

[1]In applications where high power dissipation and poor package thermal resistance are present, the maximum ambient temperature may need to be derated. Maximum ambient temperature ($T_{A,MAX}$) is dependent on the maximum operating junction temperature ($T_{J,MAX}$ = 150°C), the maximum power dissipation of the device in the application ($P_{D,MAX}$), and the junction-to-ambient thermal resistance of the package in the application (θ_{JA}), is given by the following equation: $T_{A,MAX} = T_{J,MAX} - (\theta_{JA} \times P_{D,MAX})$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
10-lead MSOP on a 2-layer PCB	200	°C/W
10-lead MSOP on a 4-layer PCB	172	°C/W

Junction-to-ambient thermal resistance of the package is based on modeling and calculation using 2-layer and 4-layer boards, and natural convection. The junction-to-ambient thermal resistance is application- and board-layout dependent. In applications where high maximum power dissipation exists, attention to thermal dissipation issues in board design is required.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SIMPLIFIED BLOCK DIAGRAM

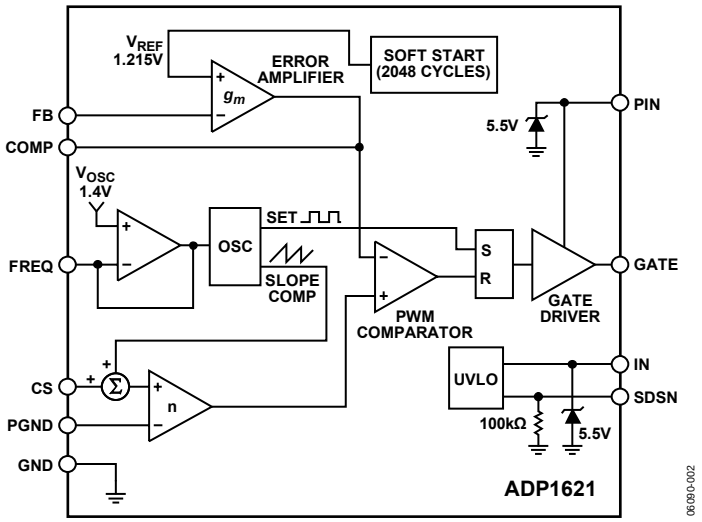


Figure 3. ADP1621 Simplified Block Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

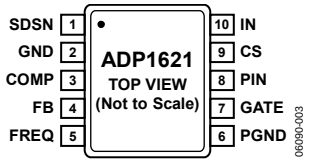


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SDSN	Shutdown and Synchronization Input. Turn the ADP1621 on by driving SDSN high; turn it off by driving SDSN low. If SDSN is left floating or when the SDSN is pulled low, the ADP1621 goes into shutdown after 50 µs. If synchronization is needed, synchronize the switching frequency to an external clock by connecting the external clock to the SDSN pin. An internal 100 kΩ pull-down resistor is connected from SDSN to GND.
2	GND	Ground.
3	COMP	Regulation Control Compensation Node. COMP is the output of the internal transconductance error amplifier. Connect a series RC from COMP to GND to compensate the regulator. The nominal voltage range for this pin is 1.0 V to 2.0 V.
4	FB	Feedback Input. FB is the input to the internal transconductance error amplifier. Drive FB from the output voltage through a resistive voltage divider. The ratio of the voltage divider sets the output voltage. The regulation voltage at FB is nominally 1.215 V.
5	FREQ	Frequency Control Input. Connect a resistor from FREQ to GND to set the free-running switching frequency between 100 kHz and 1.5 MHz. The nominal voltage of this pin is 1.4 V.
6	PGND	Power Ground Input. PGND is the ground return for the internal gate driver and the negative input of the internal current-sense amplifier. Connect PGND to GND as close to the ADP1621 as possible.
7	GATE	Gate Driver Output. The maximum gate driver output is equal to the PIN voltage. GATE drives the gate of the external n-channel power MOSFET. Connect GATE to the gate of the MOSFET.
8	PIN	Power Input. PIN powers the gate driver output. An internal 5.5 V shunt regulator is connected to this pin. Bypass PIN to PGND with a 0.1 µF or greater capacitor.
9	CS	Current-Sense Input. CS is the positive input of the current-sense amplifier. When GATE is turned on, the voltage at the CS pin increases linearly from 0 V to a maximum of 116 mV, and the nominal peak slope-compensation output current is 70 µA. When GATE is off, the CS function is disabled. For current sensing in lossless mode, connect CS to the drain of the power MOSFET. The absolute maximum voltage at CS is 33 V. For higher accuracy current sensing or higher switch-node voltages, connect CS to a current-sense power resistor in the source of the power MOSFET. In both sensing methods, it is required to add a slope-compensation resistor, R_S, to the CS pin to achieve stability in the inductor current for duty cycles greater than 50%. However, it is recommended to add R_S for all duty cycles because load transients can momentarily cause the duty cycle to be greater than 50%, even when the steady-state duty cycle is less than 50%.
10	IN	Input Voltage. IN powers the ADP1621 internal circuitry. An internal 5.5 V shunt regulator is connected to this pin. Bypass IN to GND with a 0.1 µF or greater capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

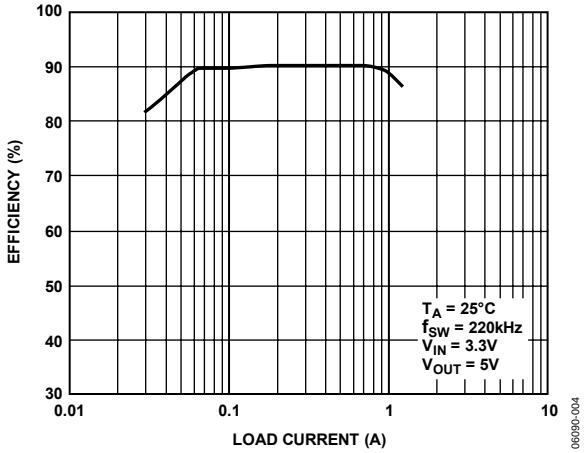


Figure 5. Efficiency vs. Load Current

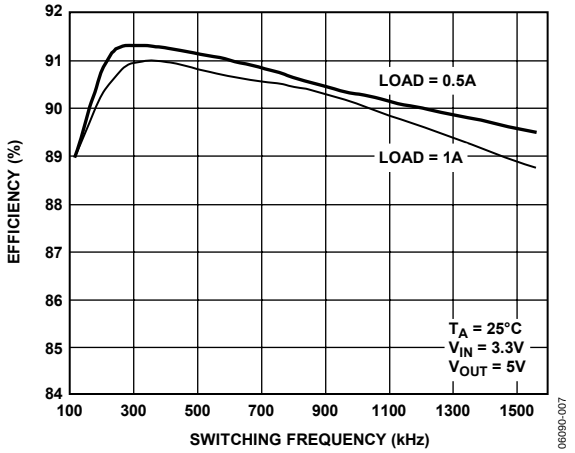


Figure 8. Efficiency vs. Switching Frequency

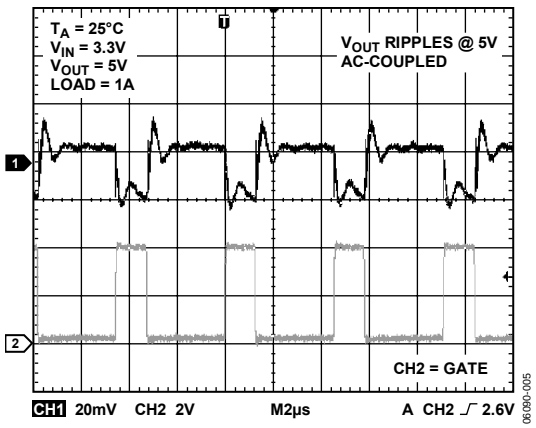


Figure 6. Output Voltage Ripple of the Circuit Shown in Figure 1

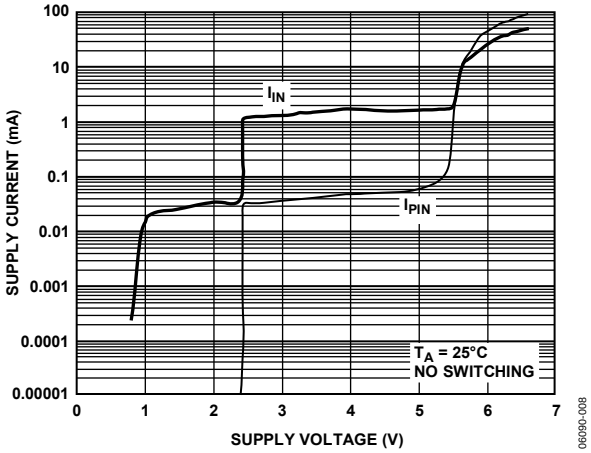


Figure 9. Supply Current vs. Supply Voltage

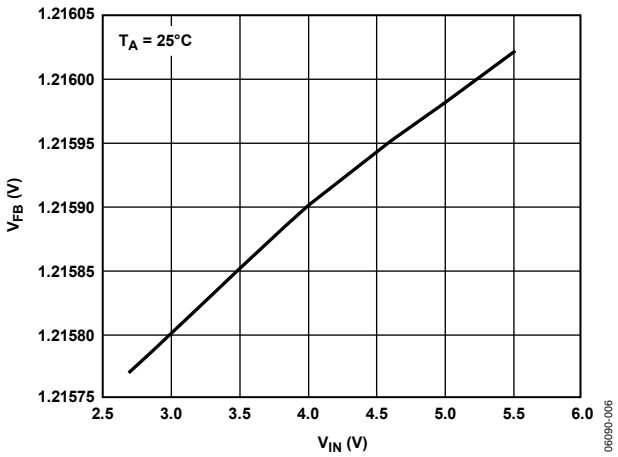


Figure 7. V_{FB} vs. V_{IN}

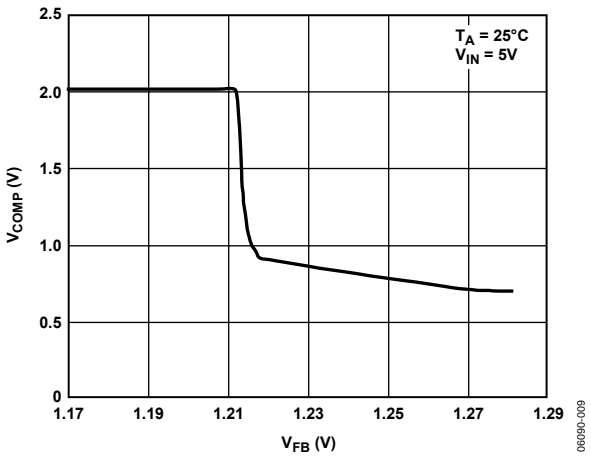


Figure 10. V_{COMP} vs. V_{FB}

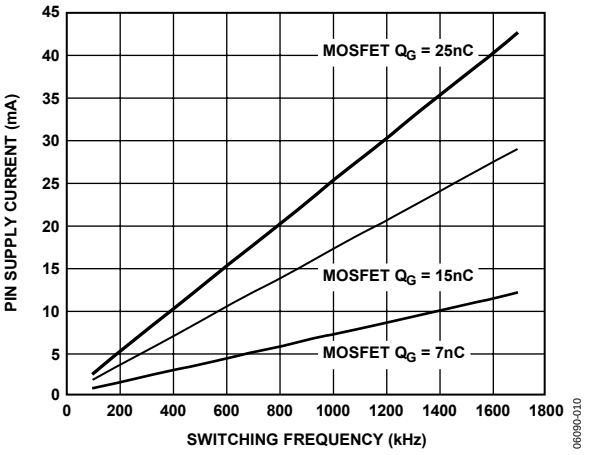


Figure 11. PIN Supply Current vs. Switching Frequency

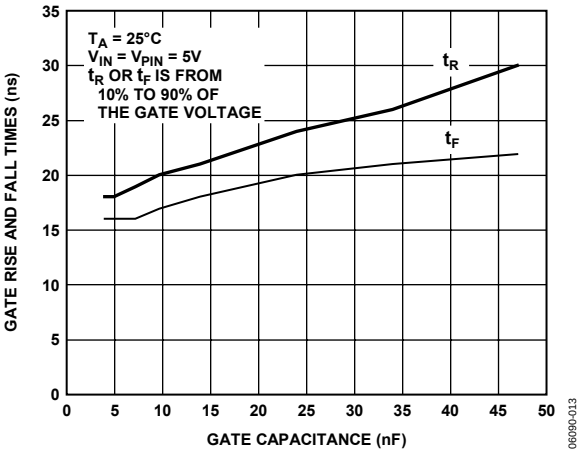


Figure 14. GATE Rise and Fall Times vs. C_{GATE}

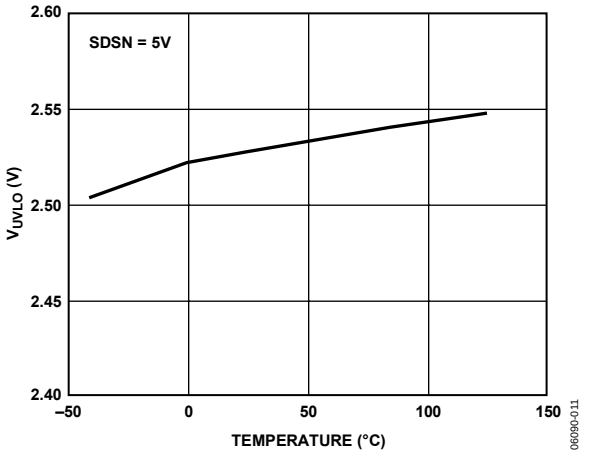


Figure 12. V_{UVLO} Threshold vs. Temperature

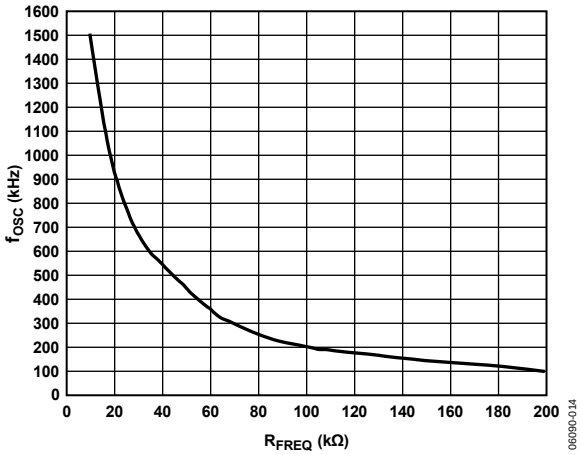


Figure 15. Oscillator Frequency vs. Resistance

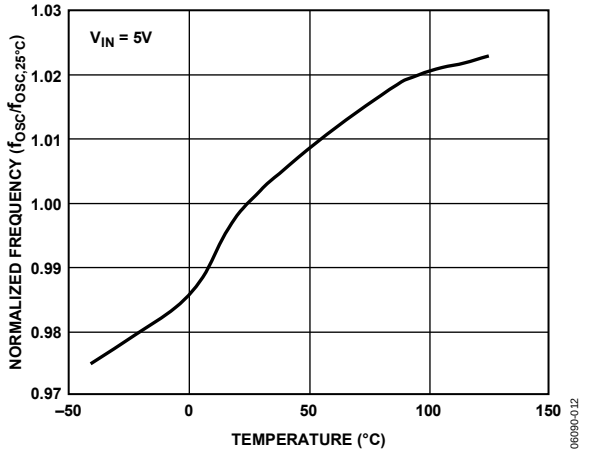


Figure 13. Frequency vs. Temperature

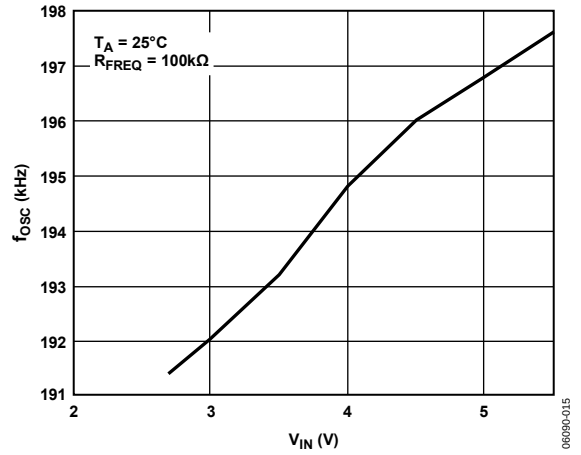


Figure 16. Oscillator Frequency vs. V_{IN}

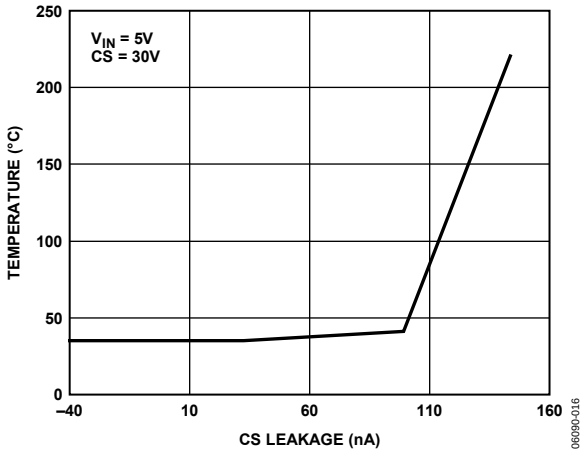


Figure 17. Temperature vs. CS Leakage

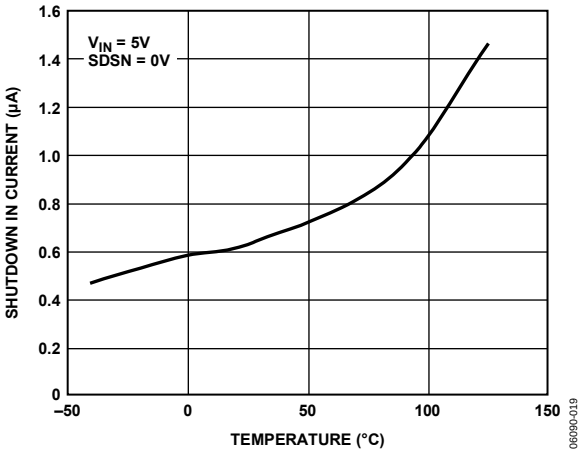


Figure 20. Shutdown IN Current vs. Temperature

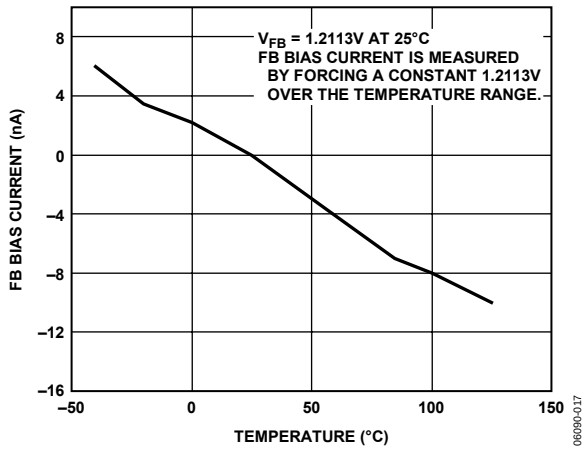


Figure 18. FB Bias Current vs. Temperature

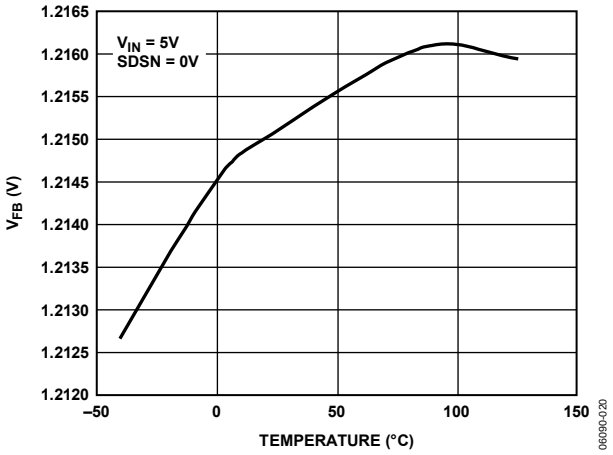


Figure 21. FB Voltage vs. Temperature

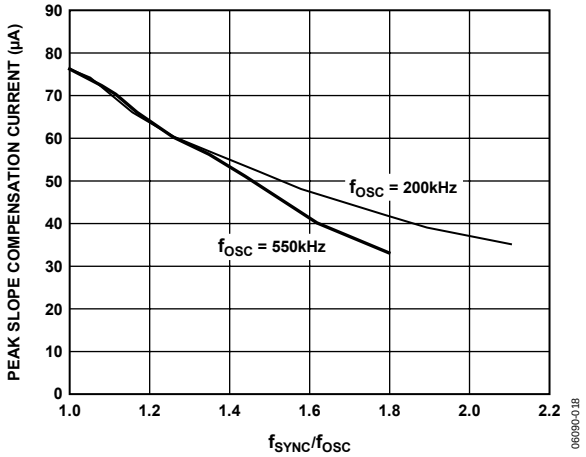


Figure 19. Slope-Compensation Current vs. f_{SYNC}/f_{OSC}

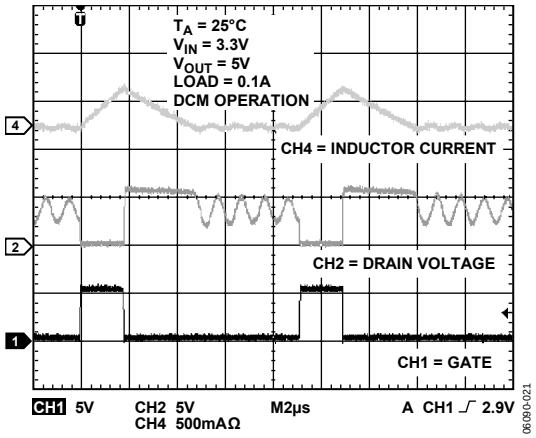


Figure 22. DCM Switching Waveform

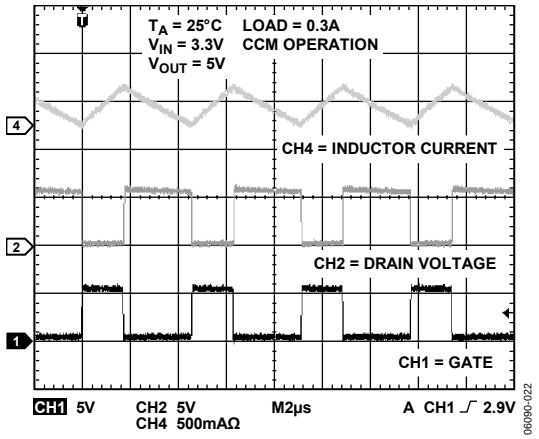


Figure 23. CCM Switching Waveform

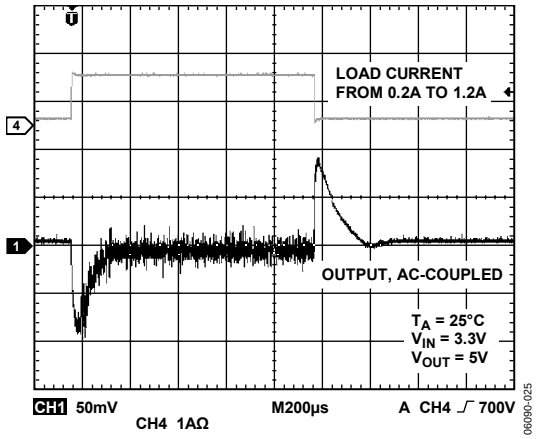


Figure 26. Load Transient Response of the Circuit Shown in Figure 1

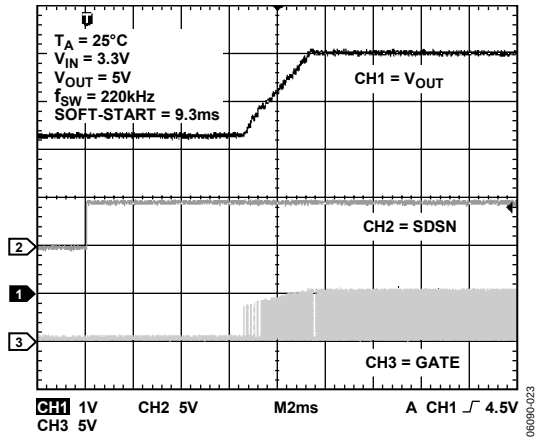


Figure 24. Soft Start Waveform

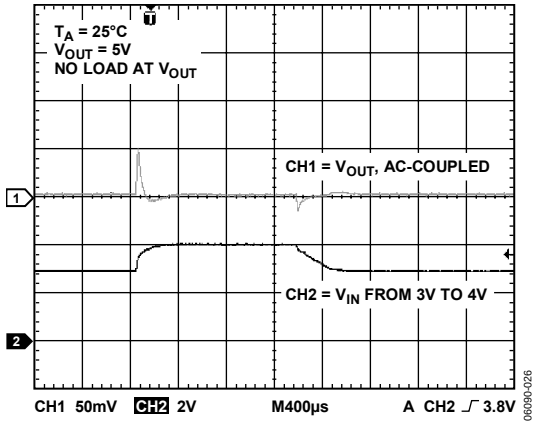


Figure 27. Line Transient Response of the Configuration Shown in Figure 1 with No Load

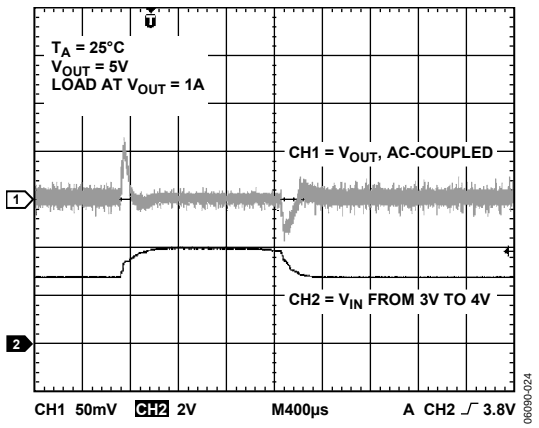


Figure 25. Line Transient Response of the Configuration Shown in Figure 1 with a 1 A Load

THEORY OF OPERATION

The ADP1621 is a fixed-frequency, current-mode, step-up dc/dc converter controller. It drives an external n-channel MOSFET to step the input voltage up to a higher output voltage. It can be used for SEPIC, flyback, boost, buck-boost, forward, and other converter topologies. It operates at a fixed switching frequency that is set by an external resistor over a range of 100 kHz to 1.5 MHz, and it can be synchronized to an external clock by connecting the SDSN pin to the clock.

The input supply current to the ADP1621 is less than 3 mA during normal operation and less than 10 µA during shutdown. The ADP1621 can drive large external MOSFETs, allowing it to support load currents in excess of 10 A.

CONTROL LOOP

The ADP1621 uses a current-mode architecture to regulate the output voltage. The output voltage is monitored at FB through a resistive voltage divider. The voltage at FB is compared to the internal 1.215 V reference voltage by the internal transconductance error amplifier to create an error current at COMP. A resistor-capacitor compensation impedance connected from COMP to GND converts the error current to an error voltage.

At the beginning of the switching cycle, the MOSFET is turned on and the inductor current ramps up. The MOSFET current is measured and converted to a voltage using R_{CS} or R_{DSON} and is added to the stabilizing slope-compensation ramp. The resulting voltage sum passes through the current-sense amplifier to generate the current-sense voltage. When the current-sense voltage is greater than the COMP error voltage, the MOSFET is turned off and the inductor current ramps down until the internal clock initiates the next switching cycle. The duty-cycle of the PWM modulator is thus adjusted to provide the necessary load current at the desired output voltage. Because the output voltage ultimately controls the peak inductor current through the COMP error voltage, this scheme is referred to as peak current-mode control.

With light loads, the converter can also operate under discontinuous conduction mode and pulse-skipping modulation to maintain output-voltage regulation. These two forms of operation are discussed in detail in the Light Load Operation section. Note that the converter can also be designed to operate in discontinuous conduction mode at full load if desired.

Overall, the current-mode regulation system of the ADP1621 allows fast transient responses while maintaining a stable output voltage. By selecting the proper resistor-capacitor network from COMP to GND, the regulator response can be optimized for a wide range of input voltages, output voltages, and load currents.

CURRENT-SENSE CONFIGURATIONS

The ADP1621 can sense the current across the on resistance of the MOSFET to minimize external component count and improve efficiency by eliminating the power that would be lost in a current-sense resistor. This lossless technique eliminates the need for an expensive current-sense resistor. In the lossless mode configuration, the voltage at the CS pin (or the switch-node voltage at the drain of the MOSFET) must not exceed 30 V (see Figure 28). This technique maximizes efficiency and reduces cost. In practice, when the calculated V_{SW} approaches 30 V, one should build the board and measure the actual V_{SW} before committing to the lossless mode design. Because of the parasitic inductance in the diode, output capacitor, and PCB traces, V_{SW} typically has narrow peaks that exceed the theoretical maximum voltage at V_{SW}—the sum of V_{OUT} and the forward-voltage drop of Diode D1. If the measured peak voltage exceeds 30 V, or if a more accurate current limit is desired, then the CS pin can be connected to an external current-sense resistor in the source of the MOSFET (Figure 29). The maximum power output is limited by the selection of the external components.

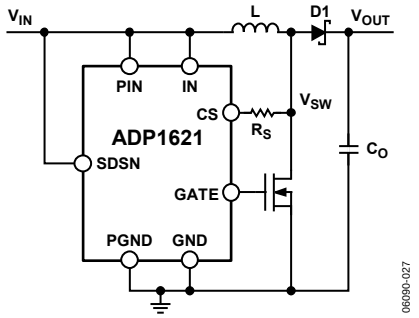


Figure 28. CS Pin Connection for V_{SW} < 30 V, Lossless Mode (No Current-Sense Resistor Needed)

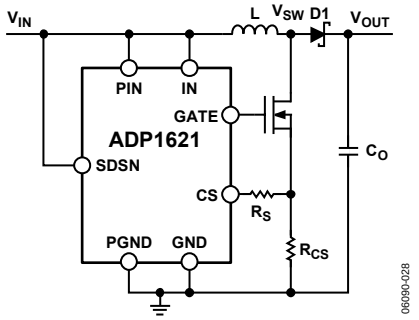


Figure 29. CS Pin Connection for V_{SW} > 30 V, Resistor Sense Mode with a Current-Sense Resistor, R_{CS}

CURRENT LIMIT

The current limit is achieved by the COMP voltage clamp, owing to the current-mode operation of the ADP1621. A detailed explanation of how the current limit is determined can be found in the Current Limit section of the Application Information: Boost Converter section.

UNDERVOLTAGE LOCKOUT

An internal undervoltage lockout (UVLO) circuit at the IN pin holds the GATE voltage low when the IN voltage is below the UVLO voltage, which is typically 2.5 V.

SHUTDOWN

The ADP1621 goes into shutdown approximately 50 µs after the SDSN pin is pulled low or left floating. There is an internal 100 kΩ resistor connected between SDSN and GND.

When the junction temperature of the ADP1621 reaches about 150°C, the ADP1621 goes into thermal shutdown and the GATE voltage is pulled low. When the junction temperature drops below about 140°C, the ADP1621 resumes normal operation after the soft start sequence.

SOFT START

The ADP1621 has an internal soft start circuit that ramps the FB regulation voltage from 0 V to 1.215 V in 64 steps over 2048 clock oscillator cycles. This soft start ramp allows the output voltage to slowly rise to the steady-state output voltage, preventing input inrush current at startup.

INTERNAL SHUNT REGULATORS

The IN and PIN pins each have an internal shunt regulator that allows the ADP1621 to operate over a wide input voltage range. The shunt regulators limit the voltages at IN and PIN to about 5.5 V, allowing the use of logic-level MOSFETs independent of the input and/or output voltage. The shunt regulator voltage can reach 5.7 V at 10 mA. See Figure 9 for the I-V characteristics of these shunt regulators.

The internal power is derived from the IN pin, whereas the MOSFET gate driver (GATE) current comes from the power input, PIN. By separating the two inputs, PIN can be driven with an external small-signal NPN transistor to limit the power loss in the PIN shunt regulator when the input voltage is higher than 5.5 V. See Figure 37 for an example. The maximum currents going into PIN and IN should not exceed 35 mA and 25 mA, respectively.

SETTING THE OSCILLATOR FREQUENCY AND SYNCHRONIZATION FREQUENCY

The free-running oscillator frequency, f_{OSC}, is set by a resistor from FREQ to GND. A 100 kΩ resistor sets the typical oscillator frequency to 200 kHz, a 65 kΩ resistor sets it to 325 kHz, a 32 kΩ resistor sets it to 600 kHz, and a 10 kΩ resistor sets it to 1.5 MHz. Figure 30 shows a typical relationship between f_{OSC} and R_{FREQ}.

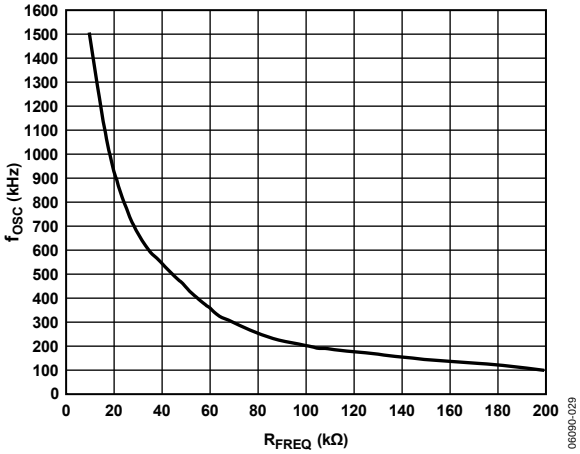


Figure 30. f_{OSC} vs. R_{FREQ}

The switching frequency can be synchronized to an external clock by driving the SDSN pin with that clock signal. The SDSN pin serves the two functions of shutdown control and frequency synchronization input. If the SDSN input detects a low-to-high transition within 10 µs of a high-to-low transition, it resets the oscillator to synchronize to the frequency of the signal at SDSN. The ADP1621 only synchronizes to frequencies greater than the free-running switching frequency. To ensure proper synchronization operation, set the synchronization frequency, f_{SYNC}, to 1.2× the free-running frequency, f_{OSC}. The switching frequency, f_{SW}, is equal to f_{SYNC}. Although the switching frequency can be synchronized to as high as 1.8 MHz, the peak slope-compensation current decreases at higher f_{SYNC}. It is recommended that the maximum f_{SYNC} be less than 1.4× of f_{OSC}. The slope-compensation resistor, R_S, should be chosen for the synchronization frequency (see the Slope Compensation section). For SDSN to detect a high input, the high state must remain high for at least 100 ns.

APPLICATION INFORMATION: BOOST CONVERTER

In this section, an analysis of a boost converter is presented, along with guidelines for component selection. A typical boost-converter application circuit is shown in Figure 1.

DUTY CYCLE

To determine the worst-case inductor current ripple, output voltage ripple, and slope-compensation factor, it is first necessary to determine the system duty cycle. The duty cycle in continuous conduction mode (CCM) is calculated by the equation

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D} \quad (1)$$

where V_{OUT} is the desired output voltage, V_{IN} is the input voltage, and V_D is the forward-voltage drop of the diode. A typical Schottky diode has a forward-voltage drop of 0.5 V.

The GATE minimum on and off times determine the minimum and maximum duty cycles, respectively. The minimum on and off times are typically 180 ns and 190 ns, respectively. The minimum and maximum duty cycles are given by

$$D_{MIN} = \frac{t_{ON,MIN}}{t_{SW}} = t_{ON,MIN} \times f_{SW} \quad (2)$$

$$D_{MAX} = 1 - \frac{t_{OFF,MIN}}{t_{SW}} = 1 - (t_{OFF,MIN} \times f_{SW}) \quad (3)$$

where D_{MIN} is the minimum duty cycle, D_{MAX} is the maximum duty cycle, $t_{ON,MIN}$ is the minimum on time, $t_{OFF,MIN}$ is the minimum off time, t_{SW} is the switching period, and f_{SW} is the switching frequency.

Note that when the converter tries to operate at a duty cycle lower than D_{MIN}, pulse-skipping modulation occurs to maintain the output voltage regulation (see the Light Load Operation section).

SETTING THE OUTPUT VOLTAGE

The output voltage is set through a voltage divider from the output voltage to the FB input. The feedback resistor ratio sets the output voltage of the system. The regulation voltage at FB is 1.215 V. The output voltage is given by (see Figure 1)

$$V_{OUT} = 1.215\ \text{V} \times \left(1 + \frac{R1}{R2}\right) \quad (4)$$

The input bias current into FB is 25 nA typical, 70 nA maximum. For a 0.1% degradation in regulation voltage and with 70 nA bias current, R2 must be less than 18 kΩ, which results in 68 µA of divider current. Choose the value of R1 to set the output voltage. Using higher values for R2 results in reduced output voltage accuracy due to the input bias current at the FB pin, whereas lower values cause increased quiescent current consumption.

INDUCTOR CURRENT RIPPLE

Choose a peak-to-peak inductor ripple current between 20% and 40% of the average inductor current. A good starting point for a design is to choose the peak-to-peak ripple current to be 30% of 1/(1 − D) times the maximum load current:

$$\Delta I_L = 0.3 \times \frac{I_{LOAD,MAX}}{1 - D} \quad (5)$$

where ΔI_L is the peak-to-peak inductor ripple current, and $I_{LOAD,MAX}$ is the maximum load current required by the application.

INDUCTOR SELECTION

The inductor value choice is important because it dictates the inductor current ripple and therefore the voltage ripple at the output.

The average inductor current, $I_{L,AVE}$, is given by

$$I_{L,AVE} = \frac{I_{LOAD}}{1 - D} \quad (6)$$

and the peak-to-peak inductor ripple current is inversely proportional to the inductor value:

$$\Delta I_L = \frac{V_{IN} \times D}{f_{SW} \times L} \quad (7)$$

where f_{SW} is the switching frequency, and L is the inductor value.

Assuming continuous conduction mode (CCM) operation, the peak inductor current is given by

$$I_{L,PK} = \frac{I_{LOAD}}{1 - D} + \frac{\Delta I_L}{2} = \frac{I_{LOAD}}{1 - D} + \frac{V_{IN} \times D}{2 \times f_{SW} \times L} \quad (8)$$

Smaller inductor values are typically smaller in size and usually less expensive, but increase the ripple current. Larger ripple current also increases the power loss in the inductor core. Too large an inductor value results in added expense and may impede load transient responses because it reduces the effect of slope compensation.

Assuming the ripple current is 30% of 1/(1 − D) times the maximum load current, a reasonable choice for the inductor value is

$$L = \frac{V_{IN} \times D \times (1 - D)}{0.3 \times f_{SW} \times I_{LOAD,MAX}} \quad (9)$$

From this starting point, modify the inductance to obtain the right balance of size, cost, and output voltage ripple while maintaining the inductor ripple current between 20% and 40% of 1/(1 − D) times the maximum load current. Keep in mind that the inductor saturation current must be greater than the peak inductor current. Magnetically shielded inductors are generally recommended, although they cost slightly more than unshielded inductors.

Also, losses due to the inductor winding resistance reduce the efficiency of the boost converter. This power loss is given by

$$P_{L,W} = \left(\frac{I_{LOAD}}{1 - D}\right)^2 \times R_W \quad (10)$$

where $P_{L,W}$ is the power dissipation in the winding of the inductor, and R_W is the winding resistance.

INPUT CAPACITOR SELECTION

The bulk input capacitor provides a low impedance path for the inductor ripple current. Capacitor C1 in Figure 1 represents a bulk input capacitor. Choose a bulk input capacitor whose impedance at the switching frequency is lower than the impedance of the voltage source V_{IN}.

The preferred bulk input capacitor is a 10 µF to 100 µF ceramic capacitor because it has low equivalent series resistance (ESR) and low impedance. Aluminum electrolytic and aluminum polymer capacitors can also be used as the bulk input capacitors. The bulk input capacitor does not need to be placed very close to the IN and PIN pins. Aluminum electrolytic capacitors are the cheapest and generally have high ESR values, which increase dramatically at temperatures less than 0°C. Some aluminum electrolytic capacitors have ESR less than 20 mΩ, but their capacitances are generally greater than 800 µF. Aluminum polymer capacitors are more expensive than the aluminum electrolytic ones, but are generally cheaper than the ceramic capacitors for the same amount of capacitance. Polymer capacitors have relatively low ESR, with some models having less than 10 mΩ.

Regardless of the type of capacitor used, make sure the ripple current rating of the bulk input capacitor, $I_{CIN,RMS}$, is greater than

$$I_{CIN,RMS} = \frac{1}{\sqrt{3}} \times \frac{\Delta I_L}{2} \quad (11)$$

where ΔI_L is the peak-to-peak inductor ripple current.

In addition to the bulk input capacitor, a bypass input capacitor is required. The function of the bypass capacitor is to locally filter the input voltage to the ADP1621 and maintain the input voltage at a steady value during switching transitions. The bypass capacitor is typically a 0.1 µF or greater ceramic capacitor and should be placed as close as possible to the IN and PIN pins of the ADP1621. Capacitors C3 and C4 in Figure 1 represent the bypass capacitors.

OUTPUT CAPACITOR SELECTION

The output capacitor maintains the output voltage and supplies current to the load while the external MOSFET is on.

The value and characteristics of the output capacitor greatly affect the output voltage ripple and stability of the converter.

The amount of peak-to-peak output voltage ripple, ΔV_{OUT}, can be approximated by

$$\Delta V_{OUT} \approx \left(\frac{I_{LOAD}}{1-D} + \frac{\Delta I_L}{2} \right) \times \sqrt{\left(\frac{1}{2\pi \times f_{SW} \times C_{OUT}} \right)^2 + ESR^2 + \left(2\pi \times f_{SW} \times ESL \right)^2} \quad (12)$$

where ΔI_L is the peak-to-peak inductor ripple current, f_{SW} is the switching frequency, C_{OUT} is the output capacitance, *ESR* is the effective ESR of C_{OUT}, and *ESL* is the effective equivalent series inductance of C_{OUT}.

Because the output capacitor is typically greater than 40 µF, the ESR dominates the output capacitance impedance and thus the output voltage ripple. The use of low ESR, ceramic dielectric capacitors is preferred, although aluminum electrolytic, tantalum, OS-CON™ (from Sanyo), and aluminum polymer capacitors can be used. At higher switching frequencies, the ESL of the output capacitor may also be a factor in determining the output voltage ripple. Multiple capacitors can be connected in parallel to reduce the effective ESR and ESL. Keep in mind that the capacitance of a given capacitor typically degrades with increased temperature and bias voltage. Consult the capacitor manufacturer's data sheet when determining the actual capacitance of a capacitor under certain conditions.

Ensure that the output capacitor ripple current rating, $I_{COUT,RMS}$, is greater than

$$I_{COUT,RMS} = I_{LOAD} \times \sqrt{\frac{D}{1-D}} \quad (13)$$

DIODE SELECTION

The diode conducts the inductor current to the output capacitor and load while the MOSFET is off. The average diode current is the load current:

$$I_{DIODE,AVE} = I_{LOAD} \quad (14)$$

The rms diode current in continuous conduction mode is given by

$$I_{DIODE,RMS} = \frac{I_{LOAD}}{1-D} \times \sqrt{1-D} \quad (15)$$

where *D* is the duty cycle.

The power dissipated in the diode is

$$P_{DIODE} = V_D \times I_{LOAD} \quad (16)$$

where V_D is the forward-voltage drop of the diode.

The total power dissipation determines the diode junction temperature, which is given by

$$T_{J,DIODE} = T_A + P_{DIODE} \times \theta_{JA} \quad (17)$$

where $T_{J,DIODE}$ is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the diode package. The diode junction temperature must not exceed its maximum rating at the given power dissipation level.

For high efficiency, Schottky diodes are recommended. The low forward-voltage drop of a Schottky diode reduces the power losses during the MOSFET off time, and the fast switching speed reduces the switching losses during the MOSFET transitions. However, for high voltage, high temperature applications where the reverse leakage current of the Schottky diode can become significant and degrade efficiency, use an ultrafast-recovery junction diode.

Make sure that the diode is rated to handle the average output load current. Many diode manufacturers derate the current capability of the diode as a function of the duty cycle. Verify that the diode is rated to handle the average output load current with the minimum duty cycle. Also, ensure that the peak inductor current is less than the maximum rated current of the diode.

MOSFET SELECTION

When turned on, the external n-channel MOSFET allows energy to be stored in the magnetic field of the inductor. When the MOSFET is turned off, this energy is delivered to the load to boost the output voltage.

The choice of the external power MOSFET directly affects the boost converter performance. Choose the MOSFET based on the following: threshold voltage (V_T), on resistance (R_{DSON}), maximum voltage and current ratings, and gate charge.

The minimum operating voltage of the ADP1621 is 2.9 V. Choose a MOSFET with a V_T that is at least 0.3 V less than the minimum input supply voltage at PIN used in the application. Ensure that the maximum V_{GS} rating of the MOSFET is at least a few volts greater than the maximum voltage that is applied to PIN. Ensure that the maximum V_{DS} rating of the MOSFET exceeds the maximum V_{OUT} by at least 5 V to 10 V. Depending on parasitics, the MOSFET may be exposed to voltage spikes that exceed the sum of V_{OUT} and the forward-voltage drop of the diode.

Estimate the rms current in the MOSFET under continuous conduction mode by

$$I_{MOSFET,RMS} = \frac{I_{LOAD}}{1-D} \times \sqrt{D} \quad (18)$$

where D is the duty cycle. Derate the MOSFET current at least 20% to account for inductor ripple and changes in the forward-voltage drop of the diode.

The MOSFET power dissipation due to conduction is thus

$$P_C = \left(\frac{I_{LOAD}}{1-D}\right)^2 \times D \times R_{DSON} \times (1+K) \quad (19)$$

where P_C is the conduction power loss, and R_{DSON} is the MOSFET on resistance. The variable K is a factor that models the increase of R_{DSON} with temperature:

$$K = 0.005/^{\circ}\text{C} \times (T_{J,MOSFET} - 25^{\circ}\text{C}) \quad (20)$$

where $T_{J,MOSFET}$ is the MOSFET junction temperature. Note that multiple n-channel MOSFETs can be placed in parallel to reduce the effective R_{DSON}.

The power dissipation due to switching transition loss is approximated by

$$P_{SW} = \frac{(V_{OUT} + V_D) \times \frac{I_{LOAD}}{1-D} \times (t_R + t_F) \times f_{SW}}{2} \quad (21)$$

where P_{SW} is the switching power loss, t_R is the MOSFET rise time, and t_F is the MOSFET fall time. The MOSFET rise and fall times are functions of both the gate drive circuitry and the MOSFET used in the application.

The total power dissipation of the MOSFET is the sum of the conduction and transition losses:

$$P_{MOSFET} = P_C + P_{SW} \quad (22)$$

where P_{MOSFET} is the total MOSFET power dissipation. Ensure that the maximum power dissipation is significantly less than the maximum power rating of the MOSFET.

The total power dissipation also determines the MOSFET junction temperature, which is given by

$$T_{J,MOSFET} = T_A + P_{MOSFET} \times \theta_{JA} \quad (23)$$

where $T_{J,MOSFET}$ is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the MOSFET package. The MOSFET junction temperature must not exceed its maximum rating at the given power dissipation level.

If lossless current sensing is not used, there will also be power dissipation in the external current-sense resistor, R_{CS}. The power dissipation, P_{CS}, in the external resistor due to conduction losses is given by

$$P_{CS} = \left(\frac{I_{LOAD}}{1-D}\right)^2 \times D \times R_{CS} \quad (24)$$

LOOP COMPENSATION

The ADP1621 uses external components to compensate the regulator loop, allowing optimization of the loop dynamics for a given application.

The step-up converter produces an undesirable right-half plane (RHP) zero in the regulation feedback loop. This RHP zero requires compensating the regulator such that the crossover

frequency occurs well below the frequency of the RHP zero. The location of the RHP zero is determined by the following equation:

$$f_{Z,RHP} = (1-D)^2 \times \frac{R_{LOAD}}{2\pi \times L} \quad (25)$$

where $f_{Z,RHP}$ is the RHP zero frequency, and R_{LOAD} is the equivalent load resistance or the output voltage divided by the load current.

To stabilize the regulator, ensure that the regulator crossover frequency is less than or equal to one-fifth of the RHP zero frequency and less than or equal to one-fifteenth of the switching frequency. For an initial practical design, choose the crossover frequency f_C to be the lower of

$$f_C = \frac{f_{SW}}{15} \quad (26)$$

and

$$f_C = \frac{f_{Z,RHP}}{5} \quad (27)$$

where f_C is the crossover frequency, and f_{SW} is the switching frequency.

The regulator loop gain is

$$A_{VL} = \frac{V_{FB}}{V_{OUT}} \times (1-D) \times g_m \times |Z_{COMP}| \times \frac{1}{n \times R_{CS}} \times |Z_{OUT}| \quad (28)$$

where A_{VL} is the loop gain, V_{FB} is the feedback regulation voltage (typically 1.215 V), V_{OUT} is the regulated output voltage, D is the duty cycle, g_m is the error amplifier transconductance gain (typically 300 µS), Z_{COMP} is the impedance of the RC network from COMP to GND, n is the current-sense amplifier gain (typically 9.5), R_{CS} is the current-sense resistance, and Z_{OUT} is the impedance of the load and output capacitor. In the case of lossless current sensing, as shown in Figure 28, R_{CS} is equal to the on resistance, R_{DSON}, of the external power MOSFET. Otherwise, R_{CS} represents the external current-sense resistor, as shown in Figure 29.

To determine the crossover frequency, it is important to note that at that frequency the compensation impedance, Z_{COMP}, is dominated by Resistor R_{COMP}, and the output impedance, Z_{OUT}, is dominated by the impedance of the output capacitor, C_{OUT}. When solving for the crossover frequency, the equation is simplified to

$$|A_{VL}| = \frac{V_{FB}}{V_{OUT}} \times (1-D) \times g_m \times R_{COMP} \times \frac{1}{n \times R_{CS}} \times \frac{1}{2\pi \times f_C \times C_{OUT}} = 1 \quad (29)$$

where f_C is the crossover frequency, R_{COMP} is the compensation resistor, and C_{OUT} is the output capacitance.

Solving for R_{COMP} gives

$$R_{COMP} = \frac{2\pi \times f_C \times C_{OUT} \times n \times R_{CS} \times V_{OUT}}{V_{FB} \times (1-D) \times g_m} \quad (30)$$

Once the compensation resistor, R_{COMP}, is known, set the zero formed by the resistor and compensation capacitor, C_{COMP}, to one-fourth of the crossover frequency, or

$$C_{COMP} = \frac{2}{\pi \times f_C \times R_{COMP}} \quad (31)$$

Capacitor C2 is chosen to cancel the zero introduced by the output capacitance ESR. Thus, C2 should be set to (see Figure 31)

$$C2 = \frac{ESR \times C_{OUT}}{R_{COMP}} \quad (32)$$

where *ESR* represents the ESR of C_{OUT}.

For low ESR output capacitors, such as ceramic capacitors, C2 is small, generally in the range of 10 pF to 400 pF. Because of the parasitic inductance, resistance, and capacitance of the PCB layout, the R_{COMP}, C_{COMP}, and C2 values might need to be adjusted by observing the load transient response of the ADP1621 to establish a stable operating system and achieve optimal transient performance. For most applications, R_{COMP} is in the range of 5 kΩ to 100 kΩ, and C_{COMP} is in the range of 100 pF to 30 nF.

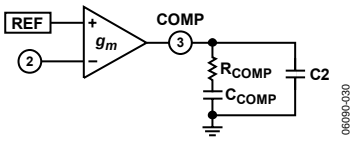


Figure 31. Compensation Components

SLOPE COMPENSATION

The ADP1621 includes a circuit that allows adjustable slope compensation. Slope compensation is required by current-mode regulators to stabilize the current-control loop when operating in continuous conduction and the switching duty cycle is greater than 50%.

Slope compensation is achieved by internally forcing a ramping current source out of the CS current-sense pin. By placing a resistor between the CS pin and the current sensing device (the drain of the external MOSFET in the case of lossless current sensing or the source of the MOSFET if a current-sense resistor is used), a voltage is developed across the resistor that is proportional to the slope-compensation current.

To ensure stability of the current-mode control loop, use a compensation voltage slope that is equal to or greater than one-half of the current-sense representation of the inductor current downslope. Therefore, it follows that

$$2 \times R_S \times \frac{I_{SC,PK} \times f_{SW}}{1 - t_{OFF,MIN} \times f_{SW}} > R_{CS} \times \frac{V_{OUT} + V_D - V_{IN}}{L} \quad (33)$$

where R_S is the slope-compensation resistor, $I_{SC,PK}$ is the peak slope-compensation current, f_{SW} is the switching frequency, R_{CS} is the current-sense resistor, V_{OUT} is the regulated output voltage, V_D is the forward-voltage drop of the diode, V_{IN} is the input voltage, $t_{OFF,MIN}$ is the minimum off time, and L is the power-stage inductor. In the case of lossless current sensing, R_{CS} is equal to the on resistance,

R_{DSON}, of the external power MOSFET. Otherwise, R_{CS} represents the external current-sense resistor.

Solving for R_S gives the slope-compensation criterion:

$$R_S > \frac{R_{CS} \times (V_{OUT} + V_D - V_{IN}) \times (1 - t_{OFF,MIN} \times f_{SW})}{2 \times I_{SC,PK} \times f_{SW} \times L} \quad (34)$$

Keep in mind that the above inequality is a function of both ADP1621 parameters and off-chip components, the values of which vary from part to part and with temperature. Select R_S to ensure current-loop stability for all possible variations.

After accounting for parameter variations, use values of R_S that are as close to the calculated limit as possible because excessive slope compensation reduces the benefits of current-mode control and increases the "softness" of the current limit, as discussed in the Current Limit section. Given a typical peak slope-compensation current of 70 µA, R_S should not exceed 1.6 kΩ because the voltage at the CS pin is typically clamped at 116 mV. It is also recommended that R_S be greater than 20 Ω. If the calculated R_S is greater than 1.6 kΩ, the parameters in Equation 34, such as R_{CS}, f_{SW}, and L, can be adjusted such that R_S is less than 1.6 kΩ.

In conclusion, the value of R_S should be 20 Ω ≤ R_S ≤ 1.6 kΩ.

CURRENT LIMIT

The current limit in the ADP1621 limits the peak inductor current and is achieved by the COMP voltage clamp. The peak inductor current, $I_{L,PK}$, is given by

$$I_{L,PK} = \frac{\frac{V_{COMP,CLAMP} - V_{COMP,ZCT}}{n} - \frac{I_{SC,PK} \times R_S \times D}{1 - t_{OFF,MIN} \times f_{SW}}}{R_{CS}} \quad (35)$$

where $V_{COMP,CLAMP}$ is the COMP clamp voltage (typically 2.0 V), $V_{COMP,ZCT}$ is the COMP zero-current threshold (typically 1.0 V), n is the current-sense amplifier gain (typically 9.5), $I_{SC,PK}$ is the peak slope-compensation current (typically 70 µA), R_S is the slope-compensation resistor, D is the duty cycle, f_{SW} is the switching frequency, $t_{OFF,MIN}$ is the minimum off time (typically 190 ns), and R_{CS} is the current-sense resistor. In the case of lossless current sensing, R_{CS} is equal to the on resistance, R_{DSON}, of the external power MOSFET. Otherwise, R_{CS} represents the external current-sense resistor.

The current limit in the ADP1621 is a "soft" current limit. When the inductor current reaches the $I_{L,PK}$ limit given in Equation 35, the duty cycle decreases, and the output voltage drops below the desired voltage. The $I_{L,PK}$ limit in Equation 35 then increases in response to the smaller duty cycle, D. The larger the slope-compensation resistor, R_S, the larger the effect on $I_{L,PK}$ for an incremental decrease in D. This behavior results in a "soft" current limit for the ADP1621. Use values of R_S that are as close as possible to the calculated limit derived from Equation 34. If high-precision current limiting is required, consider inserting a fuse in series with the inductor.

Also, keep in mind that the current limit is a function of both ADP1621 parameters and off-chip components, the values of which vary from part to part and with temperature. If lossless current sensing is used, consider that the on resistance of a MOSFET typically increases with increasing junction temperature.

The peak inductor current limit also limits the maximum load current at a given output voltage. The maximum load current, assuming CCM operation, is given by

$$I_{LOAD,MAX} = (1 - D) \times \left(\frac{\frac{V_{COMP,CLAMP} - V_{COMP,ZCT}}{n} - \frac{I_{SC,PK} \times R_S \times D}{1 - t_{OFF,MIN} \times f_{SW}}}{R_{CS}} - \frac{V_{IN} \times D}{2 \times f_{SW} \times L} \right) \quad (36)$$

If the load current exceeds $I_{LOAD,MAX}$, the output voltage drops below the desired voltage.

LIGHT LOAD OPERATION

Discontinuous Conduction Mode

With light loads, the average inductor current is small, and, depending on the converter design, the instantaneous inductor current may reach 0 during the time when the MOSFET is off. This mode of operation is termed discontinuous conduction mode. The condition for entering discontinuous conduction mode in a boost converter is

$$I_{LOAD} < \frac{V_{IN} \times D \times (1 - D)}{2 \times L \times f_{SW}} \quad (37)$$

When the instantaneous inductor current reaches 0 during the cycle, the inductor ceases to be a current source, and ringing can be observed in the waveforms of the MOSFET drain voltage and the inductor current. The frequency of the ringing is the resonant frequency of the inductor and the total capacitance from the SW node to GND, which includes the capacitances of the MOSFET and diode, and any parasitic capacitances from the PCB. While adding a resistive element, such as a snubber, to the system further dampens the resonance, it also decreases the efficiency of the regulator.

Pulse-Skipping Modulation

The ADP1621 features circuitry that improves the converter efficiency and minimizes power consumption with no load or very light loads. When the COMP voltage drops below $V_{COMP,ZCT}$ (typically 1.0 V), which can occur at sufficiently light loads, the MOSFET is powered off until the FB voltage drops below 1.215 V. Then, the error amplifier drives the COMP voltage higher, and the converter resumes switching when the COMP voltage rises above the $V_{COMP,ZCT}$ voltage. While the MOSFET is powered off, the output capacitor supplies current to the load.

With light loads, the COMP voltage hovers around 1.0 V, and short periods of switching are followed by long periods of the MOSFET being powered off. This pulse-skipping modulation operation improves converter efficiency by reducing the number of switching cycles and therefore reducing the gate drive current and the switching transition power loss.

Given the minimum on time of the ADP1621, pulse-skipping modulation is also a requirement to maintain output voltage regulation with light loads. During the short switching periods of pulse-skipping modulation, the MOSFET is turned on for the minimum on time each cycle, storing just enough energy in the inductor to charge the output capacitor. During the long period when the MOSFET is off, no current flows through the inductor, and the light load current is supplied by the output capacitor.

RECOMMENDED COMPONENT MANUFACTURERS

Table 5.

Vendor	Components
AVX Corporation	Capacitors
Central Semiconductor Corp.	Diodes
Coilcraft, Inc.	Inductors
Diodes, Inc.	Diodes
International Rectifier	Diodes, MOSFETs
Murata Manufacturing Co., Ltd.	Capacitors, inductors
ON Semiconductor	Diodes, MOSFETs
Rubycon Corporation	Capacitors
Sanyo	Capacitors
Sumida	Inductors
Taiyo Yuden, Inc.	Capacitors, inductors
Toko America, Inc.	Inductors
United Chemi-Con, Inc.	Capacitors
Vishay Siliconix	Diodes, MOSFETs, resistors, capacitors

LAYOUT CONSIDERATIONS

Layout is important for all switching regulators, but is particularly important for regulators with high switching frequencies. To achieve high efficiency, good regulation, and stability, a well-designed printed circuit board layout is required. A sample PCB layout for the standard boost converter circuit shown in Figure 33 is given in Figure 32.

Follow these guidelines when designing printed circuit boards:

- Keep the low ESR bypass input capacitor of 0.1 µF or higher close to IN/PIN and GND.
- Keep the high current path from Bulk Input Capacitor C1 through Inductor L1 and MOSFET M1 to PGND as short as possible.
- Keep the high current path from Bulk Input Capacitor C1 through Inductor L1, Diode D1, and Output Capacitor C_{OUT} to PGND as short as possible. Place C_{OUT} as close to PGND as possible to reduce ground bouncing.
- Keep high current traces as short and wide as possible to minimize parasitic series inductance, which causes spiking and electromagnetic interference (EMI).
- To minimize switching noise, the drain of the power MOSFET should be placed very close to the inductor, and the source of the MOSFET (or the bottom side of the sense resistor) should be connected directly to the power GND plane. Use wide copper traces on the drain and on the source of the MOSFET to minimize parasitic inductance and resistance. Parasitic inductance can lead to excessive ringing during switching transitions, and parasitic resistance reduces the converter efficiency. Make sure that the MOSFET selected is capable of handling the total power loss (conduction plus transition losses) in the application circuit.
- Avoid routing high impedance traces near any node connected to the switch node (the MOSFET drain) or near Inductor L1 to prevent radiated switching-noise injection.
- Add an extra copper plane at the connection of the MOSFET drain and the anode of the diode to help dissipate the heat generated by losses in those components.
- Avoid ground loops by having one central ground node on the PCB. If this is impractical, place the power ground with high current levels physically closer to the PCB ground terminal. The analog, low current-level ground should be placed farther from the PCB ground terminal.
- Minimize the length of the PCB trace between the GATE pin and the MOSFET gate. The parasitic inductance in this PCB trace can give rise to excessive voltage ringing at the MOSFET gate and drain, as well as the regulator output. It is recommended to add 5 Ω of resistance for every inch of PCB trace. This helps to reduce the overshoot and ringing at the drain and the output. However, this added resistance increases the rise and fall times of the MOSFET; thus, the switching loss in the MOSFET is increased.
- Place the feedback resistors as close to FB as possible to prevent high frequency switching-noise injection.
- Place the top of the upper feedback resistor, R1, as close as possible to the top of C_{OUT} for optimum output voltage sensing.
- If a current-sense resistor is connected between the source of the MOSFET and PGND, ensure that the capacitance from CS to PGND is minimized.
- Place the compensation components as close as possible to COMP.

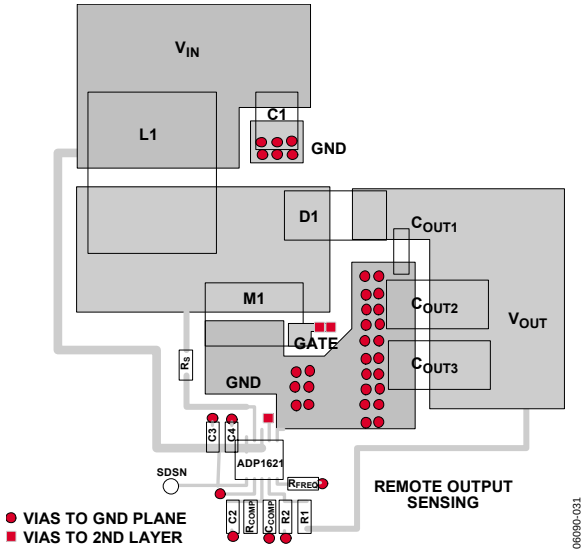


Figure 32. PCB Layout of the Circuit Shown in Figure 33 (2-layer PCB)

EFFICIENCY CONSIDERATIONS

The efficiency, η, of a dc/dc converter is given by

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\% \quad (38)$$

where P_{OUT} is the output power, and P_{IN} is the input power to the converter. While switching regulators are ideally lossless converters of power, the nonideal characteristics of regulator components degrade the efficiency of the regulator.

The primary sources of power dissipation in the regulator include

- The power dissipation in the external power MOSFET due to conduction and switching losses.

$$P_{MOSFET} = P_C + P_{SW} \quad (39)$$
$$= \left[\left(\frac{I_{LOAD}}{1-D}\right) \times D \times R_{DSON} \times (1+K)\right] +$$
$$\left[\frac{(V_{OUT} + V_D) \times \frac{I_{LOAD}}{1-D} \times (t_R + t_F) \times f_{SW}}{2}\right]$$

- The power dissipation in the external current-sense resistor if lossless current sensing is not used.

$$P_{CS} = \left(\frac{I_{LOAD}}{1-D}\right)^2 \times D \times R_{CS} \quad (40)$$

- The power dissipation in the external diode.

$$P_{DIODE} = V_D \times I_{LOAD} \quad (41)$$

- The power dissipation in the winding resistance of the power stage inductor.

$$P_{L,W} = \left(\frac{I_{LOAD}}{1-D}\right)^2 \times R_W \quad (42)$$

- The supply current to the ADP1621 IC, which includes the quiescent current and the gate driver charging current. The power dissipation due to gate charging loss is approximated by

$$P_G = V_{PIN} \times Q_G \times f_{SW} \quad (43)$$

where P_G is the gate charging power loss, V_{PIN} is the voltage at the PIN pin, Q_G is the MOSFET total gate charge, and f_{SW} is the converter switching frequency. Therefore, the total power dissipation in the IC itself is given by

$$P_{IC} = P_G + (V_{IN} \times I_Q) \quad (44)$$
$$= (V_{PIN} \times Q_G \times f_{SW}) + (V_{IN} \times I_Q)$$

where P_{IC} is the total power dissipated in the IC, I_Q is the quiescent current, and V_{IN} is the voltage at the IN pin.

The secondary sources of power dissipation in the regulator include

- The power dissipation in the ESR of the input and output capacitors.
- Inductor core losses due to hysteresis and eddy currents.

EXAMPLES OF APPLICATION CIRCUITS

STANDARD BOOST CONVERTER—DESIGN EXAMPLE

The example covered here is for the ADP1621 configured as a standard boost converter, as shown in Figure 33, where lossless current sensing is employed. The design parameters are V_{IN} = 3.3 V, V_{OUT} = 5 V, and a maximum load current of 1 A.

To begin this design, a switching frequency of 600 kHz is chosen (by setting R_{FREQ} to 32 kΩ, see Figure 30) so that a small inductor and small output capacitors can be used. The duty cycle is calculated from Equation 1 to be 0.4, given a forward-voltage drop of 0.5 V for the Schottky diode. The feedback resistors are calculated to be R1 = 35.7 kΩ and R2 = 11.5 kΩ from Equation 4.

Assuming that the inductor ripple is 30% of 1/(1 − D) times the maximum load current, the inductor size is calculated to be about 4.4 µH, according to Equation 9. The small, magnetically shielded 4.7 µH Toko FDV0630-4R7M inductor is selected. Because ceramic capacitors have very low ESR (a few milliohms), a 47 µF/6.3 V Murata GRM31CR60J476M ceramic capacitor is chosen for the input capacitor. The output voltage ripple for a given C_{OUT}, ESR, and ESL can be found by solving Equation 12. By choosing an output voltage ripple equal to 1% of the output voltage, Equation 12 yields that the minimum C_{OUT} required is 100 µF and the maximum ESR required is 25 mΩ. Other combinations of capacitance and ESR are possible by choosing a much larger C_{OUT} and a larger ESR. In this case, a small 1 µF ceramic capacitor and two 150 µF Sanyo POSCAP™ capacitors are selected. The low ESR ceramic capacitor helps to suppress the high frequency overshoot at the output. POSCAP has low ESR and high capacitance in a relatively small package. Ceramic capacitors can also be used. Generally, bigger ceramic capacitors are more expensive.

The next step is to choose a Schottky diode. The average and rms diode currents are calculated to be 1.0 A and 1.3 A, respectively, using Equations 14 and 15. A Vishay SSA33L Schottky diode meets the current and thermal requirements and is an excellent choice.

The power MOSFET must be chosen based on threshold voltage (V_T), on resistance (R_{DSON}), maximum voltage and current ratings, and gate charge. The rms current through the MOSFET is given by Equation 18 as 1.1 A. The Vishay Si7882DP is a 20 V n-channel power MOSFET that meets the current and thermal requirements. It comes in a PowerPAK® package and offers low R_{DSON} and gate charge. At V_{GS} = 2.5 V, the on resistance, R_{DSON}, is 8 mΩ.

The loop-compensation components are chosen to be R_{COMP} = 9.1 kΩ and C_{COMP} = 1.7 nF from Equations 30 and 31, respectively. A roll-off capacitor of C2 = 120 pF is also added. The slope-compensation resistor is set to be R_S = 80 Ω from Equation 34.

Lastly, given the chosen components, the peak inductor current as set by the current limit circuitry is given by Equation 35 as $I_{L,PK}$ = 12 A. Thus, the maximum load current, assuming CCM operation, is given by Equation 36 as $I_{LOAD,MAX}$ = 8 A, which is safely above the 1.0 A load current requirement for this design example. Note that the current limit is a strong function of R_{CS}, which can vary part to part and with temperature. In addition, note that R_{CS} can be implemented with an external current-sense resistor or with the R_{DSON} of a MOSFET. Variations in R_{CS} and the other parameters in Equations 35 and 36 must be taken into account if precise current limiting is necessary. Due to the parasitic resistance of PCB traces, R_S might need to be adjusted on the actual circuit board to achieve the desired current limit. Keep in mind that R_S must be less than 1.6 kΩ. Using a MOSFET with a different R_{DSON} or adjusting R_{CS} can also set the current limit to the desired level.

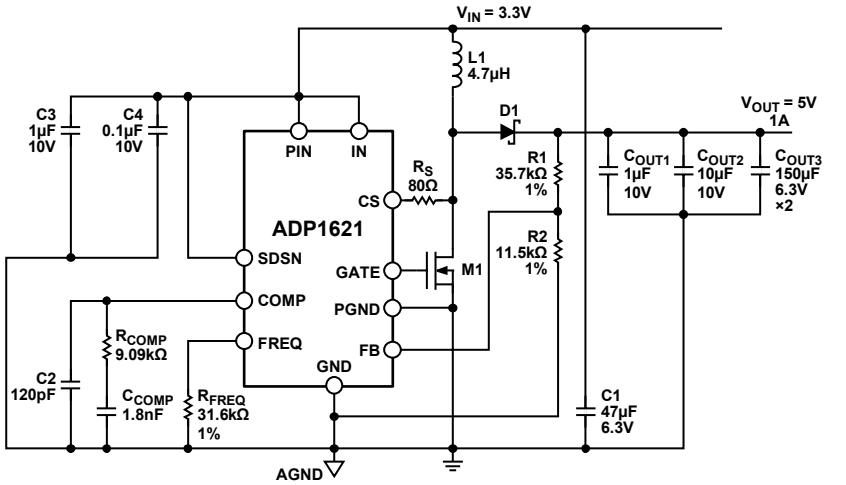


Figure 33. Typical Boost Converter Application Circuit

BOOTSTRAPPED BOOST CONVERTER

The inputs of the ADP1621 can be driven from the step-up converter output voltage to improve efficiency for low input voltages. For low input voltages, bootstrapped operation improves efficiency with heavy loads by increasing the available gate drive voltage, thus reducing the on resistance of the MOSFET. However, because the internal circuitry is driven from IN, the ADP1621 quiescent current and gate drive current supplied from the input increases due to the step-up ratio and the conversion efficiency loss.

The circuit shown in Figure 1 shows a bootstrapped boost converter, where V_{IN} = 3.3 V and V_{OUT} = 5 V. To ensure that the circuit starts, make sure that the input voltage minus the forward-voltage drop of the diode is greater than the UVLO voltage and the gate threshold voltage of the MOFSET. In this example, the MOSFET has a gate threshold voltage of 2.5 V. The regulator shown in Figure 1 is very similar to that shown in Figure 33, which is a standard boost without bootstrapping. Because the same MOSFET and inductor are used in both circuits and the input and output conditions are the same, the compensation components remain unchanged.

Figure 34 shows a bootstrapped application circuit for output voltages greater than 5.5 V. In this case, the output is 12 V. Notice that a resistor, R3, of 700 Ω is placed between V_{OUT} and the IN and PIN pins to limit the input currents because the IN and PIN pins are regulated to 5.5 V. A diode, D2, is placed between V_{IN} and the IN/PIN pins to supply the necessary quiescent current to start the ADP1621. Once the ADP1621 starts and the output voltage reaches 12 V, the quiescent current stops flowing through D2 and is supplied by the output. Keep in mind that the dynamic supply current to PIN increases as the switching frequency increases because more gate drive is needed for a higher switching frequency. Therefore, R3 needs to be set appropriately. The PIN supply current can be approximated by

$$I_{PIN} = f_{SW} \times Q_G \quad (45)$$

where I_{PIN} is the PIN supply current, f_{SW} is the switching frequency, and Q_G is the gate charge of a particular MOSFET.

An alternative implementation to Figure 34 is shown in Figure 35, where an NPN transistor is used to supply the necessary current to the input PIN at various loads, but the gate drive voltage is limited to approximately 4.8 V (one diode drop below the voltage at IN). Signal Diodes D2 and D3 help to provide the necessary quiescent current to start the ADP1621. Once the ADP1621 starts, the current stops flowing through these two diodes because the voltages at PIN and IN are approximately 4.8 V and 5.5 V, respectively. One advantage of this technique is that Q1 provides enough current to the gate driver at any switching frequency with a wide range of MOSFETs that have different gate charge specifications.

Notice that the output capacitor, C_{OUT2} in Figure 34 and Figure 35, is a large aluminum electrolytic capacitor, both in physical size and capacitance. Such capacitors are very cheap relative to ceramic capacitors (such as Sanyo POSCAP) or aluminum polymer capacitors. The ADP1621 can work with a wide range of capacitor types.

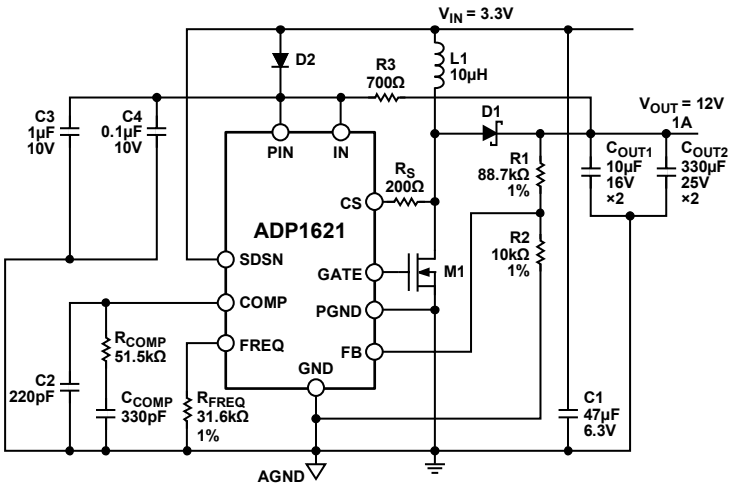


Figure 34. Bootstrapped Application Circuit for V_{OUT} > 5.5 V

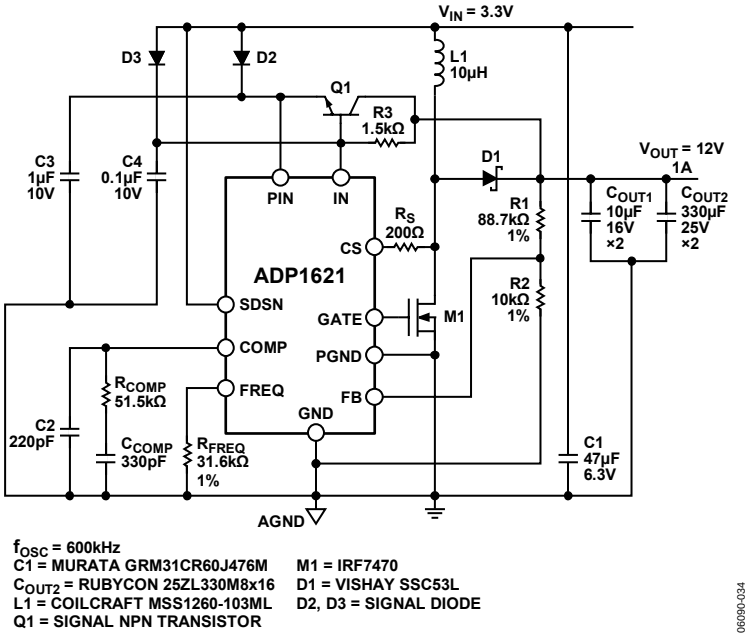


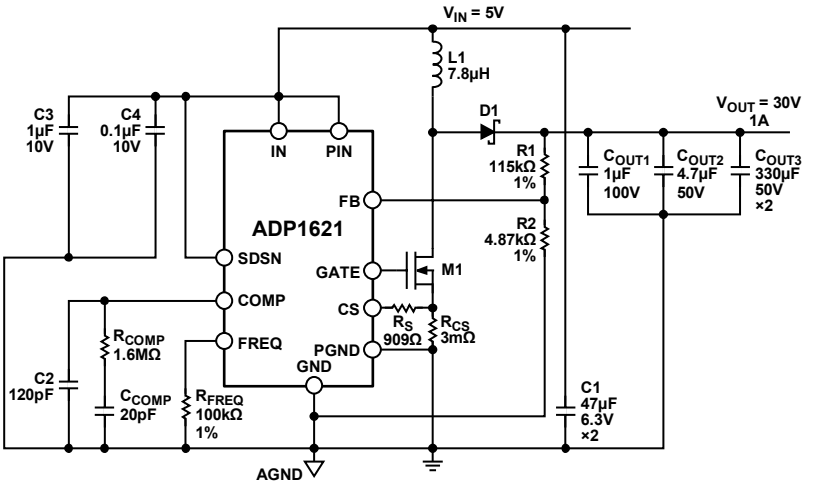
Figure 35. Bootstrapped Application Circuit for V_{OUT} > 5.5 V

Low Input and High Output Boost Converter

Figure 36 shows a typical application boost converter circuit that operates at a switching frequency of 200 kHz with V_{IN} = 5 V and V_{OUT} = 30 V with a 1 A load. The duty cycle for this circuit is about 83%. A higher switching frequency can be selected, but the switching power loss in the MOSFET increases and a bigger MOSFET is needed. For switch-node voltages greater than 30 V, a sense resistor, R_{CS}, is needed because the absolute maximum voltage at CS is 33 V.

High Input Voltage Boost Converter Circuit

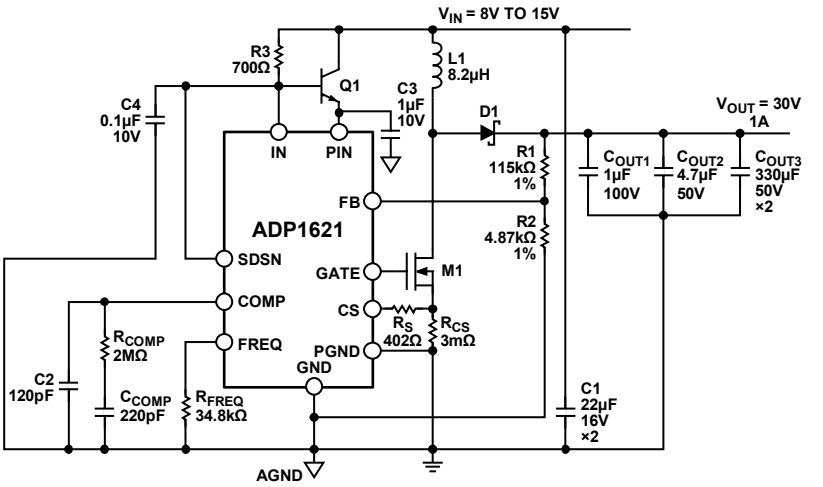
Input voltages higher than 5.5 V are possible with the addition of a resistor and an NPN transistor, as shown in Figure 37, or just with a single resistor, as shown in Figure 38. When there is a wide input voltage range, it is sometimes desirable to use the pass NPN transistor, as shown in Figure 37. If the input voltage range is narrow, a single resistor connecting to the IN and PIN pins is sufficient, as shown in Figure 38. In Figure 37, Resistor R3 limits the current going into IN, and there is power loss in this resistor. The voltages at IN and PIN are both clamped to about 5.5 V, which can rise to as high as 5.9 V when the shunt current is 30 mA. Refer to Figure 9 for the I-V characteristics of the shunt regulators. Ensure that Resistor R3 is physically large enough to handle the power dissipation. For switch-node voltages higher than 30 V, a current-sense resistor is needed and the CS pin senses the voltage across the sense resistor.



f_{OSC} = 200kHz
C1 = MURATA GRM31CR60J476M
C_{OUT1} = MURATA GRM31CR72A10
C_{OUT2} = MURATA GRM55ER71H475K
C_{OUT3} = RUBYCON 50ZL330M10x23
M1 = VISHAY SUD50N06-07L
D1 = IRF 15TQ060
L1 = COILCRAFT DO501DH-782ML

06090-035

Figure 36. Low Input, High Output Boost Converter



f_{OSC} = 560kHz
C1 = MURATA GRM32ER61C226K
C_{OUT1} = MURATA GRM31CR72A105K
C_{OUT2} = MURATA GRM55ER71H475K
C_{OUT3} = RUBYCON 50ZL220M10x23
M1 = IRF7470
Q1 = SIGNAL NPN TRANSISTOR
D1 = MBRB7H50
L1 = COILCRAFT MSS1260-822ML

06090-036

Figure 37. High Input Voltage and High Output Voltage Converter

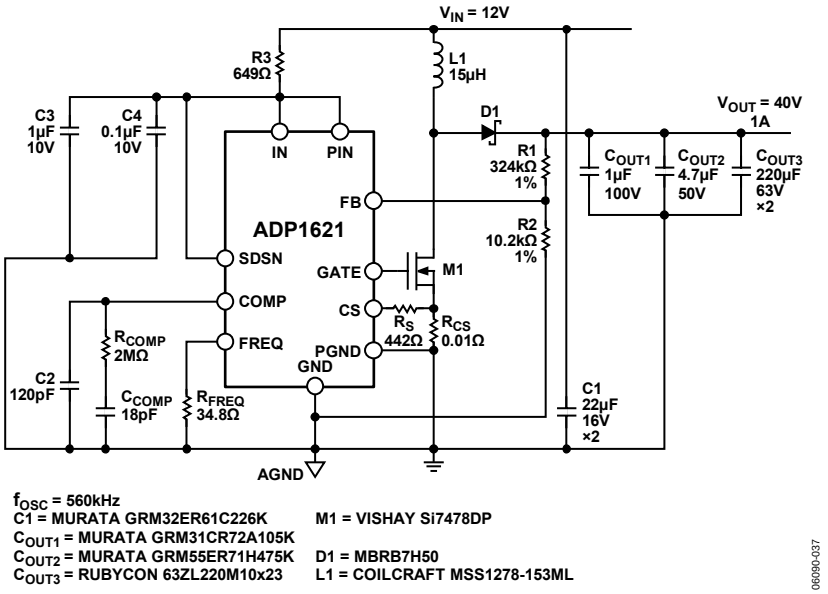


Figure 38. High Input Voltage and High Output Voltage Converter

SEPIC CONVERTER CIRCUIT

A single-ended primary inductance converter (SEPIC) topology is shown in Figure 39. This topology is useful for an unregulated input voltage, where the regulated output voltage falls within the input voltage range.

The input and output are dc-isolated by a coupling capacitor, C5. L1 and L2 are coupled inductors with a 1:1 turn ratio, which saves space on the PCB. In steady state, the average voltage across C5 is the input voltage. When the MOSFET turns on and the diode turns off, the input voltage provides energy to L1, and C5 provides energy to L2. The output capacitor, C_{OUT}, supplies the load current during this time. When the MOSFET turns off and the diode turns on, the energy in L1 and L2 is released to charge the output capacitor, C_{OUT}, and the coupling capacitor, C5, as well as to supply current to the load.

LOW VOLTAGE POWER-INPUT CIRCUIT

The ADP1621 can be configured to run from a low voltage (as low as 1 V) power input. The power source generally needs to have a high current capability, such as a fuel cell. Figure 40 illustrates such an application, where the voltage of the power input is 1 V and the voltage of the chip supply to the IN and PIN pins is provided by an auxiliary low power source.

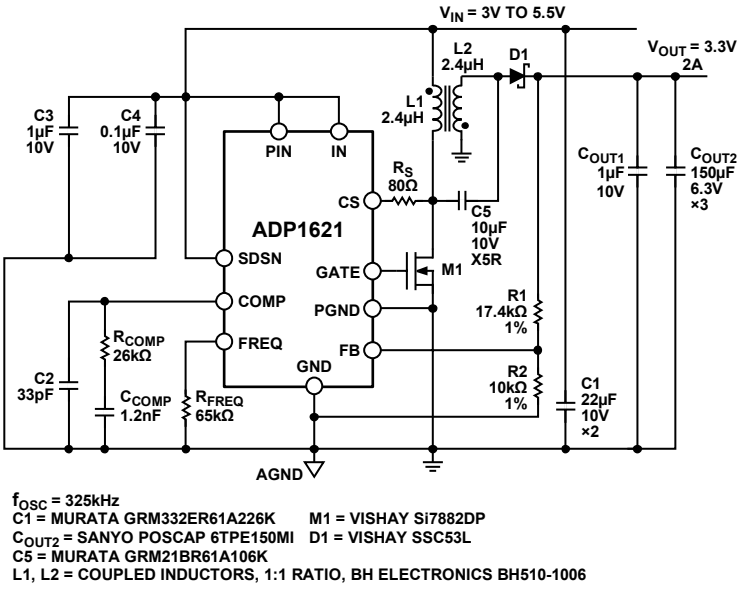


Figure 39. A SEPIC DC/DC Converter

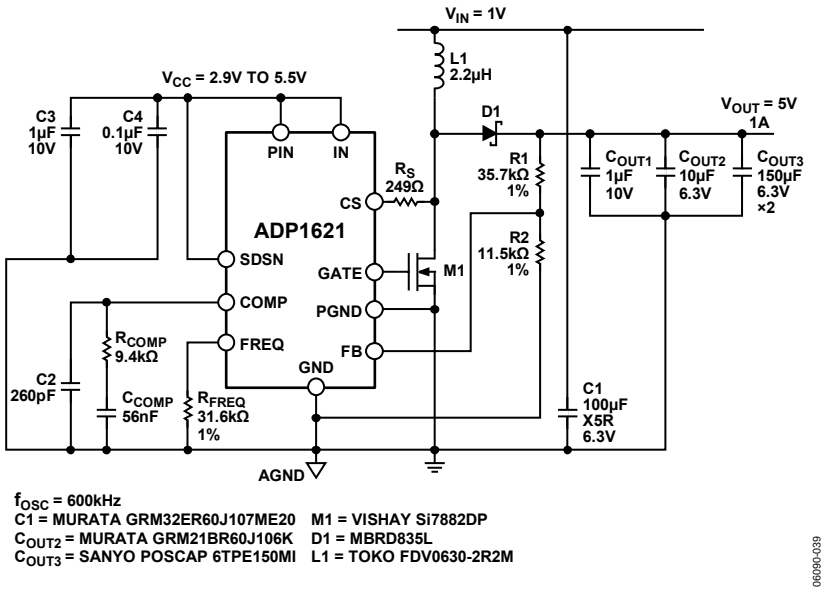


Figure 40. Low Voltage Power-Input Application Circuit

LED DRIVER APPLICATION CIRCUITS

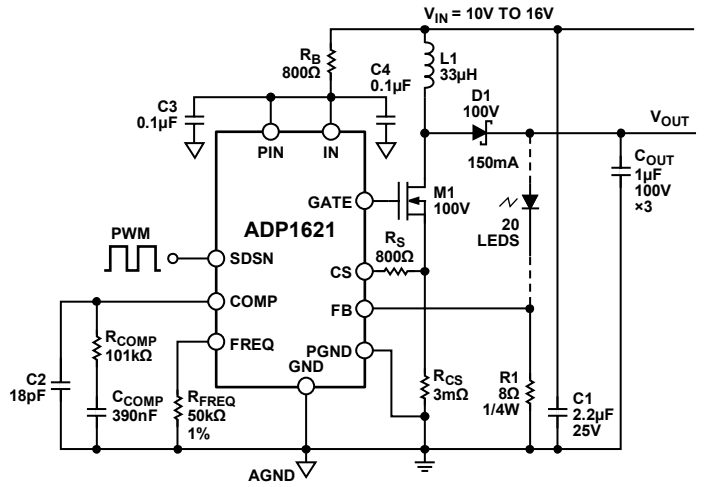
The ADP1621 can be used as an LED driver. Two LED application circuits are shown in Figure 41 and Figure 42, where each circuit is driving 20 white LEDs in series. Each white LED has a typical current of 150 mA at a typical forward voltage of 4.0 V, with a maximum voltage of 4.5 V over the temperature range of −40°C to +125°C.

Two methods for dimming the brightness of the LEDs are shown in Figure 41 and Figure 42. In Figure 41, a PWM signal is fed to the SDSN pin to turn the ADP1621 controller on and off. As a result, the LED current is turned on and off, and the average LED current is dependent on the PWM duty cycle. The advantage of this method is that no current flows through the LEDs during the PWM off cycle. In addition, when the ADP1621 is on, the forward current through the LEDs is constant, which guarantees constant color emission across the entire dimming range. Because the soft start period is fixed at 2048 oscillator cycles, the PWM frequency range is limited.

As shown in Figure 41, because the natural switching frequency chosen is 400 kHz, the useful PWM frequency range is 90 Hz to 195 Hz. However, when driving fewer LEDs, the ADP1621 can be set to run at a faster frequency, increasing the maximum PWM frequency. The PWM duty cycle can be between 5% and 95%. A higher PWM duty cycle produces a higher average LED current.

Another method for driving the LEDs is shown in Figure 42, where the PWM signal is filtered by an RC low-pass filter and is fed to the FB node. The effective FB voltage at the bottom of the LED string is modulated in an analog manner by the PWM duty cycle. Thus, the average current through the LEDs is modulated accordingly. Unlike the case depicted in Figure 41, a higher duty cycle produces a lower average LED current using the filtered PWM scheme in Figure 42. The advantage of this circuit is that the PWM frequency can be in the range between 90 Hz and 100 kHz, and the duty cycle can be between 5% and 95%. The disadvantage of this method is that the forward current through the LEDs is directly modified to control the brightness of the LEDs. Because the wavelength of the light emitted from an LED is a weak function of its forward current, perfect color purity across the entire dimming range cannot be guaranteed.

If PCB space is a constraint, smaller inductors can be selected for the circuits shown in Figure 41 and Figure 42. For example, a 4.7 µH inductor can be used, and a 200 kHz switching frequency can be selected. However, with this small inductor, the system operates in DCM, which is slightly less efficient than operating in CCM.



f_{OSC} = 400kHz
C1 = MURATA GRM31MR71E225K M1 = VISHAY Si4482DY
C_{OUT} = MURATA GRM31CR72A105K D1 = IRF 10MQ100
L1 = COILCRAFT MSS1038-333NL

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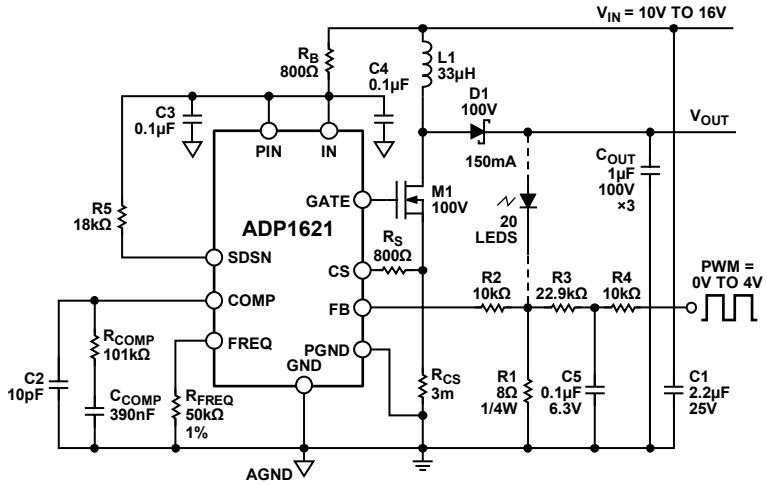
Figure 41. 20-Series LED Driver with PWM at SDSN



f_{OSC} = 400kHz
C1 = MURATA GRM31MR71E225K M1 = VISHAY Si4482DY
C_{OUT} = MURATA GRM31CR72A105K D1 = IRF 10MQ100
L1 = COILCRAFT MSS1038-333NL

06090-041

Figure 42. 20-Series LED Driver with Filtered PWM

RELATED PARTS

Table 6.

Part Number	Description	Comments
ADP1610	Current-mode PWM step-up controller	Maximum output = 12 V; PWM frequency = 700 kHz or 1.2 MHz; integrated 1.2 A, 0.2 Ω MOSFET power switch
ADP1611	Current-mode PWM step-up controller	Maximum output = 20 V; PWM frequency = 700 kHz or 1.2 MHz; integrated 1.2 A, 0.2 Ω MOSFET power switch

OUTLINE DIMENSIONS

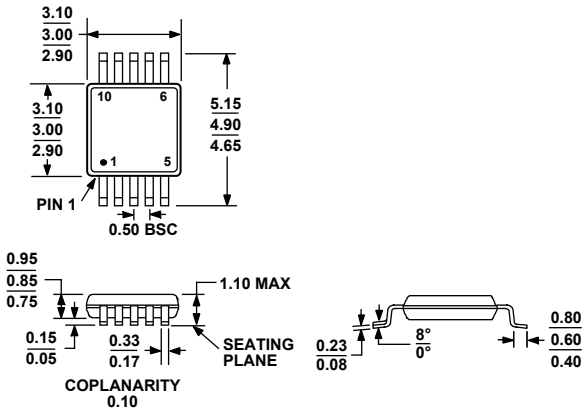


Figure 43. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADP1621ARMZ[1]	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	50	L3M
ADP1621ARMZ-R7[1]	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	1,000	L3M
ADP1621-EVAL		Evaluation Board		1	

[1] Z = Pb-free part.

NOTES

D06090-0-12/06(A)