ADM690A/ADM692A/ADM802L/M/ADM805L/M–SPECIFICATIONS

(V_{CC} = 4.75 V to 5.5 V (ADM690A/ADM802L/ADM805L), V_{CC} = 4.5 V to 5.5 V, (ADM692A/ADM802M/ADM805M), V_{BATT} = +2.8 V, T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V_{CC}/V_{BATT} OPERATION[1]					
V_{CC} Operating Voltage Range	1.0		5.5	V	
Supply Current (Excludes I_{OUT})		70	100	µA	
Supply Current in Battery Backup Mode		0.05	1.0	µA	V_{CC} = 0 V, V_{BATT} = 2.8 V
Battery Standby Current					5.5 V > V_{CC} > V_{BATT} + 0.2 V
(+ = Discharge, – = Charge)	–0.1		+0.02	µA	
V_{OUT} Output Voltage	V_{CC} – 0.02	V_{CC} – 0.01		V	I_{OUT} = 5 mA
	V_{CC} – 0.5	V_{CC} – 0.05		V	I_{OUT} = 50 mA
		V_{CC} – 0.02		V	I_{OUT} = 250 mA
V_{OUT} in Battery Backup Mode	V_{BATT} – 0.05	V_{BATT} – 0.002		V	I_{OUT} = 250 µA, V_{CC} < V_{BATT} – 0.2 V
Battery Switchover Threshold		20		mV	Power Up
		–20		mV	Power Down
Battery Switchover Hysteresis		40		mV	
RESET THRESHOLD					
Reset Voltage Threshold					
ADM690A, ADM802L, ADM805L	4.5	4.65	4.75	V	
ADM692A, ADM802M, ADM805M	4.25	4.4	4.5	V	
ADM802L	4.55		4.7	V	T_A = 25°C, V_{CC} Falling
ADM802M	4.30		4.45	V	T_A = 25°C, V_{CC} Falling
Reset Threshold Hysteresis		40		mV	
Reset Timeout Delay	140	200	280	ms	
$\overline{\text{RESET}}$ Output Voltage	V_{CC} – 1.5			V	I_{SOURCE} = 800 µA
			0.4	V	I_{SINK} = 3.2 mA
			0.3	V	I_{SINK} = 100 µA, V_{CC} = 1 V
RESET Output Voltage	0.8			V	I_{SOURCE} = 4 µA, V_{CC} = 1.1 V
	V_{CC} – 1.5			V	ADM805L/M, I_{SOURCE} = 800 µA
			0.4	V	ADM805L/M, I_{SINK} = 3.2 mA
WATCHDOG TIMER					
Watchdog Timeout Period	1.0	1.6	2.25	s	
WDI Input Pulse Width	50			ns	V_{IL} = 0.4, V_{IH} = 0.8 (V_{CC})
WDI Input Threshold					
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current			10	µA	WDI = V_{CC}
	–10			µA	WDI = 0 V
POWER FAIL DETECTOR					
PFI Input Threshold	1.20	1.25	1.30	V	ADM690A, ADM692A, ADM805L/M
	1.225	1.25	1.275	V	ADM802L/M
PFI Input Current	–25	0.01	+25	nA	
$\overline{\text{PFO}}$ Output Voltage	V_{CC} – 1.5			V	I_{SOURCE} = 800 µA
			0.4	V	I_{SINK} = 3.2 mA

NOTES

[1]Either V_{CC} or V_{BATT} can be 0 V if the other > +2.0 V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

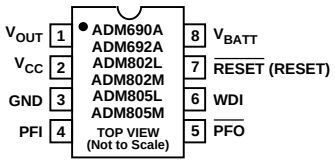
V_{CC} . . . . . –0.3 V to +6 V
V_{BATT} . . . . . –0.3 V to +6 V
All Other Inputs . . . . . –0.3 V to V_{CC} + 0.3 V
Input Current
  V_{CC} . . . . . 200 mA
  V_{BATT} . . . . . 50 mA
  GND . . . . . 20 mA
Digital Output Current . . . . . 20 mA
Power Dissipation, N-8 DIP . . . . . 400 mW
  θ_{JA} Thermal Impedance . . . . . 120°C/W
Power Dissipation, SO-8 SOIC . . . . . 500 mW
  θ_{JA} Thermal Impedance . . . . . 110°C/W
Operating Temperature Range
  Industrial (A Version) . . . . . –40°C to +85°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
  Vapor Phase (60 sec) . . . . . +215°C
  Infrared (15 sec) . . . . . +220°C
Storage Temperature Range . . . . . –65°C to +150°C
ESD Rating . . . . . >4 kV

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option
ADM690AAN	–40°C to +85°C	N-8
ADM690AARN	–40°C to +85°C	SO-8
ADM690AARM	–40°C to +85°C	RM-8
ADM692AAN	–40°C to +85°C	N-8
ADM692AARN	–40°C to +85°C	SO-8
ADM802LAN	–40°C to +85°C	N-8
ADM802LARN	–40°C to +85°C	SO-8
ADM802MAN	–40°C to +85°C	N-8
ADM802MARN	–40°C to +85°C	SO-8
ADM805LAN	–40°C to +85°C	N-8
ADM805LARN	–40°C to +85°C	SO-8
ADM805MAN	–40°C to +85°C	N-8
ADM805MARN	–40°C to +85°C	SO-8

PIN CONFIGURATIONS



PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power Supply Input: +5 V Nominal.
V_{BATT}	Backup Battery Input. As V_{CC} falls below the reset threshold and below V_{BATT} by 20 mV, V_{BATT} will be switched to V_{OUT}. On power-up as V_{CC} rises to 20 mV above V_{BATT}, V_{OUT} will be switched back to V_{CC}.
V_{OUT}	Output Voltage. When V_{CC} is above the reset threshold, V_{OUT} is connected to V_{CC} through an on chip switch. When V_{CC} is below the reset threshold, the higher of V_{CC} or V_{BATT} is connected to V_{OUT}.
GND	0 V. Ground reference for all signals.
PFI	Power Fail Comparator Input. If PFI is less than 1.25 V, the power fail output $\overline{PFO}$ goes low. If unused, PFI should be connected to V_{CC} or GND.
$\overline{PFO}$	Power Fail Comparator Output. If PFI is less than 1.25 V, the power fail output $\overline{PFO}$ goes low.
$\overline{RESET}$	Logic Output. $\overline{RESET}$ goes low if 1. V_{CC} falls below the Reset Threshold 2. The watchdog timer is not serviced within its timeout period (1.6 seconds) The reset threshold is typically 4.65 V for the ADM690A/ADM802L/ADM805L and 4.4 V for the ADM692A/ADM802M/ADM805M. $\overline{RESET}$ remains low for 200 ms after V_{CC} returns above the threshold. $\overline{RESET}$ also goes low for 200 ms if the watchdog timer is enabled but not serviced within its timeout period.
RESET	Active high RESET output (ADM805L/M only). This is the inverse of $\overline{RESET}$. The asserted (high) level is V_{CC} or V_{BATT} whichever is higher.
WDI	Watchdog Input. WDI is a three level input. If WDI remains either high or low for longer than 1.6 s, (RESET) (RESET) is activated. The timer resets with each transition on the WDI line. The watchdog timer may be disabled if WDI is left floating or is connected to a high impedance three stated logic output.

Typical Performance Curves

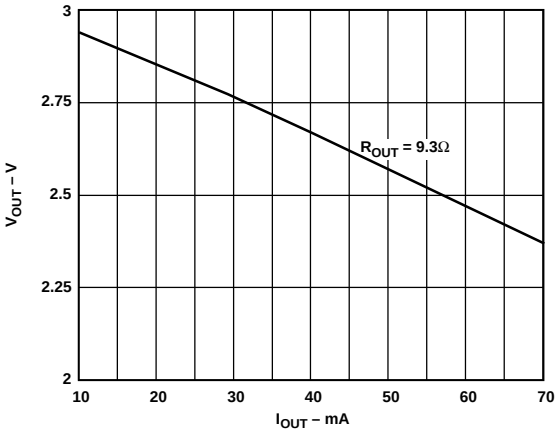


Figure 1. Output Voltage vs. Load Current in Battery Backup

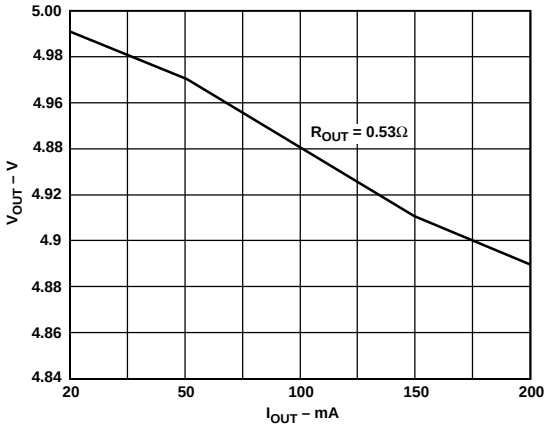


Figure 4. Output Voltage vs. Load Current in Normal Operation

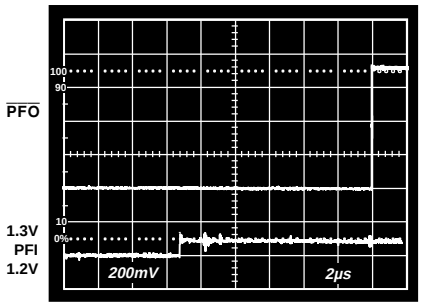


Figure 2. Power Fail Comparator Response Time L → H

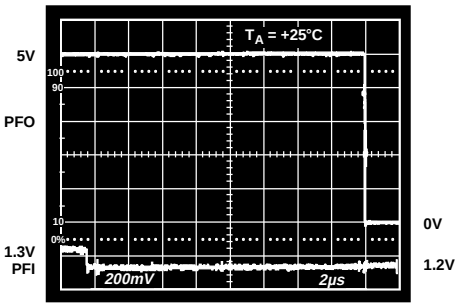


Figure 5. Power Fail Comparator Response Time H → L

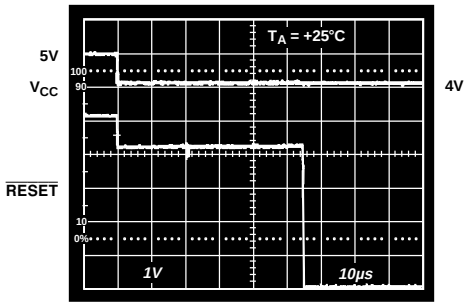


Figure 3. ADM690A $\overline{RESET}$ Response Time

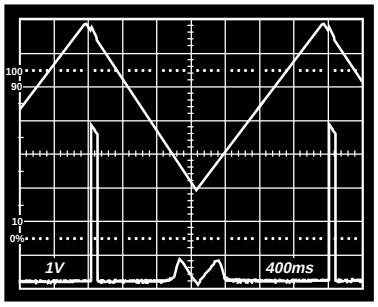


Figure 6. $\overline{RESET}$ Output Voltage vs. V_{CC}

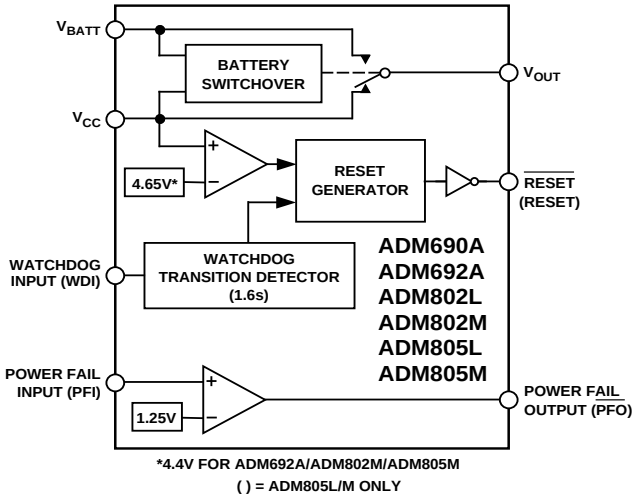


Figure 7. Functional Block Diagram

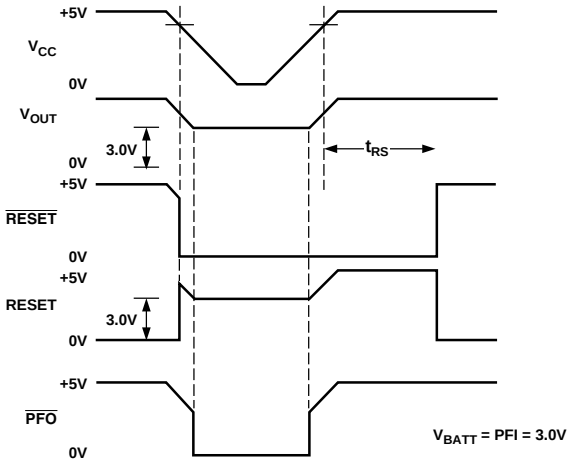


Figure 8. Timing Diagram

POWER FAIL $\overline{\text{RESET}}$, RESET

$\overline{\text{RESET}}$ is an active low output which provides a $\overline{\text{RESET}}$ signal to the microprocessor whenever V_{CC} is at an invalid level. When V_{CC} falls below the reset threshold, the $\overline{\text{RESET}}$ output is forced low. The nominal reset voltage threshold is 4.65 V (ADM690A/ADM802L/ADM805L or 4.4 V ADM692A/ADM802M/ADM805M.

On power-up $\overline{\text{RESET}}$ will remain low for 200 ms after V_{CC} rises above the reset threshold. This allows time for the power supply and microprocessor to stabilize. On power-down, the $\overline{\text{RESET}}$ output remains low with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition.

The guaranteed minimum and maximum thresholds are as follows:
ADM690A/ADM802L/ADM805L: 4.5 V and 4.75 V

ADM692A: 4.25 V and 4.5 V.

ADM802L: 4.55 V and 4.7 V

ADM802M: 4.3 V and 4.45 V

The ADM805L and ADM805M contain an active high reset output. This is the complement of $\overline{\text{RESET}}$ and is intended for processors requiring an active high RESET signal.

The guaranteed minimum and maximum thresholds for the ADM805 are:
ADM805L: 4.5 V and 4.75 V

ADM805M: 4.25 V and 4.5 V.

Watchdog Timer $\overline{\text{RESET}}$, RESET

The watchdog timer circuit monitors the activity of the microprocessor in order to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the Watchdog Input (WDI) line. If this line is not toggled within 1.6 seconds, a RESET pulse is generated. The watchdog timeout period restarts with each transition on the WDI pin. To ensure that the watchdog timer does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum timeout period. If WDI remains permanently either high or low, reset pulses will be issued after each timeout period (1.6 s). The watchdog monitor can be deactivated by floating the Watchdog Input (WDI) or by connecting it to midsupply.

BATTERY SWITCHOVER SECTION

During normal operation with V_{CC} higher than the reset threshold, V_{CC} is internally switched to V_{OUT} via an internal PMOS transistor switch. This switch has a typical on-resistance of less than 1 Ω and can supply up to 100 mA at the V_{OUT} terminal. Once V_{CC} falls below the reset threshold, the higher of V_{CC} or V_{BATT} is switched to V_{OUT}. This means that V_{BATT} connects to V_{OUT} only when V_{CC} is below the reset threshold and V_{BATT} is greater than V_{CC}.

V_{OUT} is normally used to drive a RAM memory bank which may require instantaneous currents of greater than 100 mA. If this is the case, then a bypass capacitor should be connected to V_{OUT}. The capacitor will provide the peak current transients to the RAM. A capacitance value of 0.1 µF or greater may be used.

A 9 Ω MOSFET switch connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. The supply current in battery backup is typically 0.05 µA.

Typically 3 V batteries are used as the backup supply. High value capacitors, either standard electrolytic or the farad size double layer capacitors, can also be used for short-term memory back up. A small charging current of typically 10 nA (0.1 µA max) flows out of the V_{BATT} terminal. This current is useful for maintaining rechargeable batteries in a fully charged condition. This extends the life of the back up battery by compensating for its self discharge current. Also note that this current poses no problem when lithium batteries are used for back up since the maximum charging current (0.1 µA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, V_{BATT} should be connected to GND and V_{OUT} should be connected to V_{CC}.

Table I. Input and Output Status in Battery Backup Mode

Signal	Status
V_{OUT}	V_{OUT} is connected to V_{BATT} via an internal PMOS switch.
$\overline{RESET}$	Logic low.
RESET	Logic high (ADM805L, ADM805M). The open circuit output voltage is equal to V_{OUT}.
$\overline{PFI}$	The power fail comparator is disabled
$\overline{PFO}$	Logic low.
WDI	The watchdog timer is disabled

Power Fail Comparator

The power fail comparator is an independent comparator that may be used to monitor the input power supply. The comparator's inverting input is internally connected to a 1.25 V reference voltage. The noninverting input is available at the PFI input. This input may be used to monitor the input power supply via a resistive divider network. When the voltage on the PFI input drops below 1.25 V, the comparator output ($\overline{PFO}$) goes low indicating a power failure. For early warning of power failure the comparator may be used to monitor the preregulator input simply by choosing an appropriate resistive divider network. The $\overline{PFO}$ output can be used to interrupt the processor so that a shutdown procedure is implemented before the power is lost.

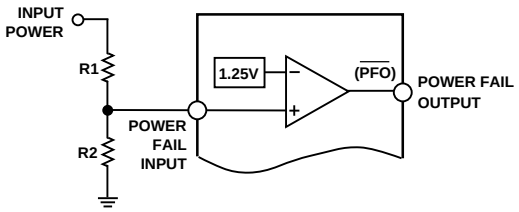


Figure 9. Power Fail Comparator

Adding Hysteresis to the Power Fail Comparator

For increased noise immunity, hysteresis may be added to the power fail comparator. Since the comparator circuit is non-inverting, hysteresis can be added simply by connecting a resistor between the $\overline{PFO}$ output and the PFI input as shown in Figure 10. When $\overline{PFO}$ is low, resistor R3 sinks current from the summing junction at the PFI pin. When $\overline{PFO}$ is high, resistor R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Further noise immunity may be achieved by connecting a capacitor between PFI and GND.

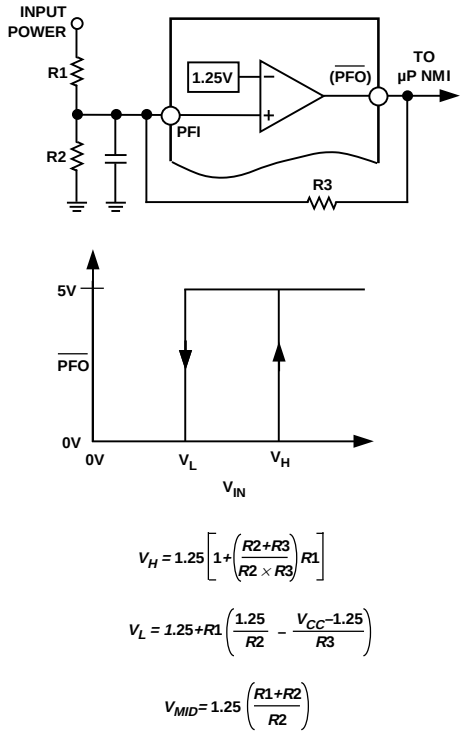


Figure 10. Adding Hysteresis to the Power Fail Comparator

TYPICAL APPLICATIONS

Figure 11 shows a typical power monitoring, battery backup application. V_{OUT} powers the CMOS RAM. Under normal operating conditions with V_{CC} present, V_{OUT} is internally connected to V_{CC}. If a power failure occurs, V_{CC} will decay and V_{OUT} will be switched to V_{BATT} thereby maintaining power for the CMOS RAM. A $\overline{RESET}$ pulse is also generated when V_{CC} falls below the reset threshold.

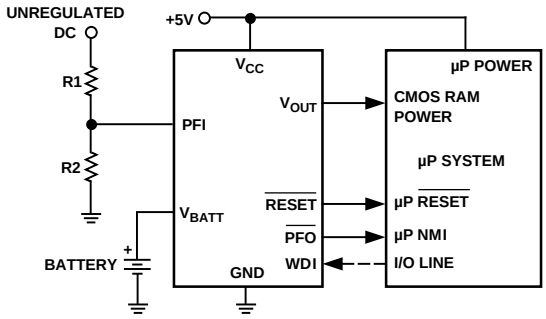


Figure 11. Typical Application Circuit

The watchdog timer input (WDI) monitors an I/O line from the µP system. This line must be toggled once every 1.6 seconds to verify correct software execution. Failure to toggle the line indicates that the µP system is not correctly executing its program and may be tied up in an endless loop. If this happens, a reset pulse is generated to initialize the processor.

If the watchdog timer is not needed, the WDI input should be left floating.

The Power Fail Input, PFI, monitors the input power supply via a resistive divider network. The voltage on the PFI input is compared with a precision 1.25 V internal reference. If the input voltage drops below 1.25 V, a power fail output ($\overline{PFO}$) signal is generated. This warns of an impending power failure and may be used to interrupt the processor so that the system may be shut down in an orderly fashion. The resistors in the sensing network are ratioed to give the desired power fail threshold voltage V_T.

$$V_T = (1.25\ R1/R2) + 1.25\ V$$

$$R1/R2 = (V_T/1.25) - 1$$

Alternate Watchdog Input Drive Circuits
The watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer. When three-stated, the WDI input will float thereby disabling the watchdog timer.

High Capacity Backup Capacitors
High capacity (0.1 µF or greater) capacitors may be used as a backup power source. A typical application is shown in Figure 12.

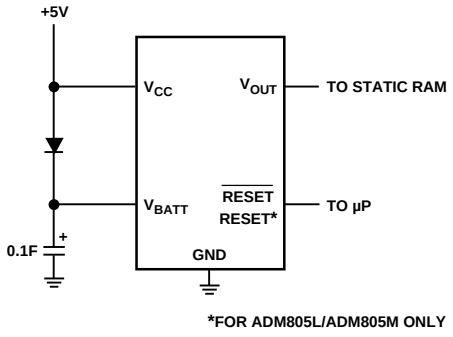


Figure 12. High Capacity Capacitor

Operation Without a Backup Supply
If a backup power source is not used, V_{BATT} should be connected to GND and V_{OUT} should be connected to V_{CC}.

Replacing the Backup Battery
The backup battery may be replaced without any danger of spurious resetting when V_{CC} is present. Since V_{CC} is above the reset threshold, a reset will not occur even if V_{BATT} is floating while a replacement battery is being inserted. This differs from older generation products where leakage currents flowing out V_{BATT} could cause spurious resetting during battery replacement.

µPs With Bidirectional $\overline{RESET}$
In order to prevent contention for microprocessors with a bidirectional reset line, a current limiting resistor should be inserted between the ADM69xA/ADM80xx $\overline{RESET}$ output pin and the µP reset pin. This will limit the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7 kΩ. If the reset output is required for other uses, then it should be buffered as shown in Figure 13.

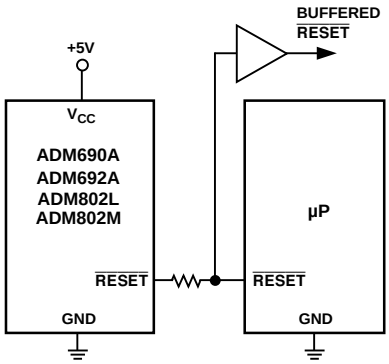
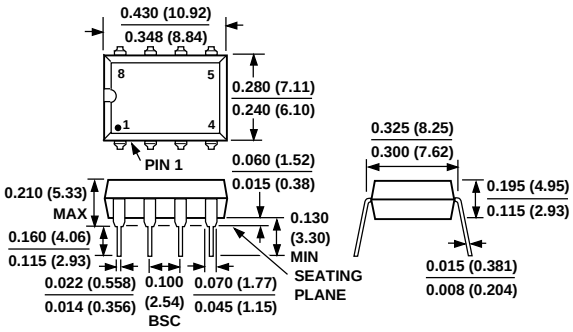


Figure 13. Bidirectional Reset

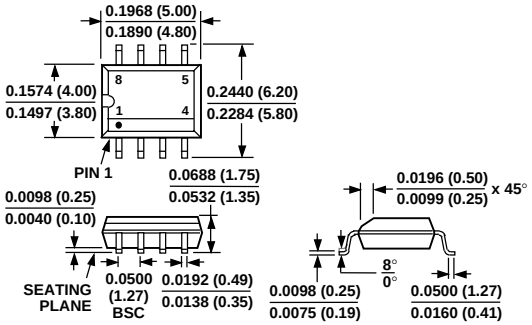
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

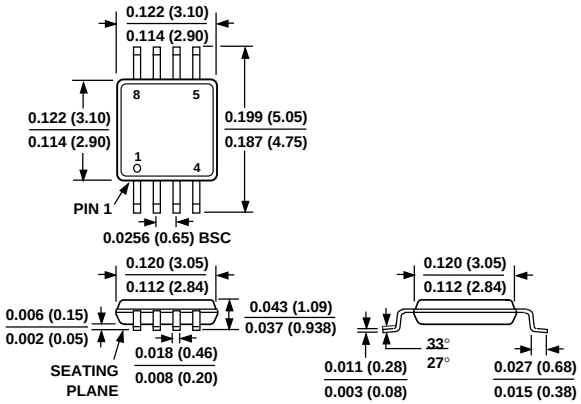
8-Pin Plastic DIP
(N-8)



8-Lead SOIC
(SO-8)



8-Lead MicroSOIC
(RM-8)



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