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# SPECIFICATIONS

## 3.3 V SPECIFICATIONS

$V_S$ = 3.3 V, $V_{CM}$ = 1.65 V, $R_L$ = 200 Ω differential, $A_V$ = 6 dB, $C_L$ = 1 pF differential, f = 100 MHz, $T_A$ = 25°C; parameters specified ac-coupled differential input and differential output, unless otherwise noted.

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Bandwidth | $A_V$ = 6 dB, $V_{OUT}$ ≤ 1.0 V p-p | | 6750 | | MHz |
| | $A_V$ = 12 dB, $V_{OUT}$ ≤ 1.0 V p-p | | 6500 | | MHz |
| | $A_V$ = 15.5 dB, $V_{OUT}$ ≤ 1.0 V p-p | | 6250 | | MHz |
| Bandwidth for 0.1 dB Flatness | $V_{OUT}$ ≤ 1.0 V p-p | | 1000 | | MHz |
| Gain Accuracy | | | ±1 | | dB |
| Gain Supply Sensitivity | $V_S$ ± 5% | | 1.9 | | mdB/V |
| Gain Temperature Sensitivity | −40°C to +85°C | | 0.35 | | mdB/°C |
| Slew Rate | Rise, $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V step | | 11 | | V/ns |
| | Fall, $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V step | | 11 | | V/ns |
| Settling Time | 2 V step to 1% | | 2 | | ns |
| Overdrive Recovery Time | $V_{IN}$ = 4 V to 0 V step, $V_{OUT}$ ≤ ±10 mV | | <3 | | ns |
| Reverse Isolation (S12) | | | 70 | | dB |
| INPUT/OUTPUT CHARACTERISTICS | | | | | |
| Input Common-Mode Range | $A_V$ = 6 dB, 12 dB, and 15.5 dB | | 1.2 to 2 | | V |
| Output Common-Mode Range | | | 1.4 to 1.8 | | V |
| Maximum Output Voltage Swing | 1 dB compressed | | 4 | | V p-p |
| Output Common-Mode Offset | Referenced to VCC/2 | −100 | | +20 | mV |
| Output Common-Mode Drift | −40°C to +85°C | | 0.34 | | mV/°C |
| Output Differential Offset Voltage | | −20 | | +20 | mV |
| CMRR | | | 60 | | dB |
| Output Differential Offset Drift | −40°C to +85°C | | 1.5 | | mV/°C |
| Input Bias Current | | | ±5 | | µA |
| Input Resistance (Differential) | $A_V$ = 6 dB | | 200 | | Ω |
| | $A_V$ = 12 dB | | 100 | | Ω |
| | $A_V$ = 15.5 dB | | 67 | | Ω |
| Input Resistance (Single-Ended) | $A_V$ = 5.6 dB | | 158 | | Ω |
| | $A_V$ = 11.1 dB | | 96 | | Ω |
| | $A_V$ = 14.1 dB | | 74 | | Ω |
| Input Capacitance (Single-Ended) | | | 0.3 | | pF |
| Output Resistance (Differential) | | | 10 | | Ω |
| POWER INTERFACE | | | | | |
| Supply Voltage | | 2.8 | 3.3 | 5.2 | V |
| ENBL Threshold | Device disabled, ENBL low | | | 0.5 | V |
| | Device enabled, ENBL high | 1.5 | | | V |
| ENBL Input Bias Current | ENBL high | | 500 | | nA |
| | ENBL low | | −165 | | µA |
| Quiescent Current | ENBL high | | 70 | | mA |
| | ENBL low | | 5 | | mA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| NOISE/HARMONIC PERFORMANCE | | | | | |
| 10 MHz | | | | | |
| Second/Third Harmonic Distortion (HD2/HD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −107/−110 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −101/−107 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −106/−112 | | dBc |
| Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | +48/−100 | | dBm/dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | +52/−108 | | dBm/dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | +50/−104 | | dBm/dBc |
| Second-Order Intermodulation Distortion (IMD2) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −86 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −86 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −86 | | dBc |
| Noise Spectral Density, RTI (NSD) | $A_V$ = 6 dB | | 2.24 | | nV/√Hz |
| | $A_V$ = 12 dB | | 1.52 | | nV/√Hz |
| | $A_V$ = 15.5 dB | | 1.53 | | nV/√Hz |
| Noise Figure (NF) | $A_V$ = 6 dB | | 10.24 | | dB |
| | $A_V$ = 12 dB | | 8.66 | | dB |
| | $A_V$ = 15.5 dB | | 8.78 | | dB |
| 1 dB Compression Point, RTO (OP1dB) | $A_V$ = 6 dB | | 13.1 | | dBm |
| | $A_V$ = 12 dB | | 12.8 | | dBm |
| | $A_V$ = 15.5 dB | | 13.1 | | dBm |
| 100 MHz | | | | | |
| Second/Third Harmonic Distortion (HD2/HD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −108/−103 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −91/−99 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −89/−100 | | dBc |
| Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | +54/−112 | | dBm/dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | +53/−110 | | dBm/dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | +52/−108 | | dBm/dBc |
| Second-Order Intermodulation Distortion (IMD2) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −85 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −85 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −86 | | dBc |
| Noise Spectral Density, RTI (NSD) | $A_V$ = 6 dB | | 2.25 | | nV/√Hz |
| | $A_V$ = 12 dB | | 1.53 | | nV/√Hz |
| | $A_V$ = 15.5 dB | | 1.52 | | nV/√Hz |
| Noise Figure (NF) | $A_V$ = 6 dB | | 10.27 | | dB |
| | $A_V$ = 12 dB | | 8.69 | | dB |
| | $A_V$ = 15.5 dB | | 8.7 | | dB |
| 1 dB Compression Point, RTO (OP1dB) | $A_V$ = 6 dB | | 13 | | dBm |
| | $A_V$ = 12 dB | | 12.8 | | dBm |
| | $A_V$ = 15.5 dB | | 12.8 | | dBm |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 200 MHz | | | | | |
| Second/Third Harmonic Distortion (HD2/HD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −82/−87 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −72/−86 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −71/−86 | | dBc |
| Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite | | +46/−96 | | dBm/dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite | | +46/−96 | | dBm/dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite | | +46/−96 | | dBm/dBc |
| Second-Order Intermodulation Distortion (IMD2) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −85 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −73 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −70 | | dBc |
| Noise Spectral Density, RTI (NSD) | $A_V$ = 6 dB | | 2.36 | | nV/√Hz |
| | $A_V$ = 12 dB | | 1.64 | | nV/√Hz |
| | $A_V$ = 15.5 dB | | 1.51 | | nV/√Hz |
| Noise Figure (NF) | $A_V$ = 6 dB | | 10.65 | | dB |
| | $A_V$ = 12 dB | | 9.25 | | dB |
| | $A_V$ = 15.5 dB | | 8.49 | | dB |
| 500 MHz | | | | | |
| Second/Third Harmonic Distortion (HD2/HD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −68/−63 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −56/−62 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −57/−63 | | dBc |
| Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite | | +34/−72 | | dBm/dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite | | +36/−76 | | dBm/dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite | | +39/−82 | | dBm/dBc |
| Second-Order Intermodulation Distortion (IMD2) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −75 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −70 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −70 | | dBc |
| Noise Spectral Density, RTI (NSD) | $A_V$ = 6 dB | | 2.62 | | nV/√Hz |
| | $A_V$ = 12 dB | | 1.57 | | nV/√Hz |
| | $A_V$ = 15.5 dB | | 1.47 | | nV/√Hz |
| Noise Figure (NF) | $A_V$ = 6 dB | | 11.47 | | dB |
| | $A_V$ = 12 dB | | 8.93 | | dB |
| | $A_V$ = 15.5 dB | | 8.07 | | dB |

## 5 V SPECIFICATIONS

$V_S$ = 5.0 V, $V_{CM}$ = 2.5 V, $R_L$ = 200 Ω differential, $A_V$ = 6 dB, $C_L$ = 1 pF differential, f = 100 MHz, $T_A$ = 25°C; parameters specified ac-coupled differential input and differential output, unless otherwise noted.

**Table 2.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Bandwidth | $A_V$ = 6 dB, $V_{OUT}$ ≤ 1.0 V p-p | | 7000 | | MHz |
| | $A_V$ = 12 dB, $V_{OUT}$ ≤ 1.0 V p-p | | 6750 | | MHz |
| | $A_V$ = 15.5 dB, $V_{OUT}$ ≤ 1.0 V p-p | | 6500 | | MHz |
| Bandwidth for 0.1 dB Flatness | $V_{OUT}$ ≤ 1.0 V p-p | | 1000 | | MHz |
| Gain Accuracy | | | ±1 | | dB |
| Gain Supply Sensitivity | $V_S$ ± 5% | | 1.6 | | mdB/V |
| Gain Temperature Sensitivity | −40°C to +85°C | | 0.37 | | mdB/°C |
| Slew Rate | Rise, $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V step | | 11 | | V/ns |
| | Fall, $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V step | | 11 | | V/ns |
| Settling Time | 2 V step to 1% | | 2 | | ns |
| Overdrive Recovery Time | $V_{IN}$ = 4 V to 0 V step, $V_{OUT}$ ≤ ±10 mV | | <3 | | ns |
| Reverse Isolation (S12) | | | 70 | | dB |
| INPUT/OUTPUT CHARACTERISTICS | | | | | |
| Input Common-Mode Range | $A_V$ = 6 dB, 12 dB, and 15.5 dB | | 1.2 to 3.8 | | V |
| Output Common-Mode Range | | | 1.4 to 3 | | V |
| Maximum Output Voltage Swing | 1 dB compressed | | 8 | | V p-p |
| Output Common-Mode Offset | Referenced to VCC/2 | −100 | | +20 | mV |
| Output Common-Mode Drift | −40°C to +85°C | | 0.4 | | mV/°C |
| Output Differential Offset Voltage | | −20 | | +20 | mV |
| CMRR | | | 60 | | dB |
| Output Differential Offset Drift | −40°C to +85°C | | 1.5 | | mV/°C |
| Input Bias Current | | | ±5 | | µA |
| Input Resistance (Differential) | $A_V$ = 6 dB | | 200 | | Ω |
| | $A_V$ = 12 dB | | 100 | | Ω |
| | $A_V$ = 15.5 dB | | 67 | | Ω |
| Input Resistance (Single-Ended) | $A_V$ = 5.6 dB | | 158 | | Ω |
| | $A_V$ = 11.1 dB | | 96 | | Ω |
| | $A_V$ = 14.1 dB | | 74 | | Ω |
| Input Capacitance (Single-Ended) | | | 0.3 | | pF |
| Output Resistance (Differential) | | | 10 | | Ω |
| POWER INTERFACE | | | | | |
| Supply Voltage | | 2.8 | 5 | 5.2 | V |
| ENBL Threshold | Device disabled, ENBL low | | | 0.6 | V |
| | Device enabled, ENBL high | 1.5 | | | V |
| ENBL Input Bias Current | ENBL high | | 1 | | µA |
| | ENBL low | | −250 | | µA |
| Quiescent Current | ENBL high | | 80 | | mA |
| | ENBL low | | 6 | | mA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| NOISE/HARMONIC PERFORMANCE | | | | | |
| 10 MHz | | | | | |
| Second/Third Harmonic Distortion (HD2/HD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −111/−116 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −100/−104 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −105/−106 | | dBc |
| Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | +47/−98 | | dBm/dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | +50/−104 | | dBm/dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | +50/−104 | | dBm/dBc |
| Second-Order Intermodulation Distortion (IMD2) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −78 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −86 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −91 | | dBc |
| Noise Spectral Density, RTI (NSD) | $A_V$ = 6 dB | | 2.25 | | nV/√Hz |
| | $A_V$ = 12 dB | | 1.54 | | nV/√Hz |
| | $A_V$ = 15.5 dB | | 1.55 | | nV/√Hz |
| Noise Figure (NF) | $A_V$ = 6 dB | | 10.29 | | dB |
| | $A_V$ = 12 dB | | 8.77 | | dB |
| | $A_V$ = 15.5 dB | | 9.04 | | dB |
| 1 dB Compression Point, RTO (OP1dB) | $A_V$ = 6 dB | | 16.8 | | dBm |
| | $A_V$ = 12 dB | | 16.7 | | dBm |
| | $A_V$ = 15.5 dB | | 16.6 | | dBm |
| 100 MHz | | | | | |
| Second/Third Harmonic Distortion (HD2/HD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −108/−109 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −92/−103 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −89.5/−105 | | dBc |
| Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | +53/−110 | | dBm/dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | +53/−110 | | dBm/dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | +52/−108 | | dBm/dBc |
| Second-Order Intermodulation Distortion (IMD2) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −87 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −91 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −87 | | dBc |
| Noise Spectral Density, RTI (NSD) | $A_V$ = 6 dB | | 2.28 | | nV/√Hz |
| | $A_V$ = 12 dB | | 1.53 | | nV/√Hz |
| | $A_V$ = 15.5 dB | | 1.52 | | nV/√Hz |
| Noise Figure (NF) | $A_V$ = 6 dB | | 10.39 | | dB |
| | $A_V$ = 12 dB | | 8.73 | | dB |
| | $A_V$ = 15.5 dB | | 8.7 | | dB |
| 1 dB Compression Point, RTO (OP1dB) | $A_V$ = 6 dB | | 16.8 | | dBm |
| | $A_V$ = 12 dB | | 16.5 | | dBm |
| | $A_V$ = 15.5 dB | | 16.4 | | dBm |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 200 MHz | | | | | |
| Second/Third Harmonic Distortion (HD2/HD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −82/−87 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −72/−86 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −71/−86 | | dBc |
| Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite | | +46/−96 | | dBm/dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite | | +46/−96 | | dBm/dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite | | +46/−96 | | dBm/dBc |
| Second-Order Intermodulation Distortion (IMD2) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −85 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −74 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −70 | | dBc |
| Noise Spectral Density, RTI (NSD) | $A_V$ = 6 dB | | 2.43 | | nV/√Hz |
| | $A_V$ = 12 dB | | 1.63 | | nV/√Hz |
| | $A_V$ = 15.5 dB | | 1.51 | | nV/√Hz |
| Noise Figure (NF) | $A_V$ = 6 dB | | 10.88 | | dB |
| | $A_V$ = 12 dB | | 9.2 | | dB |
| | $A_V$ = 15.5 dB | | 8.54 | | dB |
| 500 MHz | | | | | |
| Second/Third Harmonic Distortion (HD2/HD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −69/−66 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −56/−65 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p | | −58/−66 | | dBc |
| Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite | | +35/−74 | | dBm/dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite | | +35/−74 | | dBm/dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite | | +37/−78 | | dBm/dBc |
| Second-Order Intermodulation Distortion (IMD2) | $A_V$ = 6 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −73 | | dBc |
| | $A_V$ = 12 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −75 | | dBc |
| | $A_V$ = 15.5 dB, $R_L$ = 200 Ω, $V_{OUT}$ = 2 V p-p composite (2 MHz spacing) | | −72 | | dBc |
| Noise Spectral Density, RTI (NSD) | $A_V$ = 6 dB | | 2.64 | | nV/√Hz |
| | $A_V$ = 12 dB | | 1.6 | | nV/√Hz |
| | $A_V$ = 15.5 dB | | 1.48 | | nV/√Hz |
| Noise Figure (NF) | $A_V$ = 6 dB | | 11.56 | | dB |
| | $A_V$ = 12 dB | | 9.06 | | dB |
| | $A_V$ = 15.5 dB | | 8.17 | | dB |

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| Output Voltage Swing × Bandwidth Product | 2000 V p-p MHz |
| Supply Voltage, $V_{CC}$ | 5.25 V |
| VIPx, VINx | $V_{CC}$ + 0.5 V |
| $\pm I_{OUT}$ Maximum | 30 mA |
| Internal Power Dissipation | 525 mW |
| Maximum Junction Temperature | 125°C |
| Operating Temperature Range | −40°C to +100°C |
| Storage Temperature Range | −65°C to +150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Table 4 lists the junction-to-air thermal resistance ($\theta_{JA}$) and the junction-to-paddle thermal resistance ($\theta_{JC}$) for the ADL5565.

**Table 4. Thermal Resistance**

| Package Type | $\theta_{JA}$[1] | $\theta_{JC}$[2] | Unit |
|---|---|---|---|
| 16-Lead LFCSP | 60 | 12 | °C/W |

[1] Measured on Analog Devices evaluation board. For more information about board layout, see the Soldering Information and Recommended PCB Land Pattern section.
[2] Based on simulation with JEDEC standard JESD51.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

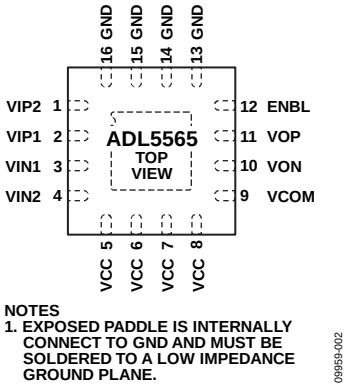


*Figure 2. Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | VIP2 | Balanced Differential Input. Biased to VCOM, typically ac-coupled. Input for $A_V$ = 12 dB gain, strapped to VIP1 for $A_V$ = 15.5 dB. |
| 2 | VIP1 | Balanced Differential Input. Biased to VCOM, typically ac-coupled. Input for $A_V$ = 6 dB gain, strapped to VIP2 for $A_V$ = 15.5 dB. |
| 3 | VIN1 | Balanced Differential Input. Biased to VCOM, typically ac-coupled. Input for $A_V$ = 6 dB gain, strapped to VIN2 for $A_V$ = 15.5 dB. |
| 4 | VIN2 | Balanced Differential Input. Biased to VCOM, typically ac-coupled. Input for $A_V$ = 12 dB gain, strapped to VIN1 for $A_V$ = 15.5 dB. |
| 5, 6, 7, 8 | VCC | Positive Supply. |
| 9 | VCOM | Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the input and output. Typically decoupled to ground with a 0.1 µF capacitor. With no reference applied, input and output common mode floats to midsupply (VCC/2). |
| 10 | VON | Balanced Differential Output. Biased to VCOM, typically ac-coupled. |
| 11 | VOP | Balanced Differential Output. Biased to VCOM, typically ac-coupled. |
| 12 | ENBL | Enable. Apply positive voltage (1.5 V ≤ ENBL < VCC) to activate device. |
| 13, 14, 15, 16, Exposed Paddle | GND | Ground. Exposed paddle is internally connected to GND and must be soldered to a low impedance ground plane. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_S$ = 3.3 V, $V_{CM}$ = 1.65 V, $R_L$ = 200 Ω differential, $A_V$ = 6 dB, $C_L$ = 1 pF differential, f = 100 MHz, $T_A$ = 25°C; parameters specified ac-coupled differential input and differential output, unless otherwise noted.

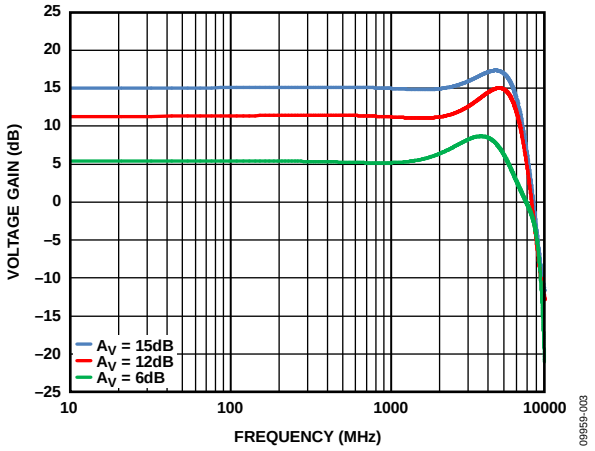


Figure 3. Gain vs. Frequency Response for 200 Ω Differential Load, $A_V$ = 6 dB, $A_V$ = 12 dB, and $A_V$ = 15.5 dB, VPOS = 3.3 V and VPOS = 5 V, 25°C

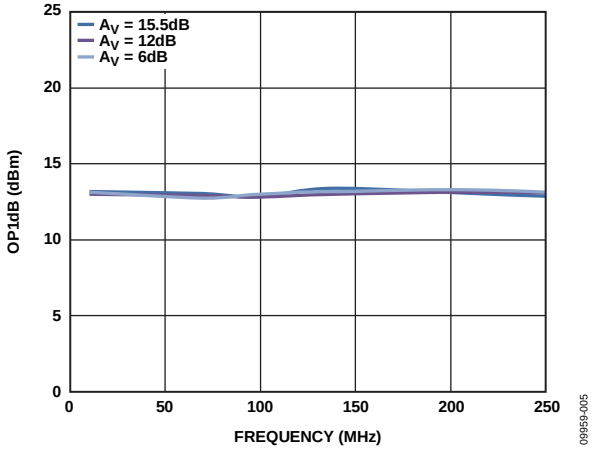


Figure 6. OP1dB vs. Frequency at Three Gains, 25°C, 200 Ω Differential Load, VPOS = 3.3 V

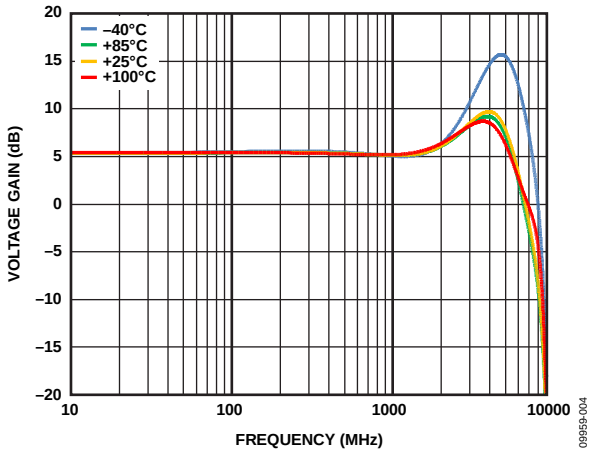


Figure 4. Gain vs. Frequency Response for 200 Ω Differential Load, $A_V$ = 6 dB, Four Temperatures, VPOS = 3.3 V, 25°C

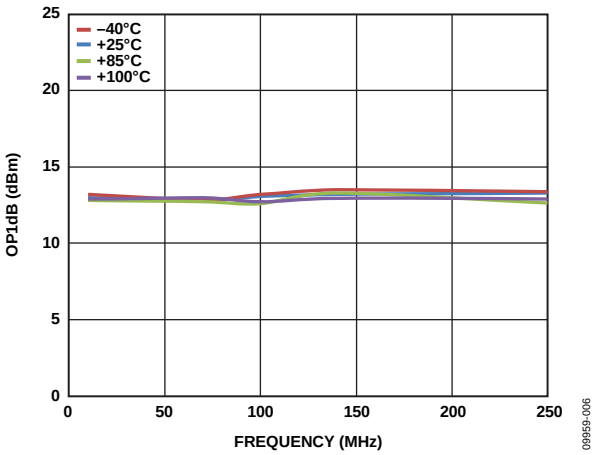


Figure 7. OP1dB vs. Frequency for 200 Ω Differential Load, $A_V$ = 6 dB, Four Temperatures, VPOS = 3.3 V

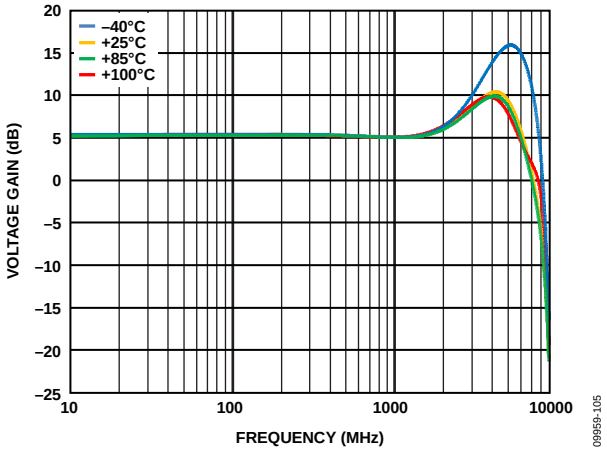


Figure 5. Gain vs. Frequency Response for 200 Ω Differential Load, $A_V$ = 6 dB, Four Temperatures, VPOS = 5 V, 25°C

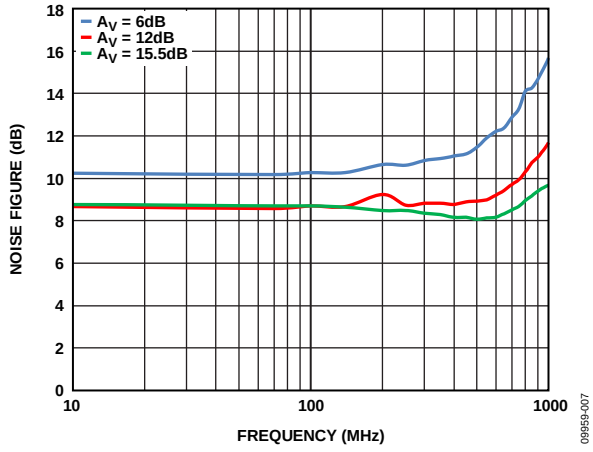


Figure 8. Noise Figure vs. Frequency at $A_V$ = 6 dB, $A_V$ = 12 dB, and $A_V$ = 15.5 dB, VPOS = 3.3 V

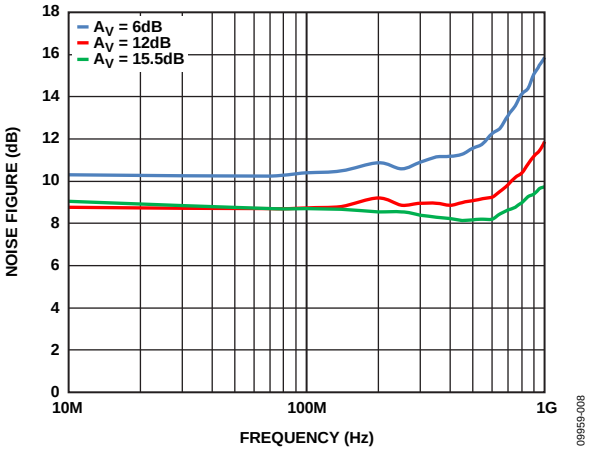


Figure 9. Noise Figure vs. Frequency at $A_V$ = 6 dB, $A_V$ = 12 dB, and $A_V$ = 15.5 dB, VPOS = 5 V

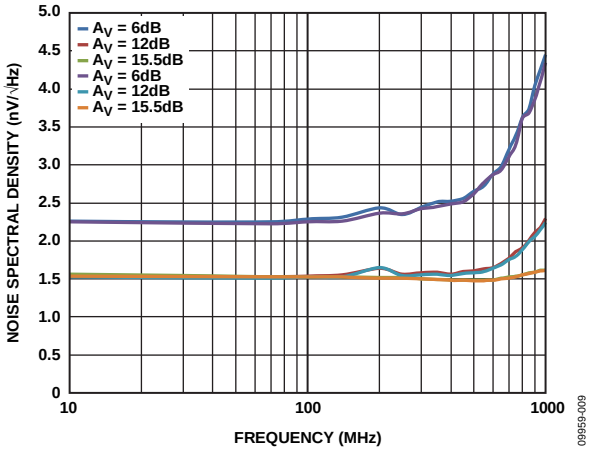


Figure 10. Noise Spectral Density vs. Frequency at $A_V$ = 6 dB, $A_V$ = 12 dB, and $A_V$ = 15.5 dB, VPOS = 3.3 V and VPOS = 5 V

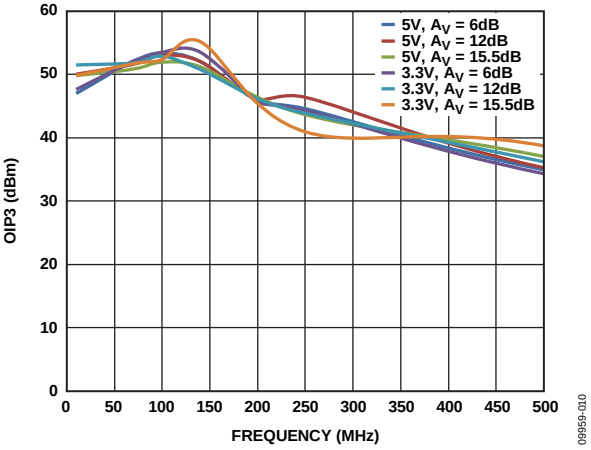


Figure 11. Output Third-Order Intercept (OIP3) at Three Gains, Output Level at 2 V p-p Composite, $R_L$ = 200 Ω, VPOS = 3.3 V and VPOS = 5 V

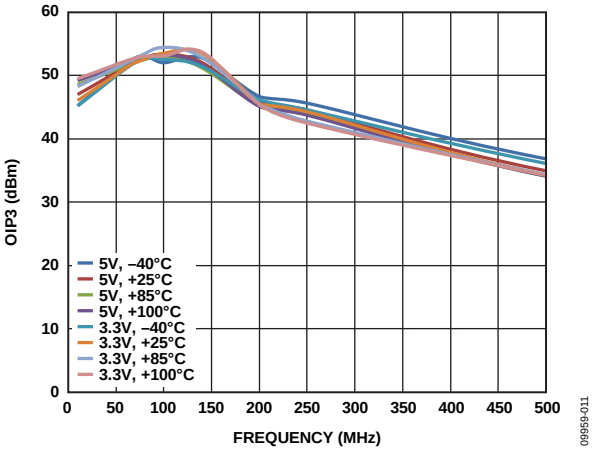


Figure 12. Output Third-Order Intercept (OIP3) vs. Frequency, Over Temperature, Output Level at 2 V p-p Composite, $R_L$ = 200 Ω, $A_V$ = 6 dB, VPOS = 3.3 V and VPOS = 5 V, Four Temperatures

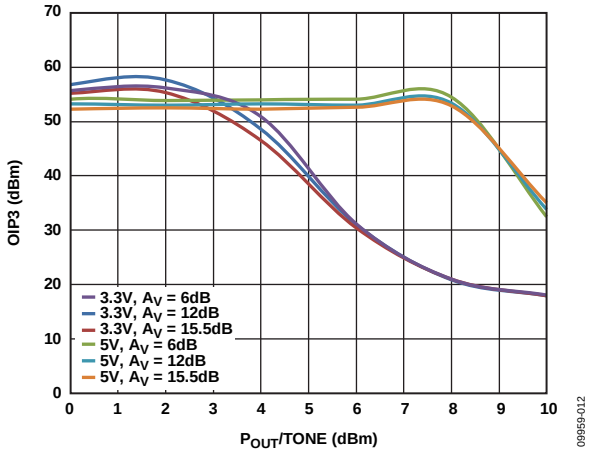


Figure 13. Output Third-Order Intercept (OIP3) vs. Power ($P_{OUT}$), Frequency 100 MHz, $A_V$ = 15.5 dB, VPOS = 3.3 V and VPOS = 5 V

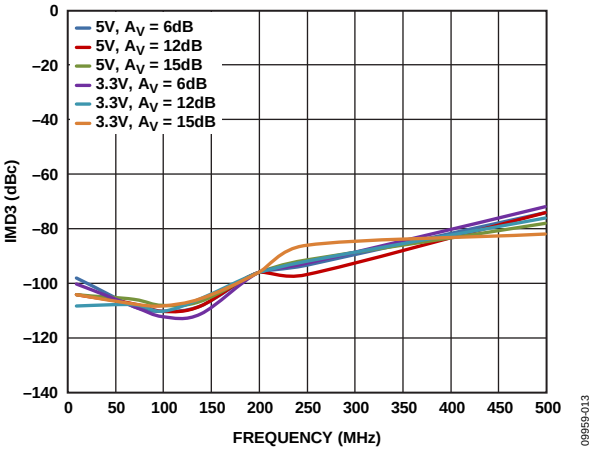


Figure 14. Output IMD3 vs. Frequency, Output Level at 2 V p-p Composite, $R_L$ = 200 Ω, VPOS = 3.3 V and VPOS = 5 V

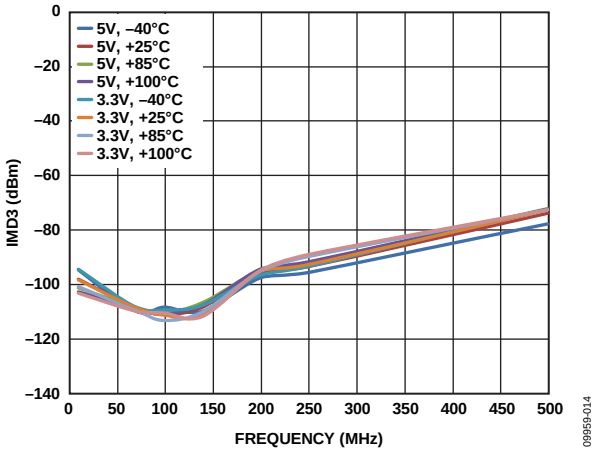


Figure 15. IMD3 vs. Frequency, Over Temperature, Output Level at 2 V p-p Composite, $R_L$ = 200 Ω, $A_V$ = 6 dB, VPOS = 3.3 V and VPOS = 5 V, Four Temperatures

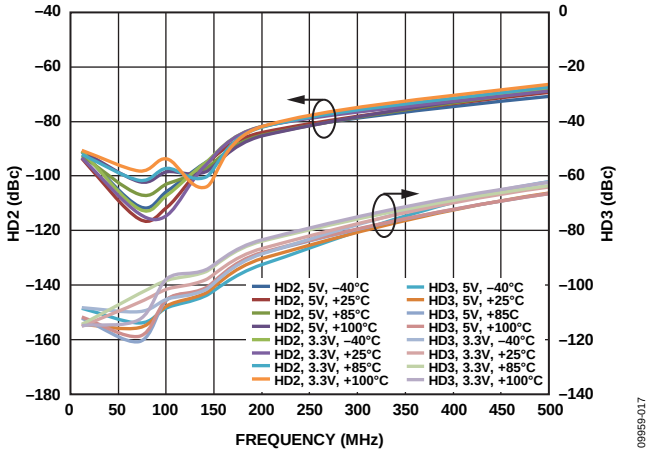


Figure 18. Harmonic Distortion (HD2/HD3) vs. Frequency, Over Temperature, Output Level at 2 V p-p Composite, $R_L$ = 200 Ω, $A_V$ = 6 dB, VPOS = 3.3 V and VPOS = 5 V, Four Temperatures

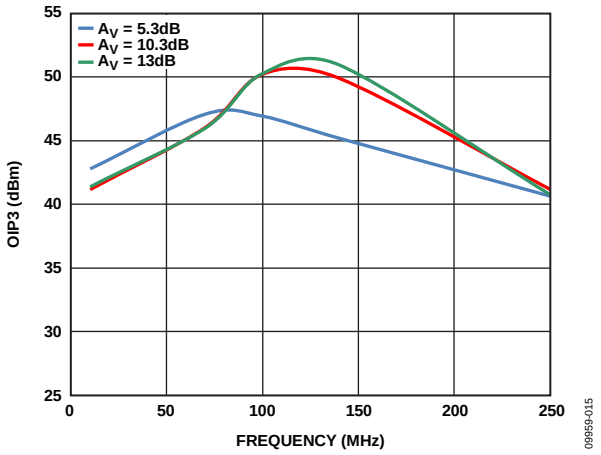


Figure 16. Single-Ended OIP3 vs. Frequency

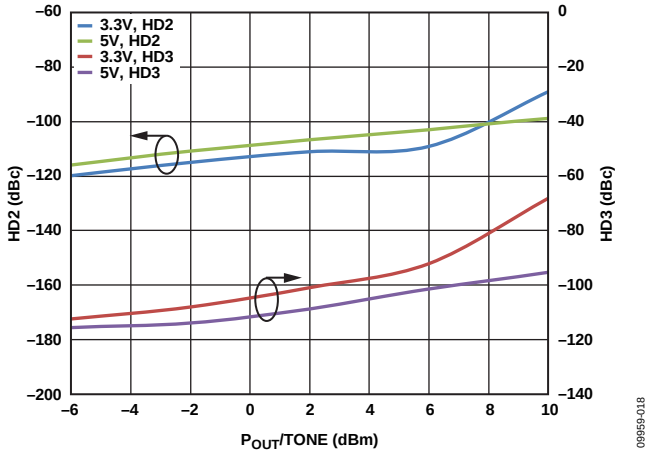


Figure 19. Harmonic Distortion vs. Output Power per Tone, Frequency = 100 MHz, $R_L$ = 200 Ω, VPOS = 3.3 V and VPOS = 5 V

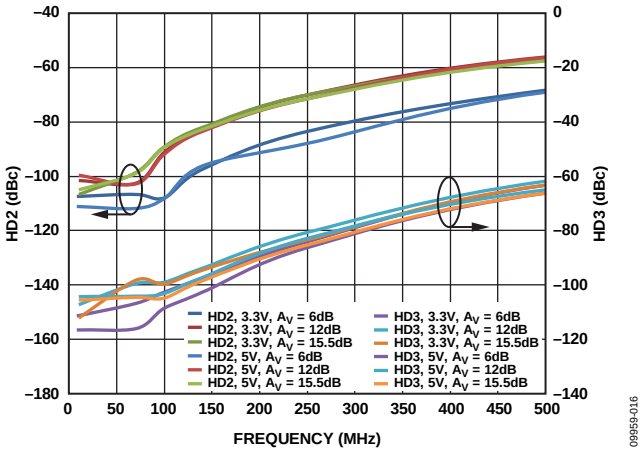


Figure 17. Harmonic Distortion (HD2/HD3) vs. Frequency, Output Level at 2 V p-p Composite, $R_L$ = 200 Ω, VPOS = 3.3 V and VPOS = 5 V

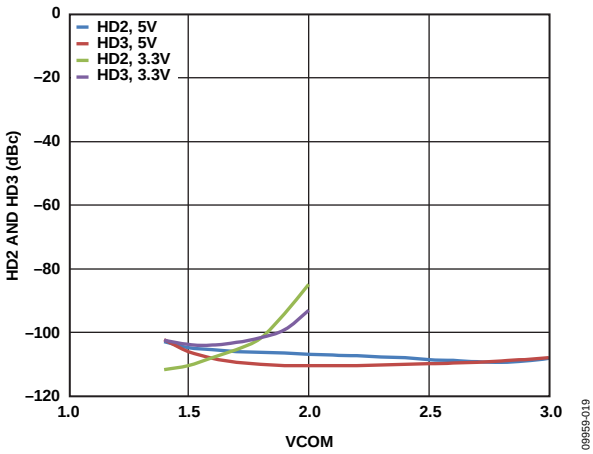


Figure 20. Harmonic Distortion (HD2/HD3) vs. VCOM, $A_V$ = 6 dB, VPOS = 3.3 V and VPOS = 5 V

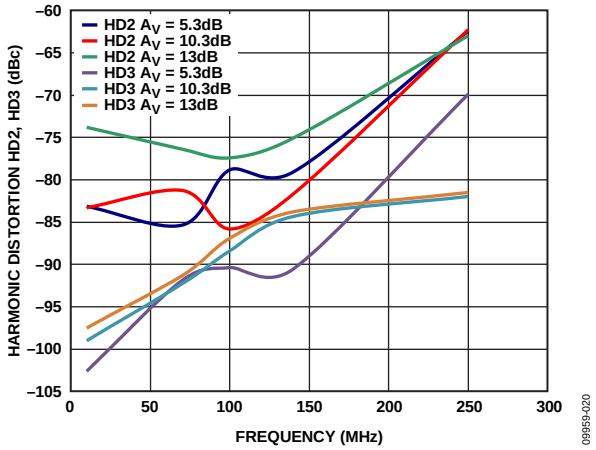


Figure 21. Single-Ended Harmonic Distortion (HD2/HD3) vs. Frequency

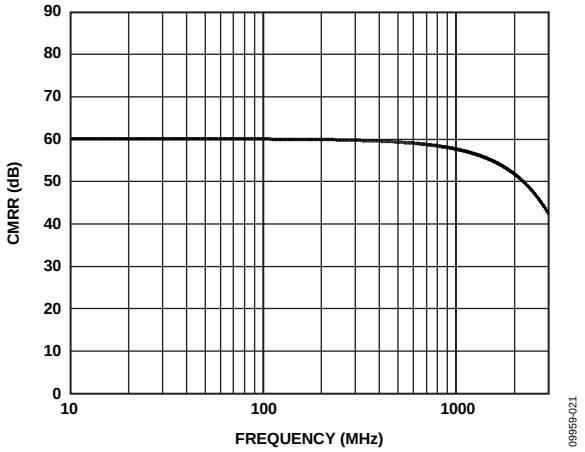


Figure 24. Common-Mode Rejection Ratio (CMRR) vs. Frequency

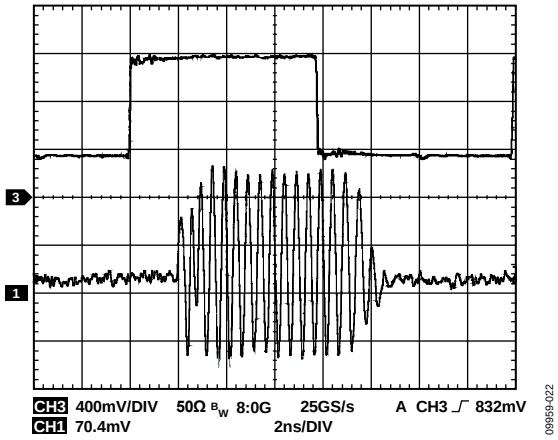


Figure 22. ENBL Time Domain Response

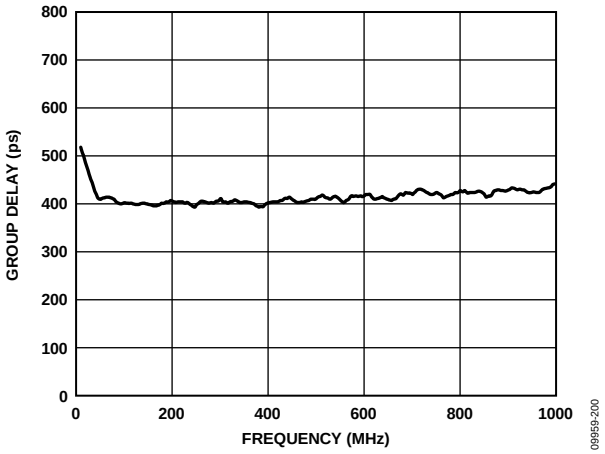


Figure 25. Group Delay vs. Frequency

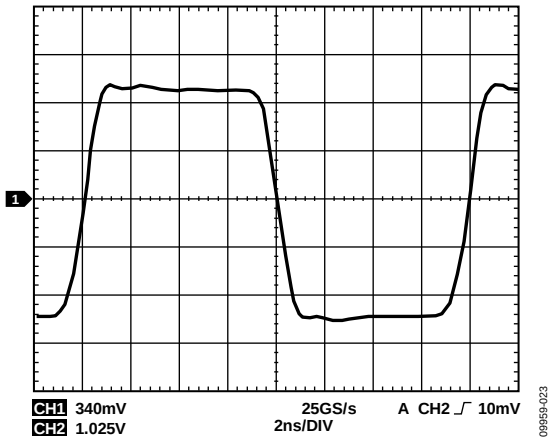


Figure 23. Large Signal Pulse Response, $A_V$ = 15.5 dB

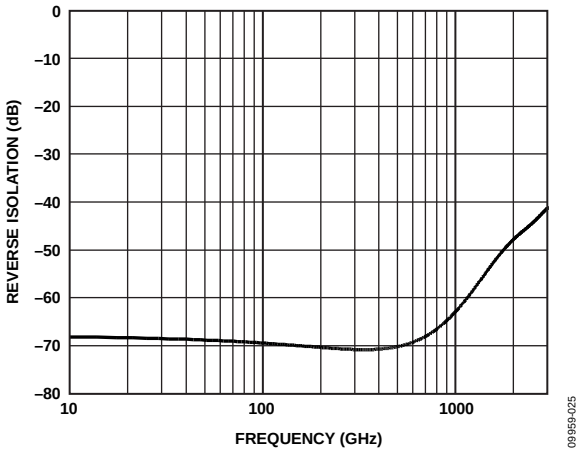


Figure 26. Reverse Isolation (S12) vs. Frequency $A_V$ = 6 dB

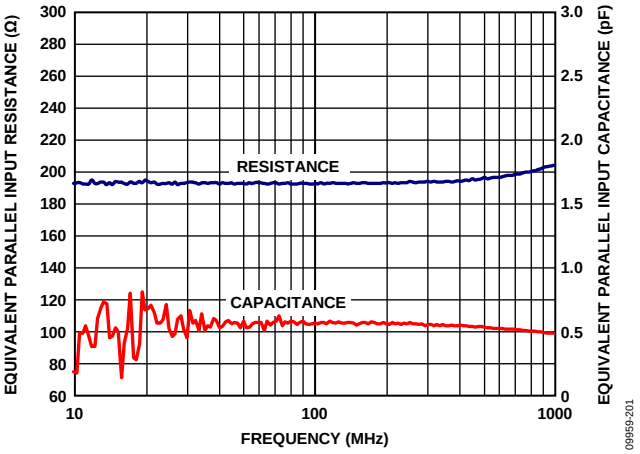


Figure 27. S11 Equivalent RLC Parallel Network, $A_V$ = 6 dB

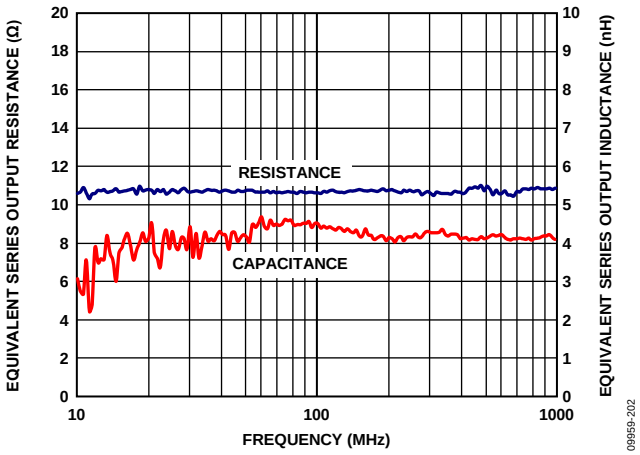


Figure 28. S22 Equivalent RLC Parallel Network, $A_V$ = 6 dB

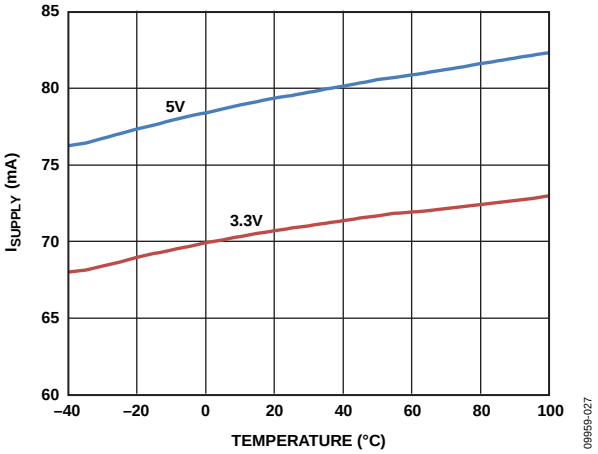


Figure 29. $I_{SUPPLY}$ vs. Temperature, $R_L$ = 200 Ω, $A_V$ = 6 dB, VPOS = 3.3 V and VPOS = 5 V

# CIRCUIT DESCRIPTION

## BASIC STRUCTURE

The ADL5565 is a low noise, fully differential amplifier/ADC driver that can operate from 2.8 V to 5.2 V. It provides three gain options, 6 dB, 12 dB, and 15.5 dB, without the need for external resistors and has wide bandwidths of greater than 6 GHz for all gains. Differential input impedance is 200 Ω for 6 dB, 100 Ω for 12 dB, and 67 Ω for 15.5 dB. It has a differential output impedance of 10 Ω.

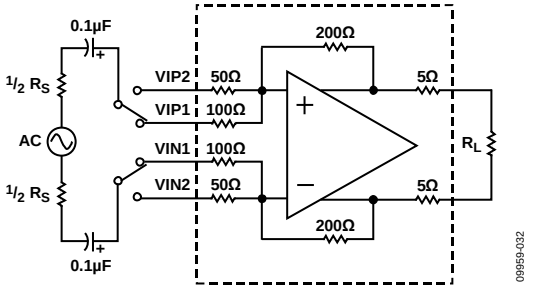


*Figure 30. Basic Structure*

The ADL5565 is composed of a fully differential amplifier with on-chip feedback and feed forward resistors. The two feedforward resistors on each input set this pin-strappable amplifier in three different gain configurations of 6 dB, 12 dB, and 15.5 dB, and by using two external resistors, any gain from 0 dB to 15.5 dB can be realized. The amplifier is designed to provide high differential open-loop gain and an output common-mode circuit that enables the user to change the common-mode voltage from the VCOM pin. The amplifier is designed to provide superior low distortion at frequencies up to and beyond 300 MHz with low noise and low power consumption from a 3.3 V power supply at 70 mA.

The ADL5565 is very flexible in terms of I/O coupling. It can be ac-coupled or dc-coupled at the inputs and/or the outputs within the specified input and output common-mode levels. The input of the device can be configured as single-ended or differential with similar third-order distortion performance. Due to the internal connections between the inputs and outputs, an output common-mode voltage between 1.4 V and 1.8 V at 3.3 V and 1.4 V to 3 V at 5 V must be maintained for the best distortion. For a dc-coupled input, the input common mode should be between 1.2 V and 2 V at the 3.3 V supply, and 1.2 V to 3.8 V at the 5 V supply. The device has been characterized using 2 V p-p into a 200 Ω ac-coupled output. If the inputs are ac-coupled, the input and output common-mode voltages are set by VCC/2 when no external circuitry is used. The ADL5565 provides an output common-mode voltage set by VCOM, which allows driving an ADC directly without external components. Although distortion is similar over the specified frequency range at both 3.3 V and 5 V, lower distortion results on the 5 V supply for signal swings larger than 2 V p-p.

# APPLICATIONS INFORMATION

## BASIC CONNECTIONS

Figure 31 shows the basic connections for operating the ADL5565. Apply a voltage between 3 V and 5 V to the VCC pins, and decouple each supply pin with at least one low inductance, 0.1 µF surface-mount ceramic capacitor, placed as close as possible to the device. Also, decouple the VCOM pin (Pin 9) using a 0.1 µF capacitor.

The gain of the part is determined by the pin-strappable input configuration. When Input A is applied to VIP1 and Input B is applied to VIN1, the gain is 6 dB (minimum gain, see Equation 1 and Equation 2). When Input A is applied to VIP2 and Input B is applied to VIN2, the gain is 12 dB (middle gain). When Input A is applied to both VIP1 and VIP2 and Input B is applied to both VIN1 and VIN2, the gain is 15.5 dB (maximum gain).

Pin 1 to Pin 4, Pin 10, and Pin 11 are biased at 1/2 VCC above ground and can be dc-coupled (if within the specified input or output common-mode voltage levels) or ac-coupled as shown in Figure 31.

To enable the ADL5565, the ENBL pin must be pulled high. Pulling the ENBL pin low puts the ADL5565 in sleep mode, reducing the current consumption to 5 mA at ambient.

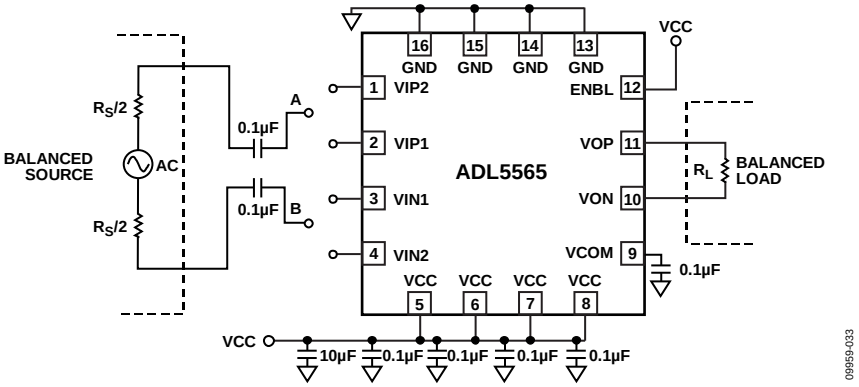


*Figure 31. Basic Connections*

## INPUT AND OUTPUT INTERFACING

The ADL5565 can be configured as a differential input to differential output driver, as shown in Figure 32. The resistors, R1 and R2, combined with the ETC1-1-13 balun transformer, provide a 50 Ω input match for the three input impedances that change with the variable gain strapping. The input and output 0.1 µF capacitors isolate the VCC/2 bias from the source and balanced load. The load should equal 200 Ω to provide the expected ac performance (see the Specifications section and the Typical Performance Characteristics section).

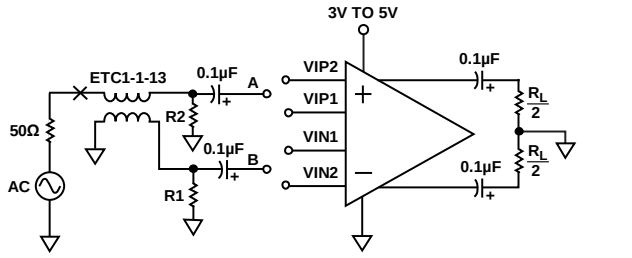


*Figure 32. Differential Input to Differential Output Configuration*

**Table 6. Differential Termination Values for Figure 32**

| Gain (dB) | R1 (Ω) | R2 (Ω) |
|---|---|---|
| 6 | 29 | 29 |
| 12 | 33 | 33 |
| 15.5 | 40.2 | 40.2 |

The differential gain of the ADL5565 is dependent on the source impedance and load, as shown in Figure 33.

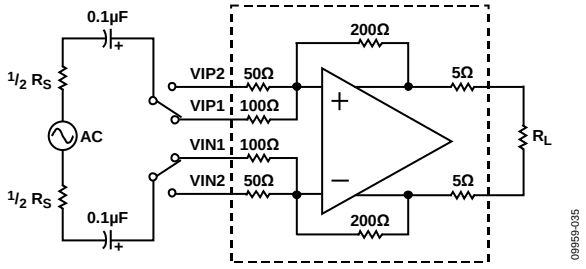


*Figure 33. Differential Input Loading Circuit*

The differential gain can be determined using the following formula. The values of $R_G$ for each gain configuration are shown in Table 7.

$$A_V = \frac{200}{R_G} \times \frac{R_L}{10 + R_L} \quad (1)$$

In Equation 1, $R_G$ is the gain setting resistor (see Figure 1).

**Table 7. Values of $R_G$ for Differential Gain**

| Gain (dB) | $R_G$ (Ω) |
|---|---|
| 6 | 100 |
| 12 | 50 |
| 15.5 | 33.5 |

### *Single-Ended Input to Differential Output*

The ADL5565 can also be configured in a single-ended input to differential output driver, as shown in Figure 34. In this configuration, the gain of the part is reduced due to the application of the signal to only one side of the amplifier. The strappable gain values are listed in Table 8 with the required terminations to match to a 50 Ω source using R1 and R2. The input and output 0.1 µF capacitors isolate the VCC/2 bias from the source and the balanced load. The performance for this configuration is shown in Figure 16 and Figure 21.

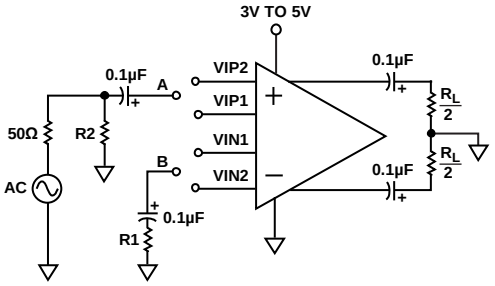


*Figure 34. Single-Ended Input to Differential Output Configuration*

**Table 8. Single-Ended Termination Values for Figure 34**

| Gain (dB) | R1 (Ω) | R2 (Ω) |
|---|---|---|
| 5.3 | 30 | 73 |
| 10.3 | 30 | 104 |
| 13 | 30 | 154 |

The single-ended gain configuration of the ADL5565 is dependent on the source impedance and load, as shown in Figure 35.

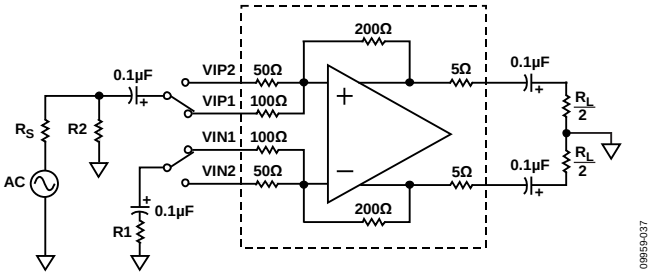


*Figure 35. Single-Ended Input Loading Circuit*

The single-ended gain can be determined using the following formula. The values of $R_G$ and $R_X$ for each gain configuration are shown in Table 9.

$$A_{V1} = \frac{200}{R_G + \left(\frac{R_S \times R2}{R_S + R2}\right)} \times \frac{R2}{R_S + R2} \times \frac{R_X + R_S}{R_X} \times \frac{R_L}{10 + R_L} \quad (2)$$

In Equation 2, $R_G$ is the gain setting resistor (see Figure 1).

**Table 9. Values of RG and RX for Single-Ended Gain**

| Gain (dB) | $R_G$ (Ω)[1] | $R_X$ (Ω) |
|---|---|---|
| 5.3 | 100 | R2 \|\| 158[2] |
| 10.3 | 50 | R2 \|\| 96[2] |
| 13 | 33.5 | R2 \|\| 74[2] |

[1] $R_G$ is the gain setting resistor (see Figure 1).
[2] These values are based on a 50 Ω input match.

## GAIN ADJUSTMENT AND INTERFACING

The effective gain of the ADL5565 can be reduced using a number of techniques. A matched attenuator network can reduce the effective gain; however, this requires the addition of a separate component that can be prohibitive in size and cost. Instead, a simple voltage divider can be implemented using the combination of additional series resistors at the amplifier input and the input impedance of the ADL5565, as shown in Figure 36. A pair of resistors is used to match to the impedance of the previous stage.

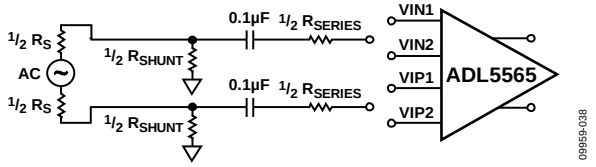


*Figure 36. Gain Adjustment Using a Series Resistor*

Figure 36 shows a typical implementation of the divider concept that effectively reduces the gain by adding attenuation at the input. For frequencies less than 100 MHz, the input impedance of the ADL5565 can be modeled as a real 66 Ω, 100 Ω, or 200 Ω resistance (differential) for maximum, middle, and minimum gains, respectively. Assuming that the frequency is low enough to ignore the shunt reactance of the input and high enough so that the reactance of moderately sized ac coupling capacitors can be considered negligible, the insertion loss, Il, due to the shunt divider can be expressed as

$$Il(dB) = 20\log\left(\frac{R_G}{R_{SERIES} + R_G}\right) \quad (3)$$

In Equation 3, $R_G$ is the gain setting resistor (see Figure 1).

*Adjusted Gain* (dB) =
6 dB, 12 dB, or 15.5 dB Gain – *Il* (dB) (4)

The necessary shunt component, $R_{SHUNT}$, to match to the source impedance, $R_S$, can be expressed as

$$R_{SHUNT} = \frac{1}{\frac{1}{R_S} - \frac{1}{R_{SERIES} + R_G}} \quad (5)$$

In Equation 5, $R_G$ is the gain setting resistor (see Figure 1).

The insertion loss and the resultant power gain for multiple shunt resistor values are summarized in Table 10. The source resistance and input impedance need careful attention when using Equation 3, Equation 4, and Equation 5. The reactance of the input impedance of the ADL5565 and the ac coupling capacitors must be considered before assuming that they make a negligible contribution.

**Table 10. Differential Gain Adjustment Using Series Resistor**

| Gain (dB) | Differential $R_G$ (Ω)[4] | $R_S$ (Ω) | Differential $R_{SERIES}$ (Ω) | Differential $R_{SHUNT}$ (Ω)[5] |
|---|---|---|---|---|
| 0[1] | 200 | 50 | 200 | 57.6 |
| 1[1] | 200 | 50 | 154 | 57.6 |
| 2[1] | 200 | 50 | 118 | 59 |
| 3[1] | 200 | 50 | 84.5 | 60.4 |
| 4[1] | 200 | 50 | 52.3 | 61.9 |
| 5[1] | 200 | 50 | 24.9 | 64.9 |
| 6[1] | 200 | 50 | 0 | 66.5 |
| 7[2] | 100 | 50 | 78.7 | 69.8 |
| 8[2] | 100 | 50 | 59 | 73.2 |
| 9[2] | 100 | 50 | 42.2 | 76.8 |
| 10[2] | 100 | 50 | 26.7 | 82.5 |
| 11[2] | 100 | 50 | 12.7 | 88.7 |
| 12[2] | 100 | 50 | 0 | 100 |
| 13[3] | 66.7 | 50 | 23.7 | 113 |
| 14[3] | 66.7 | 50 | 13.7 | 133 |
| 15.5[3] | 66.7 | 50 | 0 | 200 |

[1] Amplifier is configured for 6 dB gain setting.
[2] Amplifier is configured for 12 dB gain setting.
[3] Amplifier is configured for 15.5 dB gain setting.
[4] $R_G$ is the gain setting resistor (see Figure 1).
[5] The resistor values are rounded to the nearest real resistor value.

## ADC INTERFACING

The ADL5565 is a high output linearity amplifier that is optimized for ADC interfacing. There are several options available to the designer when using the ADL5565. Figure 40 uses a wideband 1:1 transmission line balun followed by two 40 Ω resistors in parallel with the three input impedances (which change with the gain selection of the ADL5565) to provide a 50 Ω differential impedance and provides a wideband match to a 50 Ω source. The ADL5565 is ac-coupled from the AD9467 to avoid common-mode dc loading. The 33 Ω resistors improve the isolation between the ADL5565 and any switching currents present at the analog-to-digital, sample-and-hold circuitry. The AD9467 input presents a 530 Ω differential load impedance and requires a 2 V to 2.5 V differential input swing to reach full scale (VREF = 1 V to 1.25 V). This circuit provides variable gain, isolation, and source matching for the AD9467.

Applying a full-scale, single-tone signal from the ADL5565, an SFDR of 91.9 dBc is realized (see Figure 37). Applying two half-scale signals from the ADL5565 in a gain of 6 dB, an SFDR of 86.4 dBc is achieved at 100 MHz (see Figure 38). The bandwidth of the circuit in Figure 40 is shown in Figure 39.

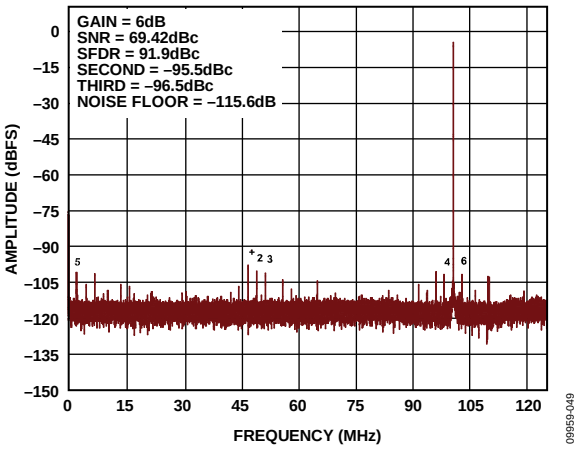


*Figure 37. Measured Single-Tone Performance of the Circuit in Figure 40 for a 100 MHz Input Signal*

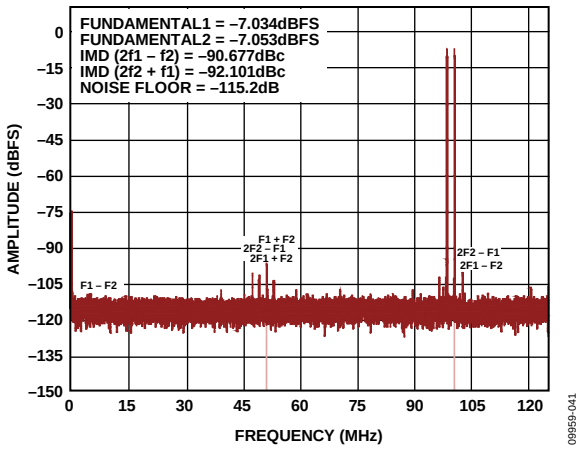


*Figure 38. Measured Two-Tone Performance of the Circuit in Figure 40 for a 100 MHz and 102 MHz Input Signals*

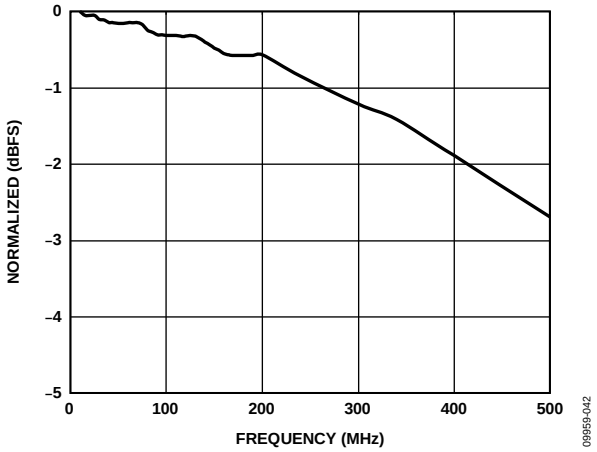


*Figure 39. Measured Frequency Response of the Wideband ADC Interface Depicted in Figure 40*

The wideband frequency response is an advantage in broadband applications, such as predistortion receiver designs and instrumentation applications. However, by designing for a wide analog input frequency range, the cascaded SNR performance is somewhat degraded due to high frequency noise aliasing into the wanted Nyquist zone.

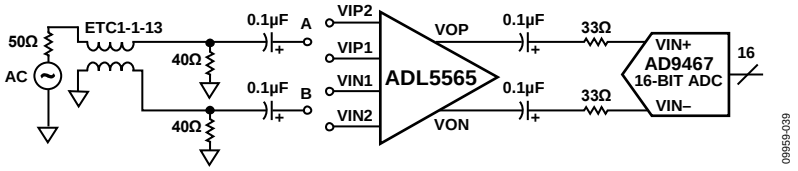


*Figure 40. Wideband ADC Interfacing Example Featuring the AD9467*

By designing a narrow band-pass antialiasing filter between the ADL5565 and the target ADC, the output noise of the ADL5565 outside of the intended Nyquist zone can be attenuated, helping to preserve the available SNR of the ADC. In general, the SNR improves several decibels when including a reasonable order anti-aliasing filter. In this example, a low loss 1:1 input transformer is used to match the ADL5565 balanced input to a 50 Ω unbalanced source, resulting in minimum insertion loss at the input.

Figure 41 is optimized for driving some of Analog Devices popular ADCs, such as the AD9467. Table 11 includes antialiasing filter component recommendations for popular IF sampling frequencies. Inductor L5 works in parallel with the on-chip ADC input capacitance and a portion of the capacitance presented by C4 to form a resonant tank circuit. The resonant tank helps to ensure that the ADC input looks like a real resistance at the target center frequency. The inductor, L5, shorts the ADC inputs at dc, which introduces a zero into the transfer function. In addition, the ac coupling capacitors introduce additional zeros into the transfer function. The final overall frequency response takes on a band-pass characteristic, helping to reject noise outside of the intended Nyquist zone. Table 11 provides initial suggestions for prototyping purposes. Some empirical optimization may be needed to help compensate for actual PCB parasitics.

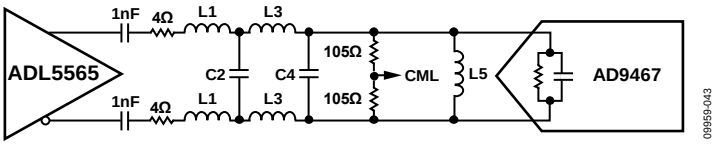


*Figure 41. Narrow-Band IF Sampling Solution for an ADC Application*

**Table 11. Interface Filter Recommendations for Various IF Sampling Frequencies**

| Center Frequency (MHz) | 1 dB Bandwidth (MHz) | L1 (nH) | C2 (pF) | L3 (nH) | C4 (pF) | L5 (nH) |
|---|---|---|---|---|---|---|
| 96 | 30 | 3.3 | 47 | 27 | 75 | 82 |
| 140 | 40 | 3.3 | 47 | 27 | 27 | 150 |
| 170 | 32 | 3.3 | 56 | 27 | 18 | 120 |
| 211 | 33 | 3.3 | 47 | 27 | 15 | 51 |

## LAYOUT CONSIDERATIONS

High-Q inductive drives and loads, as well as stray transmission line capacitance in combination with package parasitics, can potentially form a resonant circuit at high frequencies, resulting in excessive gain peaking or possible oscillation. If RF transmission lines connecting the input or output are used, design them such that stray capacitance at the input/output pins is minimized. In many board designs, the signal trace widths should be minimal where the driver/receiver is no more than one-eighth of the wavelength from the amplifier. This nontransmission line configuration requires that underlying and adjacent ground and low impedance planes be dropped from the signal lines.

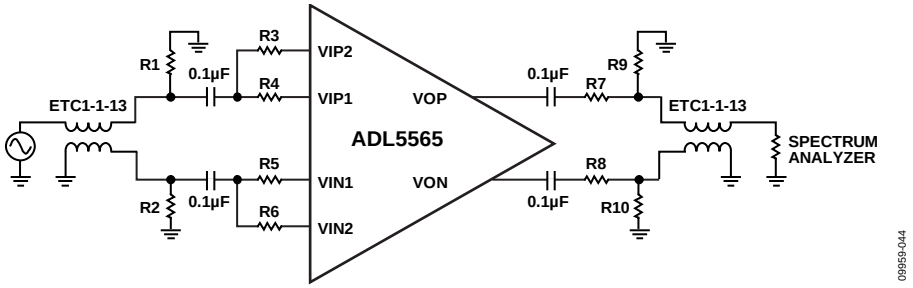


*Figure 42. General-Purpose Characterization Circuit*

**Table 12. Gain Setting and Input Termination Components for Figure 42**

| $A_V$ (dB) | R1 (Ω) | R2 (Ω) | R3 (Ω) | R4 (Ω) | R5 (Ω) | R6 (Ω) |
|---|---|---|---|---|---|---|
| 6 | 29 | 29 | Open | 0 | 0 | Open |
| 12 | 33 | 33 | 0 | Open | Open | 0 |
| 15.5 | 40.2 | 40.2 | 0 | 0 | 0 | 0 |

**Table 13. Output Matching Network for Figure 42**

| $R_L$ (Ω) | R7 (Ω) | R8 (Ω) | R9 (Ω) | R10 (Ω) |
|---|---|---|---|---|
| 200 | 84.5 | 84.5 | 34.8 | 34.8 |

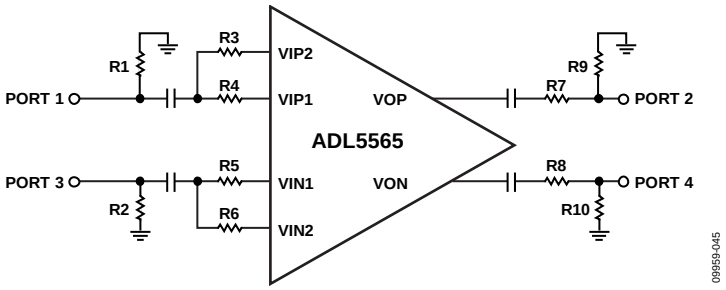


*Figure 43. Differential Characterization Circuit Using Agilent E8357A Four-Port PNA*

**Table 14. Gain Setting and Input Termination Components for Figure 43**

| $A_V$ (dB) | R1 (Ω) | R2 (Ω) | R3 (Ω) | R4 (Ω) | R5 (Ω) | R6 (Ω) |
|---|---|---|---|---|---|---|
| 6 | 100 | 100 | Open | 0 | 0 | Open |
| 12 | Open | Open | 0 | Open | Open | 0 |
| 15.5 | Open | Open | 0 | 0 | 0 | 0 |

**Table 15. Output Matching Network for Figure 43**

| $R_L$ (Ω) | R7 (Ω) | R8 (Ω) | R9 (Ω) | R10 (Ω) |
|---|---|---|---|---|
| 200 | 50 | 50 | Open | Open |

## SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 44 shows the recommended land pattern for the ADL5565. The ADL5565 is contained in a 3 × 3 mm LFCSP package, which has an exposed ground paddle (EPAD). This paddle is internally connected to the ground of the chip. To minimize thermal impedance and ensure electrical performance, solder the paddle to the low impedance ground plane on the PCB. To further reduce thermal impedance, it is recommended that the ground planes on all layers under the paddle be stitched together with vias.

For more information on land pattern design and layout, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

This land pattern, on the ADL5565 evaluation board, provides a measured thermal resistance ($\theta_{JA}$) of 60°C/W. To measure $\theta_{JA}$, the temperature at the top of the LFCSP package is found with an IR temperature gun. Thermal simulation suggests a junction temperature 1.5°C higher than the top of package temperature. With additional ambient temperature and I/O power measurements, $\theta_{JA}$ could be determined.

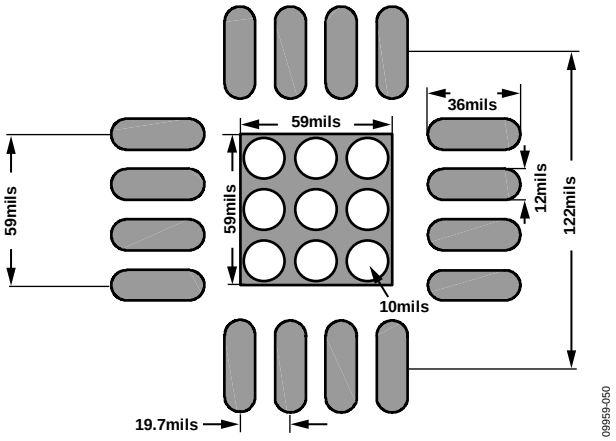


*Figure 44. Recommended Land Pattern*

## EVALUATION BOARD

Figure 45 shows the schematic of the ADL5565 evaluation board. The board is powered by a single supply in the 3 V to 5 V range. The power supply is decoupled by 10 µF and 0.1 µF capacitors.

Table 16 details the various configuration options of the evaluation board. Figure 46 and Figure 47 show the component and circuit side layouts of the evaluation board.

To realize the minimum gain (6 dB into a 200 Ω load), Input 1 (VIN1 and VIP1) must be used by installing 0 Ω resistors at R3 and R4, leaving R5 and R6 open. R1 and R2 must be 33.2 Ω for a 50 Ω input impedance.

Likewise, driving Input 2 (VIN2 and VIP2) realizes the middle gain (12 dB into a 200 Ω load) by installing 0 Ω at R5 and R6 and leaving R3 and R4 open. R1 and R2 must be 50 Ω for a 50 Ω input impedance.

For the maximum gain (15.5 dB into a 200 Ω load), both inputs are driven by installing 0 Ω resistors at R3, R4, R5, and R6. R1 and R2 are open for a 50 Ω input impedance.

The balanced input and output interfaces are converted to single ended with a pair of baluns (M/A-COM ETC1-1-13). The balun at the input, T1, provides a 50 Ω single-ended-to-differential transformation. The output balun, T2, and the matching components are configured to provide a 200 Ω to 50 Ω impedance transformation with an insertion loss of about 11 dB.

As an alternative, the input transformer, T1, can be replaced with one of the following transformers to provide a low loss balanced input to the ADL5565.

- 6 dB gain configuration, Mini-Circuits TC4-1W+
- 12 dB gain configuration, Mini-Circuits, TC2-1T+
- 15.5 dB gain configuration, Mini-Circuits TC1.5-52T

When using these alternative transformers, R1 and R2 are left open. Replace C1 and C2 with 0 Ω jumpers and add a 0.1 µF capacitor to C12.

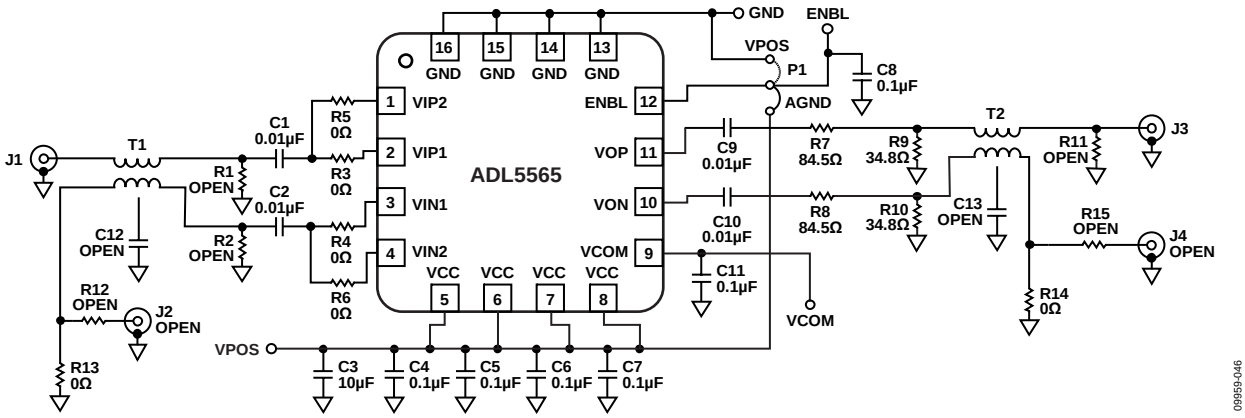


*Figure 45. Evaluation Board Schematic*

**Table 16. Evaluation Board Configuration Options**

| Component | Description | Default Condition |
|---|---|---|
| VPOS, GND | Ground and supply vector pins. | VPOS, GND = installed |
| C3, C4, C5, C6, C7, C11 | Power supply decoupling. The supply decoupling consists of a 10 µF capacitor (C3) to ground. C4 to C7 are bypass capacitors. C11 ac couples VREF to ground. | C3 = 10 µF (Size D), C4, C5, C6, C7, C11 = 0.1 µF (Size 0402) |
| J1, J2, R1, R2, R3, R4, R5, R6, R12, R13, C1, C2, C12, T1 | Input interface. The SMA labeled J1 is the input. T1 is a 1-to-1 impedance ratio balun to transform a single-ended input into a balanced differential signal. Removing R13, installing R12 (0 Ω), and installing an SMA connector (J2) allows driving from a differential source. C1 and C2 provide ac coupling. C12 is a bypass capacitor. R1 and R2 provide a differential 50 Ω input termination. R3 to R6 are used to select the input for the pin-strappable gain. The maximum gain is R3, R4, R5, R6 = 0 Ω and R1 and R2 = open. The middle gain is R5 and R6 = 0 Ω, R3 and R4 = open, and R1 and R2 = 50 Ω. The minimum gain is R3 and R4 = 0 Ω, R5 and R6 = open, and R1 and R2 = 33.2 Ω. | J1 = installed, J2 = not installed, R1, R2 = open, R3, R4, R5, R6, R13 = 0 Ω (Size 0402), R12, = open, C1, C2 = 0.01 µF (Size 0402), C12 = open, T1 = ETC1-1-13 (M/A-COM) |
| J3, J4, R7, R8, R9, R10, R11, R14, R15 C9, C10, C13, T2 | Output interface. The SMA labeled J3 is the output. T2 is a 1-to-1 impedance ratio balun to transform a balanced differential signal to a single-ended signal. Removing R14, installing R15 (0 Ω), and installing an SMA connector (J4) allows differential loading. C13 is a bypass capacitor. R7, R8, R9, and R10 are provided for generic placement of matching components. The evaluation board is configured to provide a 200 Ω to 50 Ω impedance transformation with an insertion loss of 17 dB. C9 and C10 provide ac coupling. | J3 = installed, J4 = not installed, R7, R8 = 84.5 Ω (Size 0402), R9, R10 = 34.8 Ω (Size 0402), R11, R15 = open (Size 0402), R14 = 0 Ω (Size 0402) C9, C10 = 0.01 µF (Size 0402), C13 = open T2 = ETC1-1-13 (M/A-COM) |
| ENBL, P1, C8 | Device enabled. C8 is a bypass capacitor. When the P1 jumper is set toward the VPOS label, the ENBL pin is connected to the supply, enabling the device. In the opposite direction, toward the GND label, the ENBL pin is grounded, putting the device in power-down mode. | ENBL, P1 = installed, C8 = 0.1 µF (Size 0402) |

**Table 17. Differential Values for Figure 45**

| Gain (dB) | R1 (Ω) | R2 (Ω) |
|---|---|---|
| 6 | 29 | 29 |
| 12 | 33 | 33 |
| 15.5 | Open | Open |

**Table 18. Alternative Differential Input Configuration for Figure 45**

| Gain (dB) | R1 and R2 (Ω) | C12 (µF) | C1 and C2 (Ω) | T1 |
|---|---|---|---|---|
| 6 | Open | 0.1 | 0 | Mini Circuits TC4-1W+ |
| 12 | Open | 0.1 | 0 | Mini Circuits TC2-1T+ |
| 15.5 | Open | 0.1 | 0 | Mini Circuits TC1.5-52T+ |

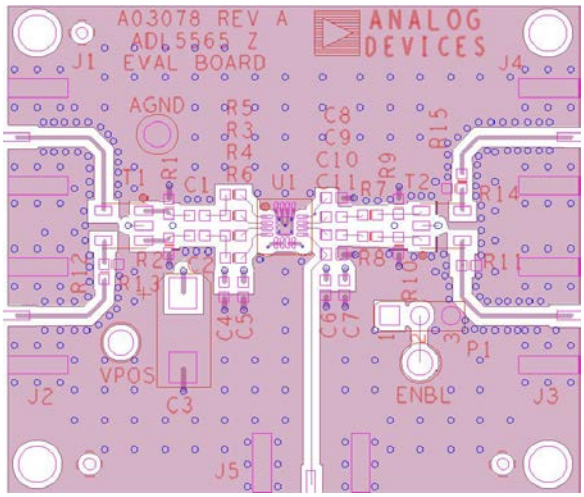


Figure 46. Layout of Evaluation Board, Component Side

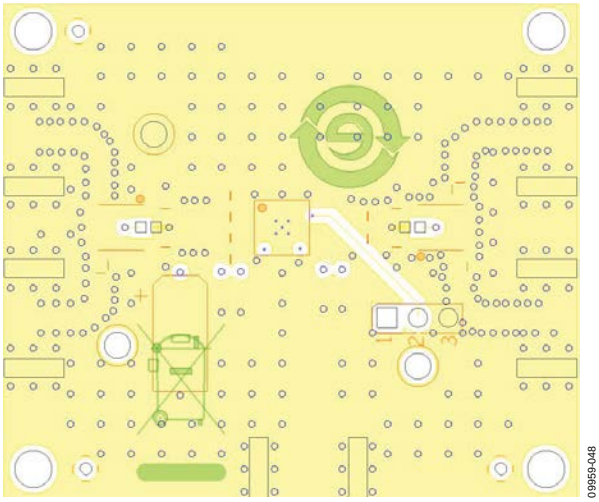


Figure 47. Layout of Evaluation Board, Circuit Side

# OUTLINE DIMENSIONS

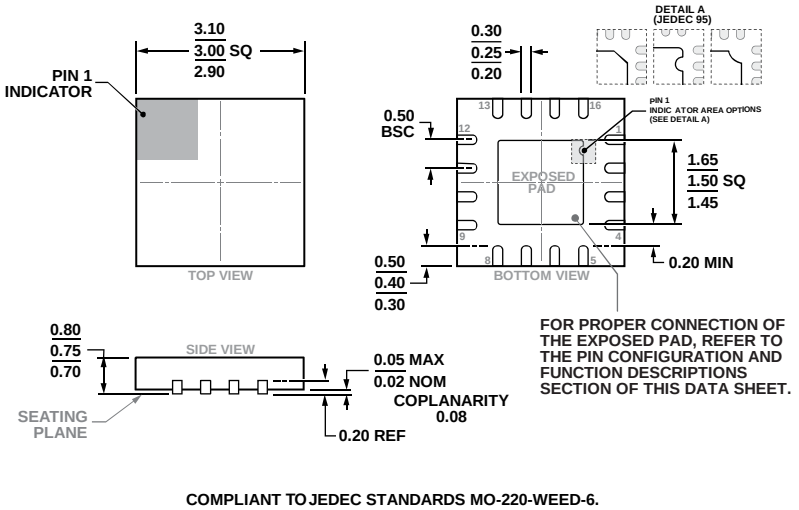


*Figure 48. 16-Lead Lead Frame Chip Scale Package [LFCSP]*
*3 mm × 3 mm Body and 0.75 mm Package Height*
*(CP-16-27)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Marking Code |
|---|---|---|---|---|
| ADL5565ACPZ-R7 | −40°C to + 85°C | 16-Lead Lead Frame Chip Scale Package [LFCSP], 7" Tape and Reel | CP-16-27 | Q1Z |
| ADL5565-EVALZ | | Evaluation Board | | |

[1] Z = RoHS Compliant Part.


D09959-0-6/18(G)