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9/2017—Rev. A to Rev. B

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10/2008—Rev. 0 to Rev. A

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7/2008—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3 V, V_{EE} = 0 V, T_A = −40°C to +125°C. All outputs terminated through 50 Ω to V_{CC}, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC INPUT CHARACTERISTICS						
Input High Voltage	V_{IH}	V_{EE} + 1.65		V_{CC}	V	
Input Low Voltage	V_{IL}	V_{EE}		V_{CC} − 0.2	V	
Input Differential Range	V_{ID}	0.2		3.4	V p-p	T_A = −40°C to +85°C (±1.7 V between input pins)
		0.2		2.8	V p-p	T_A = 85°C to 125°C (±1.4 V between input pins)
Input Capacitance	C_{IN}		0.4		pF	
Input Resistance			50		Ω	
Differential Mode			100		Ω	
Common Mode			50		kΩ	Open termination
Input Bias Current			20		μA	
DC OUTPUT CHARACTERISTICS						
Output High Voltage	V_{OH}	V_{CC} − 0.55	V_{CC} − 0.40	V_{CC} − 0.25	V	
Output Low Voltage	V_{OL}	V_{CC} − 2.75	V_{CC} − 2.35	V_{CC} − 1.9	V	
Output Differential Range	V_{OD}	1.54	1.95	2.22	V	
Reference Voltage	V_{REF}					
Output Voltage			(V_{CC} + 1)/2		V	−500 μA to +500 μA
Output Resistance			250		Ω	
AC PERFORMANCE						
Operating Frequency			7.5		GHz	>1.1 V differential output swing, V_{CC} = 3.3 V ± 10%
Propagation Delay	t_{PD}	127	158	202	ps	V_{CC} = 3.3 V ± 10%, V_{ICM} = V_{REF}, V_{ID} = 1.6 V p-p
Propagation Delay Temperature Coefficient			140		fs/°C	
Propagation Delay Skew (Device to Device)				65	ps	V_{ID} = 1.6 V p-p
Output Rise Time	t_R		100	125	ps	20%/80%
Output Fall Time	t_F		80	95	ps	80%/20%
Wideband Random Jitter[1]	RJ		110		fs rms	V_{ID} = 1.6 V p-p, 6 V/ns, V_{ICM} = 1.85 V
Additive Phase Noise						
622.08 MHz			−132		dBc/Hz	@10 Hz offset
			−143		dBc/Hz	@100 Hz offset
			−151		dBc/Hz	@1 kHz offset
			−156		dBc/Hz	@10 kHz offset
			−157		dBc/Hz	@100 kHz offset
			−156		dBc/Hz	>1 MHz offset
245.76 MHz			−133		dBc/Hz	@10 Hz offset
			−143		dBc/Hz	@100 Hz offset
			−153		dBc/Hz	@1 kHz offset
			−158		dBc/Hz	@10 kHz offset
			−159		dBc/Hz	@100 kHz offset
			−158		dBc/Hz	>1 MHz offset

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
122.88 MHz			−150		dBc/Hz	@10 Hz offset
			−156		dBc/Hz	@100 Hz offset
			−160		dBc/Hz	@1 kHz offset
			−161		dBc/Hz	@10 kHz offset
			−161		dBc/Hz	@100 kHz offset
			−160		dBc/Hz	>1 MHz offset
POWER SUPPLY						
Supply Voltage Requirement	V_{CC}	2.97		3.63	V	
Power Supply Current						
Negative Supply Current	I_{VEE}	66	111	150	mA	Includes output current
Positive Supply Current	I_{VCC}	34	55	73	mA	
Power Supply Rejection[2]	PSR_{VCC}		13		ps/V	V_{CC} = 3.3 V ± 10%
Output Swing Supply Rejection[3]			−15		dB	V_{CC} = 3.3 V ± 10%

[1] Calculated from SNR of ADC method. See Figure 8 for rms jitter vs. input slew rate.
[2] Change in t_{PD} per change in V_{CC}.
[3] Change in output swing per change in V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_{CC} to GND)	6.0 V
Input Voltage	−0.5 V to V_{CC} + 0.5 V
Maximum Output Voltage	V_{CC} + 0.5 V
Minimum Output Voltage	V_{EE} − 0.5 V
Input Termination	±2 V
Voltage Reference	V_{CC} − V_{EE}
Operating Temperature Range, Ambient	−40°C to +125°C
Operating Temperature, Junction	150°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL PERFORMANCE

The ADCLK914 is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, use an airflow source.

To determine the junction temperature on the application PCB

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by the customer at top center of package.
Ψ_{JT} is determined by the values listed in Table 3.
PD is the power dissipation.

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JB} are provided for package comparison and PCB design considerations.

Table 3. Thermal Parameters for ADCLK914 16-Lead LFCSP

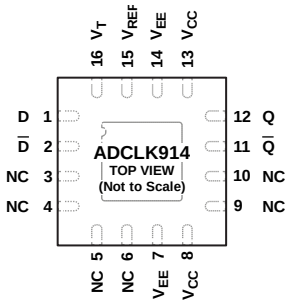
Symbol	Description[1]	Value	Units
θ_{JA}	Junction-to-ambient thermal resistance, 0.0 meters per sec air flow per JEDEC JESD51-2 (still air)	78.4	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 1.0 meter per sec air flow per JEDEC JESD51-6 (moving air)	68.5	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 2.5 m/s air flow per JEDEC JESD51-6 (moving air)	61.4	°C/W
θ_{JB}	Junction-to-board thermal resistance, 1.0 meter per sec air flow per JEDEC JESD51-8 (moving air)	48.8	°C/W
θ_{JC}	Junction-to-case thermal resistance (die-to-heatsink) per MIL-Std 883, Method 1012.1	1.5	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 0 meters per sec air flow per JEDEC JESD51-2 (still air)	2.0	°C/W

[1] Descriptions based on using a 2s2p test board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. NO PHYSICAL CONNECTION TO THE DIE.
2. EXPOSED PAD. NO CONNECT. THE METALLIC BACK SURFACE OF THE PACKAGE IS NOT ELECTRICALLY CONNECTED TO ANY PART OF THE CIRCUIT. IT CAN BE LEFT FLOATING FOR OPTIMAL ELECTRICAL ISOLATION BETWEEN THE PACKAGE HANDLE AND THE SUBSTRATE OF THE DIE. IT CAN ALSO BE SOLDERED TO GROUND ON THE APPLICATION BOARD IF IMPROVED THERMAL AND/OR MECHANICAL STABILITY IS NEEDED. EXPOSED METAL AT THE CORNERS OF THE PACKAGE IS CONNECTED TO THIS BACK SURFACE. ALLOW SUFFICIENT CLEARANCE FOR VIAS AND OTHER COMPONENTS.

06561-002

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D	Noninverting Input.
2	$\overline{D}$	Inverting Input.
3, 4, 5, 6, 9, 10	NC	No Connect. No physical connection to the die.
7, 14	V_{EE}	Negative Supply Voltage.
8, 13	V_{CC}	Positive Supply Voltage.
11	$\overline{Q}$	Inverting Output.
12	Q	Noninverting Output.
15	V_{REF}	Reference Voltage. Reference voltage for biasing ac-coupled inputs.
16	V_T	Center Tap. Center tap of 100 Ω input resistor.
Heat Sink/ Exposed Pad	NC	No Connect. The metallic back surface of the package is not electrically connected to any part of the circuit. It can be left floating for optimal electrical isolation between the package handle and the substrate of the die. It can also be soldered to ground on the application board if improved thermal and/or mechanical stability is needed. Exposed metal at the corners of the package is connected to this back surface. Allow sufficient clearance for vias and other components.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3 V, V_{EE} = 0 V, T_A = 25°C. All outputs terminated through 50 Ω to V_{CC}, unless otherwise noted.

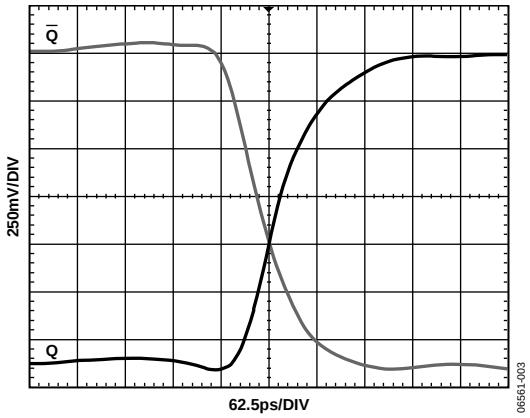


Figure 3. Output Waveform at 1 GHz, V_{CC} = 3.3 V

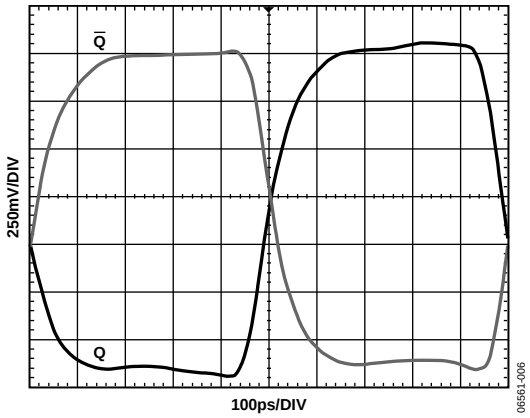


Figure 6. Output Waveform at 1 GHz, V_{CC} = 3.3 V

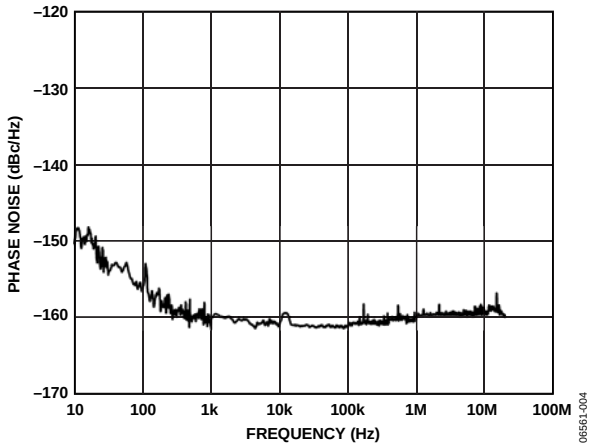


Figure 4. Phase Noise at 122.88 MHz

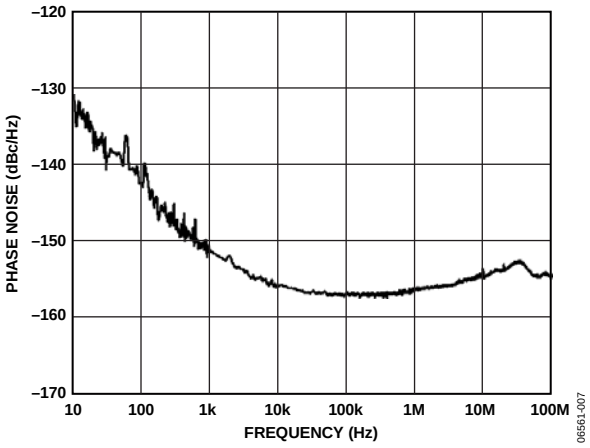


Figure 7. Phase Noise at 622.08 MHz

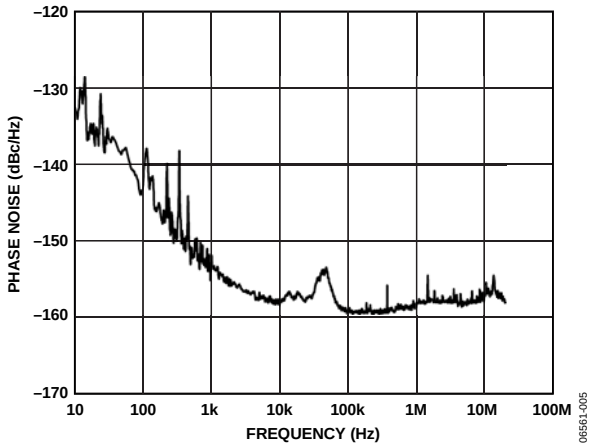


Figure 5. Phase Noise at 245.76 MHz

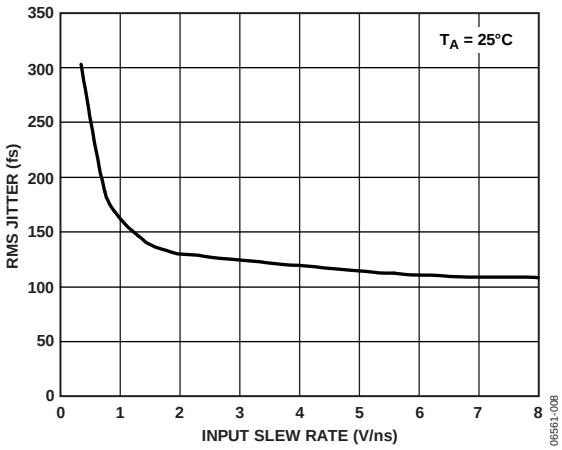


Figure 8. RMS Jitter vs. Input Slew Rate

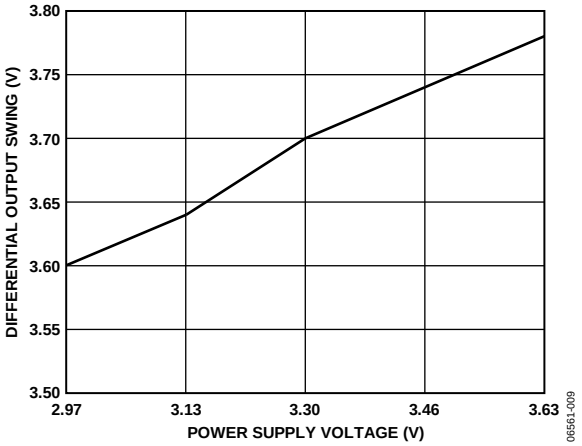


Figure 9. Differential Output Swing vs. Power Supply Voltage

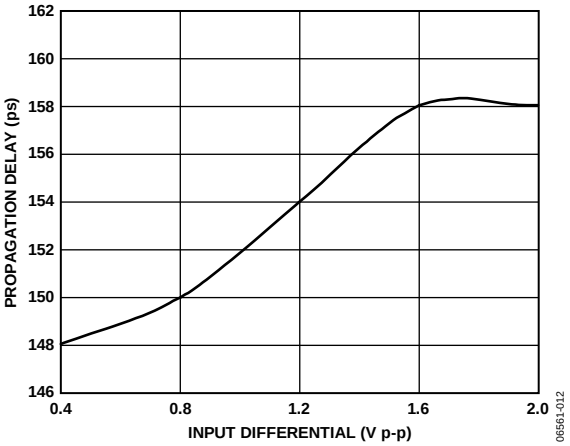


Figure 12. Propagation Delay vs. V_{ID}; V_{ICM} = 2.15 V

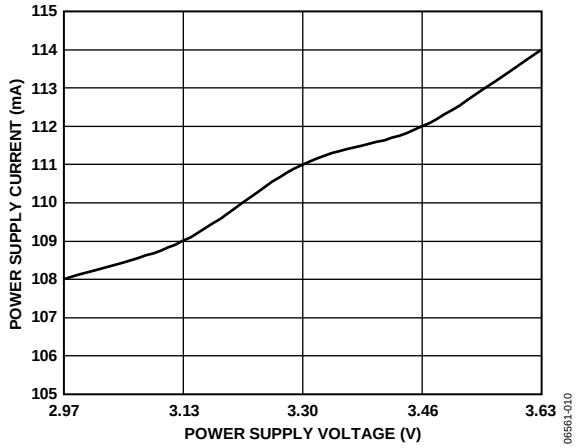


Figure 10. Power Supply Current vs. Power Supply Voltage

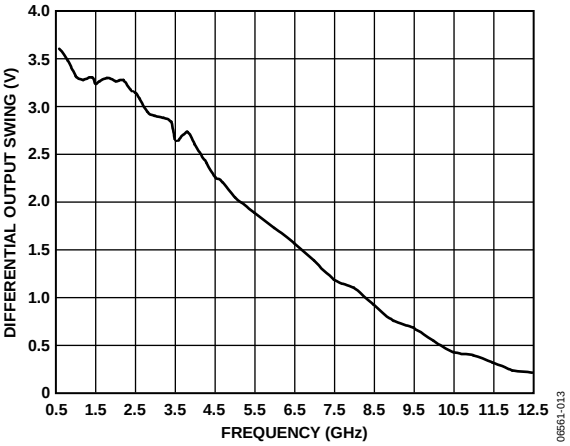


Figure 13. Toggle Rate, Differential Output Swing vs. Frequency

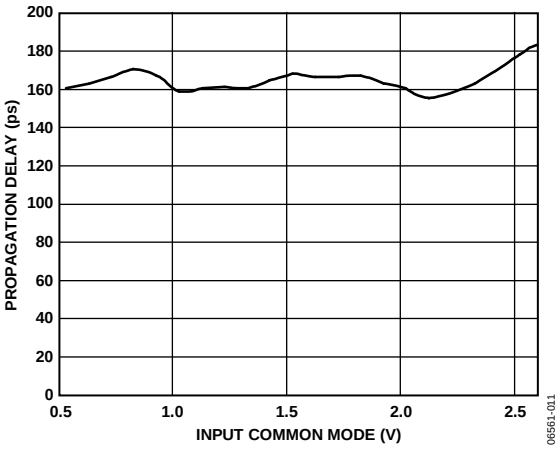


Figure 11. Propagation Delay vs. V_{ICM}; V_{ID} = 1.6 V p-p

APPLICATIONS INFORMATION

POWER/GROUND LAYOUT AND BYPASSING

The ADCLK914 buffer is designed for very high speed applications. Consequently, high speed design techniques must be used to achieve the specified performance. It is critically important to use low impedance supply planes for both the negative supply (V_{EE}) and the positive supply (V_{CC}) planes as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. Place a 1 µF electrolytic bypass capacitor within several inches of each power supply pin to ground. In addition, place multiple high quality 0.001 µF bypass capacitors as close as possible to each V_{EE} and V_{CC} supply pin and connect these capacitors to the GND plane with redundant vias. Carefully select high frequency bypass capacitors for minimum inductance and ESR. To maximize the effectiveness of the bypass capacitors at high frequencies, strictly avoid parasitic layout inductance.

Slew currents may also appear at the V_{DD} and V_{SS} pins of the device being driven by the ADCLK914.

HVDS OUTPUT STAGE

The ADCLK914 has been developed to provide a bipolar interface to any CMOS device that requires extremely low jitter, high amplitude clocks. It is intended to be placed as close as possible to the receiving device and allows the rest of the clock distribution to run at standard CML or PECL levels.

Interconnects must be short and very carefully designed because the single terminated design provides much less margin for error than lower voltage, double terminated transmission techniques.

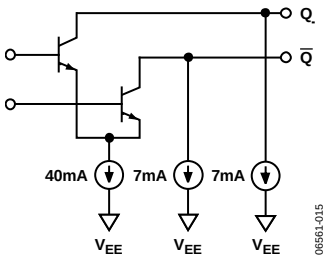


Figure 14. Simplified Schematic Diagram of the ADCLK914 HVDS Output Stage

INTERFACING TO HIGH SPEED DACs

The ADCLK914 is designed to drive high amplitude, low jitter clock signals into high speed, multi-GSPS DACs. The ADCLK914 should be placed as close as possible to the clock input of the DAC so that the high slew rate and high amplitude clock signal that these devices require do not cause routing difficulties, generate EMI, or become degraded by dielectric and other losses. The ADCLK914, in turn, may be driven directly by standard or low swing PECL, CML, CMOS, or LVTTL sources, or by LVDS with simple ac coupling, as illustrated in Figure 15 through Figure 19.

OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed circuit, proper design and layout techniques are essential to obtaining the specified performance. Stray capacitance, inductance, inductive power, and ground impedances, as well as other layout issues, can severely limit performance and can cause oscillation. Discontinuities along input and output transmission lines can also severely limit the specified jitter performance by reducing the effective input slew rate.

Input and output matching have a significant impact on performance. The ADCLK914 buffer provides internal 50 Ω termination resistors for both D and $\overline{D}$ inputs. The return side can be connected to the reference pin provided or to a current sink at V_{CC} − 2 V for use with differential PECL, or to V_{CC} for direct coupled CML. The V_{REF} pin should be left floating any time that it is not used to minimize power consumption.

Note that the ADCLK914 V_{REF} source is current-limited to resist damage from momentary shorts to V_{EE} or V_{CC} and from capacitor charging currents; for this reason, the V_{REF} source cannot be used as a PECL termination supply.

Carefully bypass the termination potential using ceramic capacitors to prevent undesired aberrations on the input signal due to parasitic inductance in the termination return path. If the inputs are directly coupled to a source, care must be taken to ensure that the pins remain within the rated input differential and common-mode ranges.

If the return is floated, the device exhibits 100 Ω cross-termination, but the source must then control the common-mode voltage and supply the input bias currents.

ESD/clamp diodes between the input pins prevent the application of excessive offsets to the input transistors. ESD diodes are not optimized for best ac performance. If a clamp is needed, it is recommended that appropriate external diodes be used.

RANDOM JITTER

The ADCLK914 buffer has been specifically designed to minimize random jitter over a wide input range. Provided that sufficient voltage swing is present, random jitter is affected most by the slew rate of the input signal. Whenever possible, clamp excessively large input signals with fast Schottky diodes because attenuators reduce the slew rate. Input signal runs of more than a few centimeters should be over low loss dielectrics or cables with good high frequency characteristics.

TYPICAL APPLICATION CIRCUITS

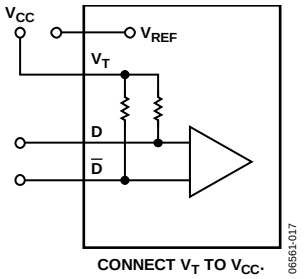


Figure 15. Interfacing to CML Inputs

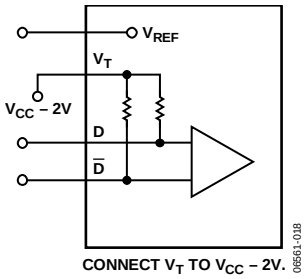


Figure 18. Interfacing to ECL Inputs

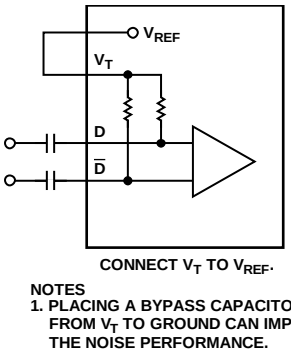


Figure 16. AC Coupling Differential Signals

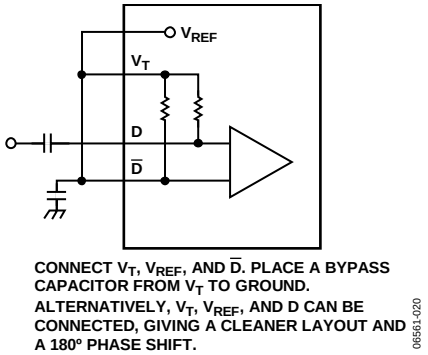


Figure 19. Interfacing to AC-Coupled, Single-Ended Inputs

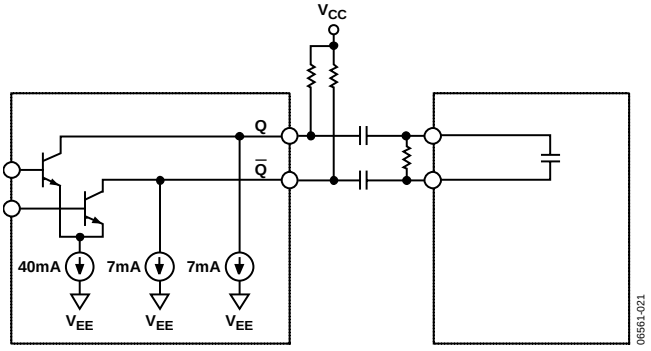


Figure 17. Interfacing to High Speed DAC

OUTLINE DIMENSIONS

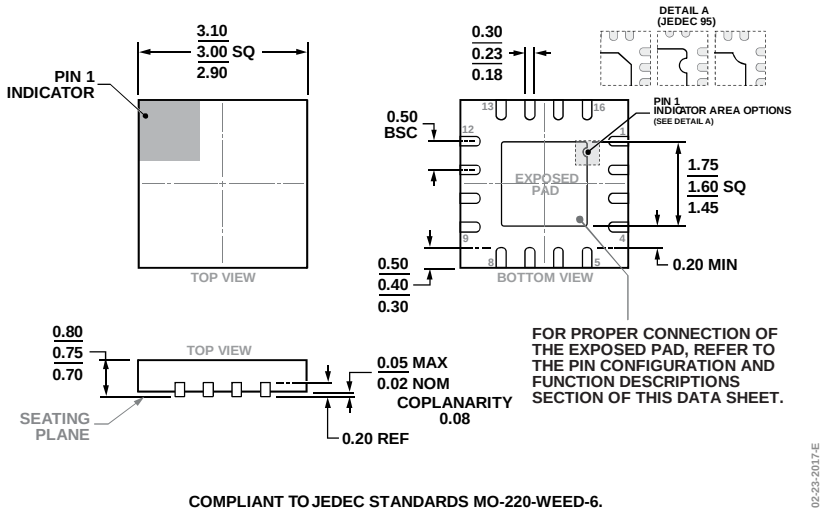


Figure 20. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADCLK914BCPZ-WP	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22
ADCLK914BCPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22
ADCLK914BCPZ-R2	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22
ADCLK914/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.