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REVISION HISTORY

6/2019—Rev. A to Rev. B

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5/2011—Rev. 0 to Rev. A

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1/2005—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±1.5 V or +3 V (at T_A = 25°C, G = +1, R_L = 25 Ω, unless otherwise noted)[1].

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p		50		MHz
0.1 dB Flatness	V_{OUT} = 0.1 V p-p		3.6		MHz
Large Signal Bandwidth	V_{OUT} = 2.0 V p-p		9		MHz
Slew Rate	V_{OUT} = 0.8 V p-p		32		V/µs
NOISE/DISTORTION PERFORMANCE					
Distortion (Worst Harmonic)	f_C = 100 kHz, V_{OUT} = 1.4 V p-p, G = +2		−90		dBc
Input Voltage Noise	f = 100 kHz		4.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.5		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			1.0	2.5	mV
	T_{MIN} – T_{MAX}		2.5		mV
Input Offset Voltage Match			1.0	2.0	mV
Input Bias Current			200	900	nA
	T_{MIN} – T_{MAX}		1.3		µA
Input Offset Current			50	300	nA
Open-Loop Gain	V_{OUT} = ±0.5 V	81	88		dB
INPUT CHARACTERISTICS					
Input Resistance	f = 100 kHz		87		kΩ
Input Capacitance			1.4		pF
Common-Mode Rejection	ΔV_{CM} = ±1 V	−71	−80		dB
OUTPUT CHARACTERISTICS					
Output Resistance			0.2		Ω
+Swing	R_{LOAD} = 25 Ω	+1.33	+1.39		V_P
−Swing	R_{LOAD} = 25 Ω		−1.36	−1.34	V_P
+Swing	R_{LOAD} = 100 Ω	+1.43	+1.47		V_P
−Swing	R_{LOAD} = 100 Ω		−1.46	−1.42	V_P
Peak AC Output Current[2]	SFDR ≤ −70 dBc, f = 100 kHz, V_{OUT} = 0.7 V_P, R_{LOAD} = 4.1 Ω		170		mA
POWER SUPPLY					
Operating Range (Dual Supply)		±1.5		±12.0	V
Supply Current		6	7	8.5	mA/Amp
Power Supply Rejection	ΔV_S = ±0.5 V	−70	−82		dB

[1] Unity gain used to facilitate characterization. To improve stability, a gain of 2 or greater is recommended.
[2] Peak ac output current specification assumes normal ac operation and is not valid for continuous dc operation.

V_S = ±2.5V or +5 V (at T_A = 25°C, G = +1, R_L = 25 Ω, unless otherwise noted)[1].

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p		60		MHz
0.1 dB Flatness	V_{OUT} = 0.1 V p-p		4.8		MHz
Large Signal Bandwidth	V_{OUT} = 2.0 V p-p		14		MHz
Slew Rate	V_{OUT} = 2.0 V p-p		53		V/μs
NOISE/DISTORTION PERFORMANCE					
Distortion (Worst Harmonic)	f_C = 100 kHz, V_{OUT} = 2 V p-p, G = +2		−98		dBc
Input Voltage Noise	f = 100 kHz		4.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.5		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			1.0	2.4	mV
	T_{MIN} – T_{MAX}		2.5		mV
Input Offset Voltage Match			1.0	2.0	mV
Input Bias Current			200	900	nA
	T_{MIN} – T_{MAX}		1.3		μA
Input Offset Current			50	300	nA
Open-Loop Gain	V_{OUT} = ±1.0 V	85	90		dB
INPUT CHARACTERISTICS					
Input Resistance	f = 100 kHz		87		kΩ
Input Capacitance			1.4		pF
Common-Mode Rejection	ΔV_{CM} = ±1 V	−76	−80		dB
OUTPUT CHARACTERISTICS					
Output Resistance			0.2		Ω
+Swing	R_{LOAD} = 25 Ω	+2.29	+2.35		V_P
−Swing	R_{LOAD} = 25 Ω		−2.29	−2.22	V_P
+Swing	R_{LOAD} = 100 Ω	+2.4	+2.45		V_P
−Swing	R_{LOAD} = 100 Ω		−2.43	−2.38	V_P
Peak AC Output Current[2]	SFDR ≤ −70 dBc, f = 100 kHz, V_{OUT} = 1.0 V_P, R_{LOAD} = 4.3 Ω		230		mA
POWER SUPPLY					
Operating Range (Dual Supply)		±1.5		±12.6	V
Supply Current		7	9	12	mA/Amp
Power Supply Rejection	ΔV_S = ±0.5 V	−75	−85		dB

[1] Unity gain used to facilitate characterization. To improve stability, a gain of 2 or greater is recommended.
[2] Peak ac output current specification assumes normal ac operation and is not valid for continuous dc operation.

V_S = ±5 V or +10 V (at T_A = 25°C, G = +1, R_L = 25 Ω, unless otherwise noted)[1].

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p		66		MHz
0.1 dB Flatness	V_{OUT} = 0.1 V p-p		6.5		MHz
Large Signal Bandwidth	V_{OUT} = 2.0 V p-p		14		MHz
Slew Rate	V_{OUT} = 4.0 V p-p		53		V/µs
NOISE/DISTORTION PERFORMANCE					
Distortion (Worst Harmonic)	f_C = 100 kHz, V_{OUT} = 6 V p-p, G = +2		−94		dBc
Input Voltage Noise	f = 100 kHz		4.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.5		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			1.0	2.5	mV
	T_{MIN} – T_{MAX}		2.5		mV
Input Offset Voltage Match			1.0	2.0	mV
Input Bias Current			200	900	nA
	T_{MIN} – T_{MAX}		1.3		µA
Input Offset Current			50	300	nA
Open-Loop Gain	V_{OUT} = ±2.0 V	85	94		dB
INPUT CHARACTERISTICS					
Input Resistance	f = 100 kHz		87		kΩ
Input Capacitance			1.4		pF
Common-Mode Rejection	ΔV_{CM} = ±1 V	−84	−94		dB
OUTPUT CHARACTERISTICS					
Output Resistance			0.2		Ω
+Swing	R_{LOAD} = 25 Ω	+4.48	+4.69		V_P
−Swing	R_{LOAD} = 25 Ω		−4.90	−4.42	V_P
+Swing	R_{LOAD} = 100 Ω	+4.87	+4.92		V_P
−Swing	R_{LOAD} = 100 Ω		−4.88	−4.81	V_P
Peak AC Output Current[2]	SFDR ≤ −80 dBc, f = 100 kHz, V_{OUT} = 3 V_P, R_{LOAD} = 12 Ω		250		mA
POWER SUPPLY					
Operating Range (Dual Supply)		±1.5		±12.6	V
Supply Current		7	9	12	mA/Amp
Power Supply Rejection	ΔV_S = ±0.5 V	−76	−85		dB

[1] Unity gain used to facilitate characterization. To improve stability, a gain of 2 or greater is recommended.
[2] Peak ac output current specification assumes normal ac operation and is not valid for continuous dc operation.

V_S = ±12 V or +24 V (at T_A = 25°C, G = +1, R_L = 25 Ω, unless otherwise noted)[1].

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p		69		MHz
0.1 dB Flatness	V_{OUT} = 0.1 V p-p		7.6		MHz
Large Signal Bandwidth	V_{OUT} = 2.0 V p-p		14		MHz
Slew Rate	V_{OUT} = 4.0 V p-p		53		V/µs
NOISE/DISTORTION PERFORMANCE					
Distortion (Worst Harmonic)	f_C = 100 kHz, V_{OUT} = 20 V p-p, G = +5		−84		dBc
Input Voltage Noise	f = 100 kHz		4.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.5		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			1.0	3.0	mV
	T_{MIN} – T_{MAX}		2.5		mV
Input Offset Voltage Match			1.0	2.0	mV
Input Bias Current			200	900	nA
	T_{MIN} – T_{MAX}		1.3		µA
Input Offset Current			50	300	nA
Open-Loop Gain	V_{OUT} = ±3.0 V	90	96		dB
INPUT CHARACTERISTICS					
Input Resistance	f = 100 kHz		87		kΩ
Input Capacitance			1.4		pF
Common-Mode Rejection	ΔV_{CM} = ±1 V	−85	−96		dB
OUTPUT CHARACTERISTICS					
Output Resistance			0.2		Ω
+Swing	R_{LOAD} = 100 Ω	+11.67	+11.81		V_P
−Swing	R_{LOAD} = 100 Ω		−11.72	−11.58	V_P
Peak AC Output Current[2]	SFDR ≤ −80 dBc, f = 100 kHz, V_{OUT} = 10 V_P, R_{LOAD} = 32 Ω		310		mA
POWER SUPPLY					
Operating Range (Dual Supply)		±1.5		±12.6	V
Supply Current		8.5	11	15	mA/Amp
Power Supply Rejection	ΔV_S = ±0.5 V	−76	−86		dB

[1] Unity gain used to facilitate characterization. To improve stability, a gain of 2 or greater is recommended.
[2] Peak ac output current specification assumes normal ac operation and is not valid for continuous dc operation.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	26.4 V
Power Dissipation[1]	See Figure 4
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

[1] Thermal resistance for standard JEDEC 4-layer board:
8-lead SOIC_N: θ_{JA} = 157.6°C/W
8-Lead SOIC_N_EP: θ_{JA} = 47.2°C/W

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be dissipated safely by the AD8397 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package.

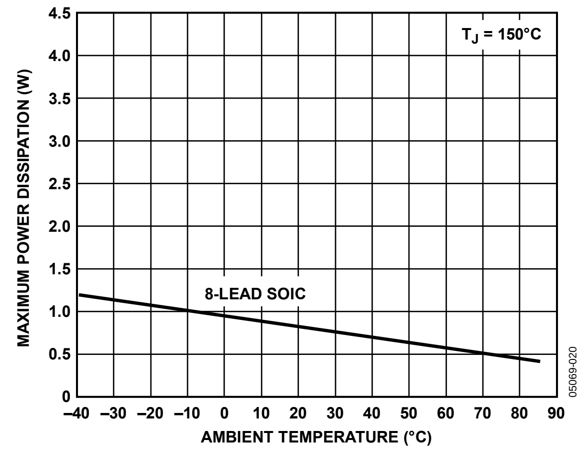
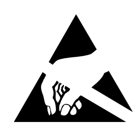


Figure 4. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

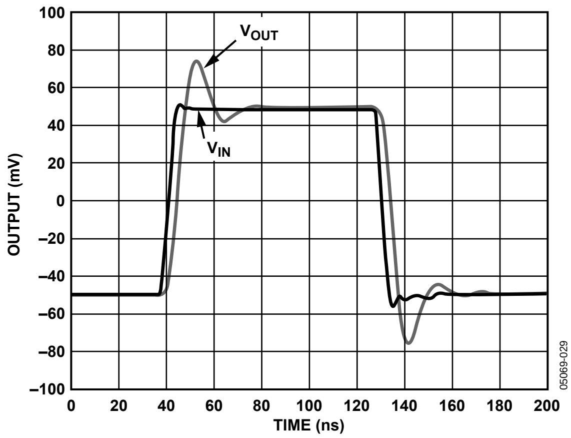


Figure 5. Small Signal Pulse Response (G = +1, V_S = ±5 V, R_L = 25 Ω)

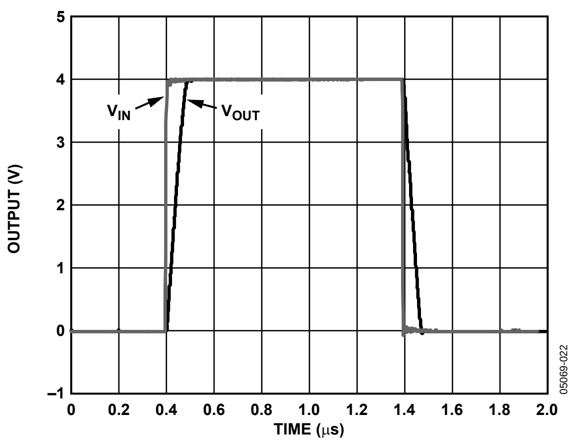


Figure 6. Large Signal Pulse Response (0 V to 4 V, V_S = ±5 V, R_L = 25 Ω)

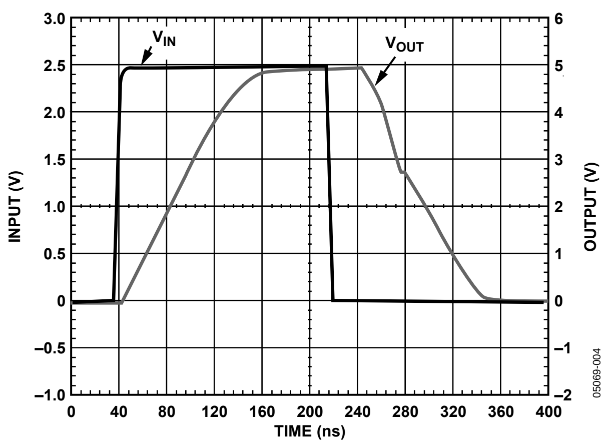


Figure 7. Output Overdrive Recovery
(V_S = ±5 V, Gain = +2, R_L = 25 Ω)

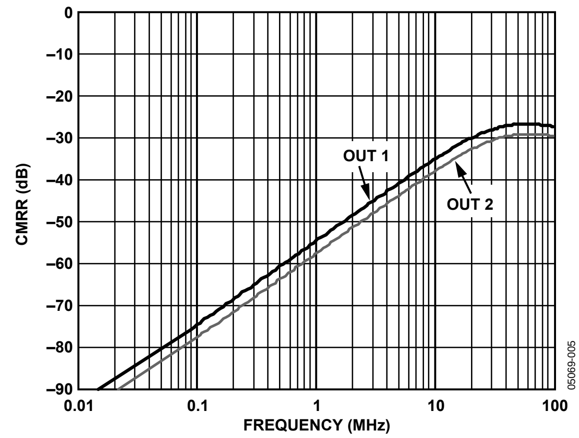


Figure 8. Common-Mode Rejection (CMRR) vs. Frequency
(V_S = ±5 V, R_L = 25 Ω)

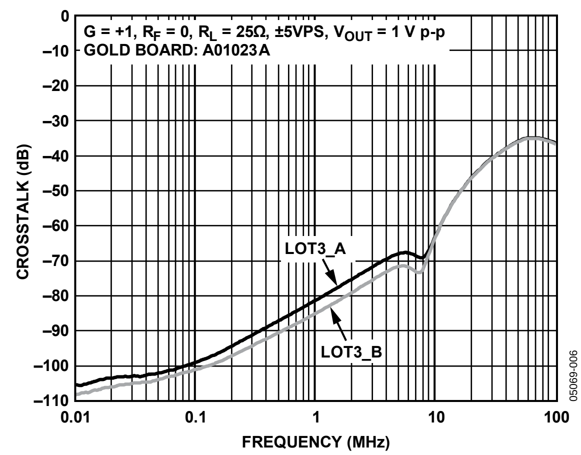


Figure 9. Output-to-Output Crosstalk vs. Frequency
(V_S = ±5 V, V_O = 1 V p-p, R_L = 25 Ω)

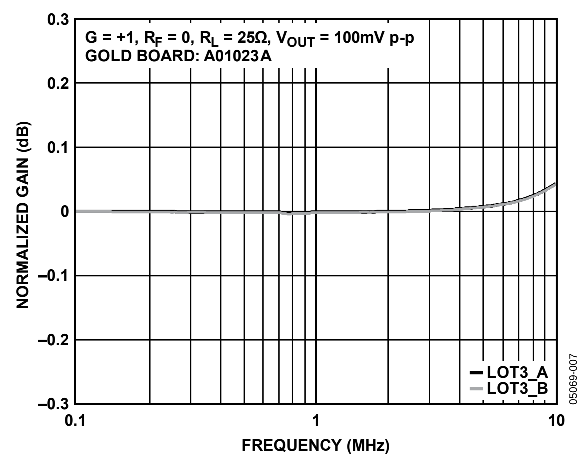


Figure 10. 0.1 dB Flatness
(V_S = ±5 V, V_O = 0.1 V p-p, Gain = +1, R_L = 25 Ω)

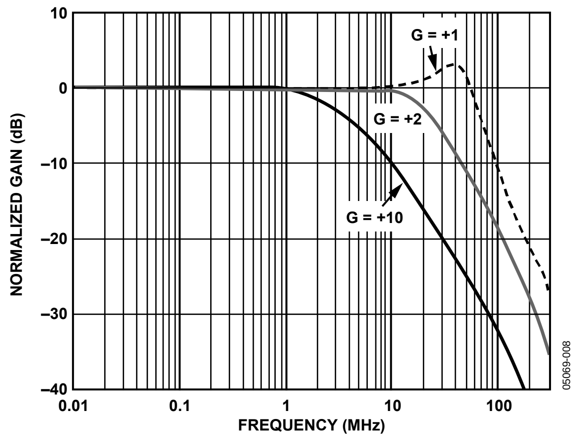


Figure 11. Small Signal Frequency Response for Various Gains (V_S = ±5 V, V_O = 0.1 V p-p, R_L = 25 Ω)

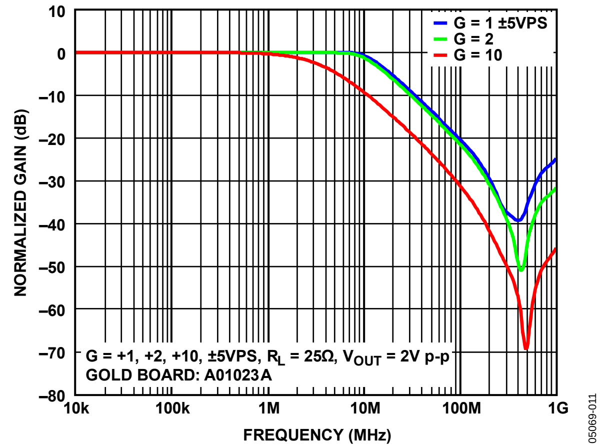


Figure 14. Large Signal Frequency Response for Various Gains (V_S = ±5 V, V_O = 2 V p-p, R_L = 25 Ω)

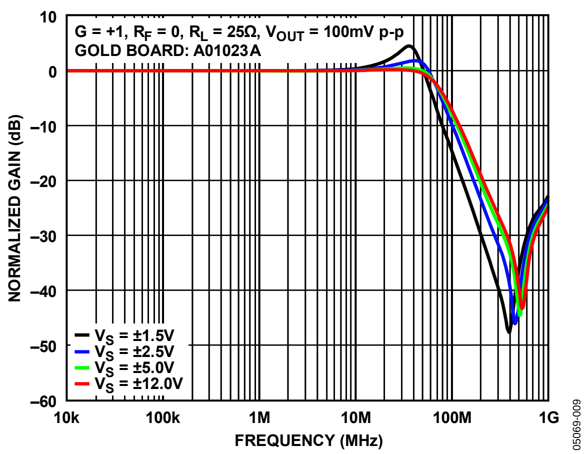


Figure 12. Small Signal Frequency Response for Various Supplies (Gain = +1, V_O = 0.1 V p-p, R_L = 25 Ω)

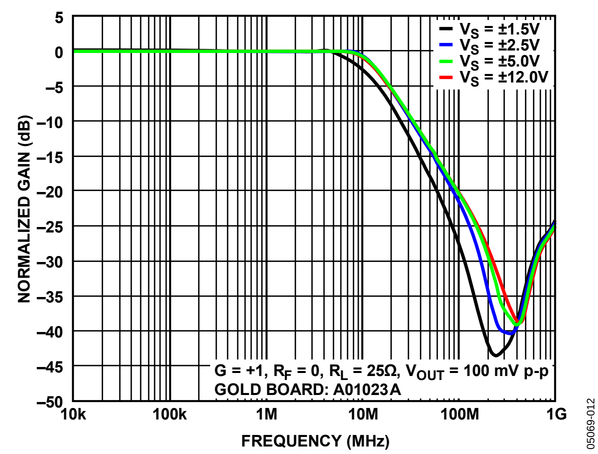


Figure 15. Large Signal Frequency Response for Various Supplies (Gain = +1, V_O = 2 V p-p, R_L = 25 Ω)

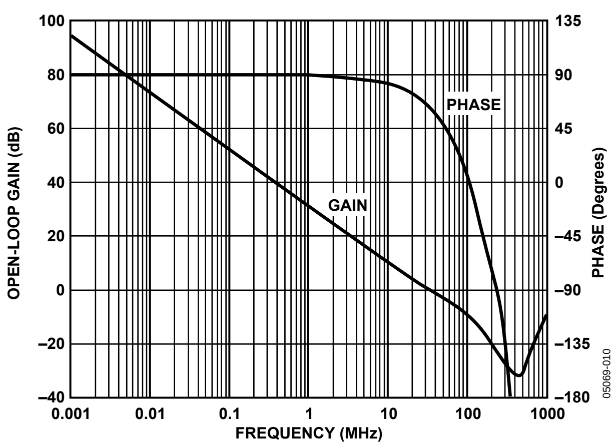


Figure 13. Open-Loop Gain and Phase vs. Frequency (V_S = ±5 V, R_L = 25 Ω)

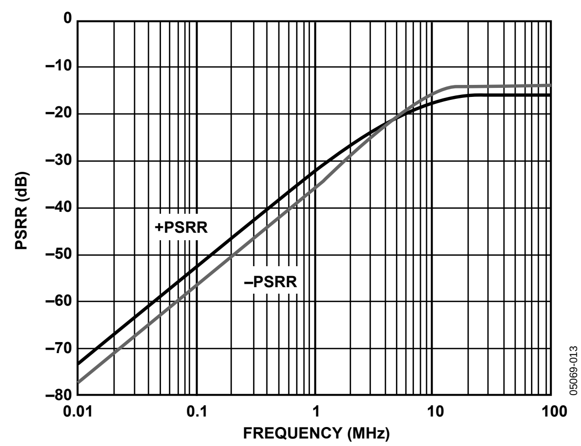


Figure 16. Power Supply Rejection Ratio (PSRR) vs. Frequency (V_S = ±5 V, R_L = 25 Ω)

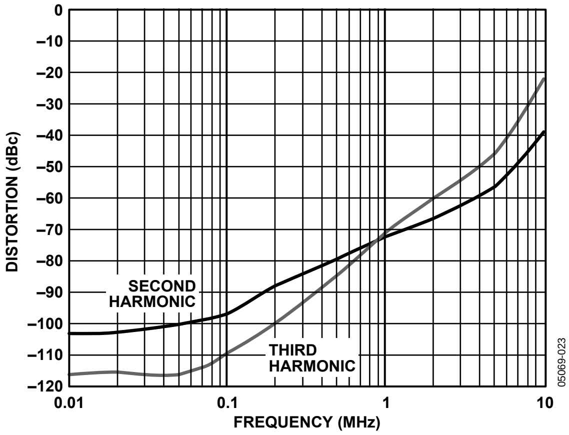


Figure 17. Distortion vs. Frequency (V_S = ±5 V, V_O = 2 V p-p, G = +2, R_L = 25 Ω)

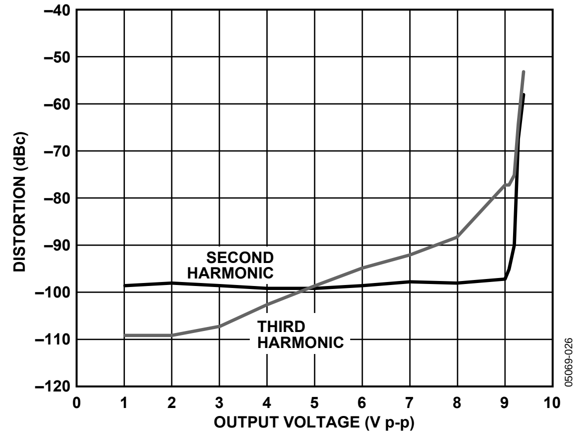


Figure 20. Distortion vs. Output Voltage @ 100 kHz, (V_S = ±5 V, G = +2, R_L = 25 Ω)

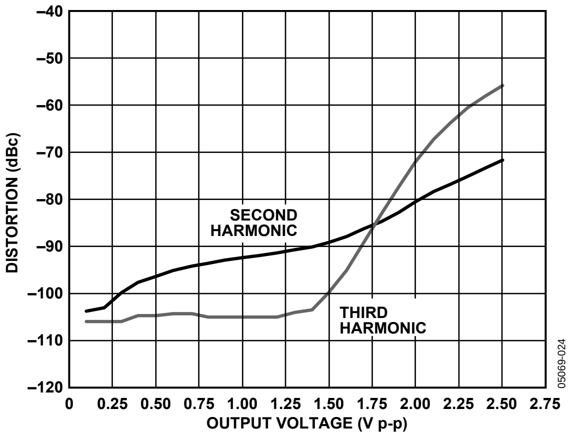


Figure 18. Distortion vs. Output Voltage @ 100 kHz, (V_S = ±1.5 V, G = +2, R_L = 25 Ω)

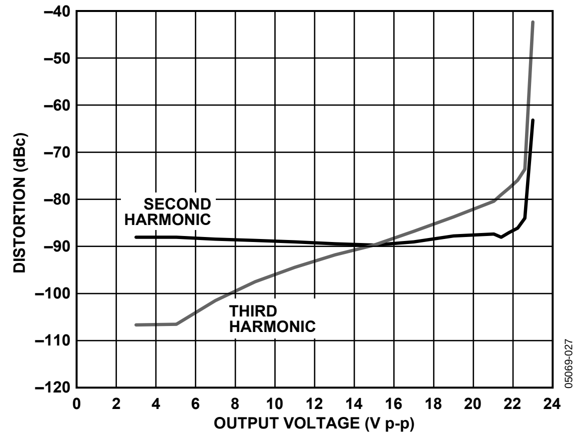


Figure 21. Distortion vs. Output Voltage @ 100 kHz, (V_S = ±12 V, G = +5, R_L = 50 Ω)

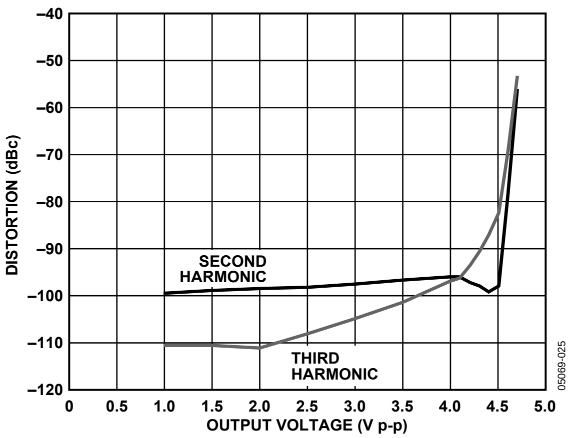


Figure 19. Distortion vs. Output Voltage @ 100 kHz, (V_S = ±2.5 V, G = +2, R_L = 25 Ω)

APPLICATIONS INFORMATION

The AD8397 is a voltage feedback operational amplifier that features an H-bridge input stage and common-emitter, rail-to-rail output stage. The AD8397 can operate from a wide supply range, ±1.5 V to ±12 V. When driving light loads, the rail-to-rail output is capable of swinging to within 0.2 V of either rail. The output can also deliver high linear output current when driving heavy loads, up to 310 mA into 32 Ω while maintaining –80 dBc SFDR. The AD8397 is fabricated on Analog Devices proprietary XFCB-HV.

POWER SUPPLY AND DECOUPLING

The AD8397 can be powered with a good quality, well-regulated, low noise supply from ±1.5 V to ±12 V. Pay careful attention to decoupling the power supply. Use high quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), to minimize the supply voltage ripple and power dissipation. Locate a 0.1 µF MLCC decoupling capacitor(s) no more than 1/8 inch away from the power supply pin(s). A large tantalum 10 µF to 47 µF capacitor is recommended to provide good decoupling for lower frequency signals and to supply current for fast, large signal changes at the AD8397 outputs.

LAYOUT CONSIDERATIONS

As with all high speed applications, pay careful attention to printed circuit board (PCB) layout to prevent associated board parasitics from becoming problematic. The PCB should have a low impedance return path (or ground) to the supply. Removing the ground plane from all layers in the immediate area of the amplifier helps to reduce stray capacitances. The signal routing should be short and direct in order to minimize the parasitic inductance and capacitance associated with these traces. Locate termination resistors and loads as close as possible to their respective inputs and outputs. Keep input traces as far apart as possible from the output traces to minimize coupling (crosstalk) though the board.

When the AD8397 is configured as a differential driver, as in some line driving applications, provide a symmetrical layout to the extent possible in order to maximize balanced performance. When running differential signals over a long distance, the traces on the PCB should be close together or any differential wiring should be twisted together to minimize the area of the inductive loop that is formed. This reduces the radiated energy and makes the circuit less susceptible to RF interference. Adherence to stripline design techniques for long signal traces (greater than approximately 1 inch) is recommended.

UNITY-GAIN OUTPUT SWING

When operating the AD8397 in a unity-gain configuration, the output does not swing to the rails and is constrained by the H-bridge input. This can be seen by comparing the output overdrive recovery in Figure 7 and the input overdrive recovery in Figure 22. To avoid overdriving the input and to realize the full swing afforded by the rail-to-rail output stage, use the amplifier in a gain of two or greater.

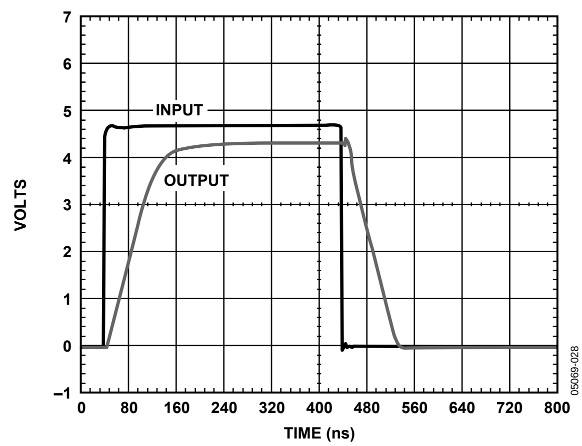


Figure 22. Unity-Gain Input Overdrive Recovery

CAPACITIVE LOAD DRIVE

When driving capacitive loads, many high speed operational amplifiers exhibit peaking in their frequency response. In a gain-of-two circuit, Figure 23 shows that the AD8397 can drive capacitive loads up to 270 pF with only 3 dB of peaking. For amplifiers with more limited capacitive load drive, a small series resistor (R_S) is generally used between the amplifier output and the capacitive load in order to minimize peaking and ensure device stability. Figure 24 shows that the use of a 2.2 Ω series resistor can further extend the capacitive load drive of the AD8397 out to 470 pF, while keeping the frequency response peaking to within 3 dB.

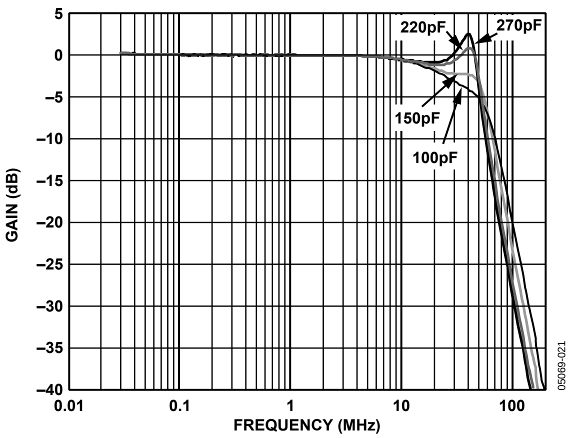


Figure 23. Capacitive Load Peaking Without Series Resistor

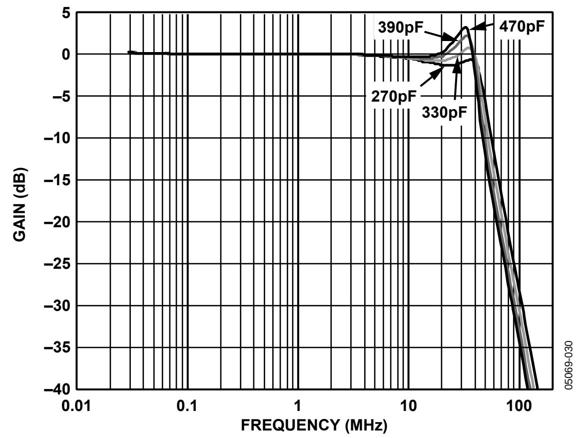


Figure 24. Capacitive Load Peaking with 2.2 Ω Series Resistor

OUTLINE DIMENSIONS

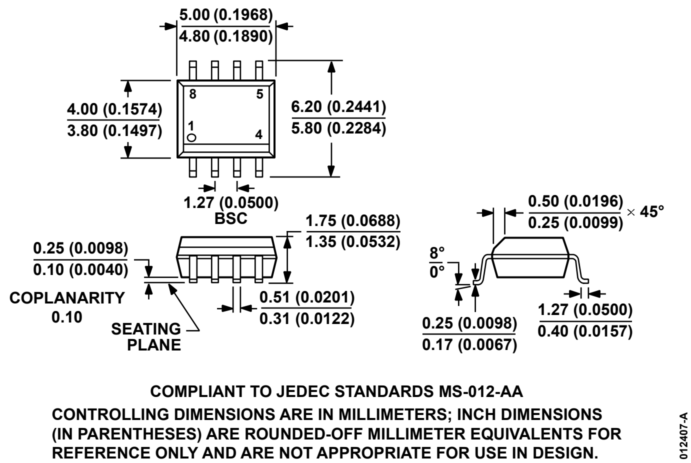


Figure 25. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

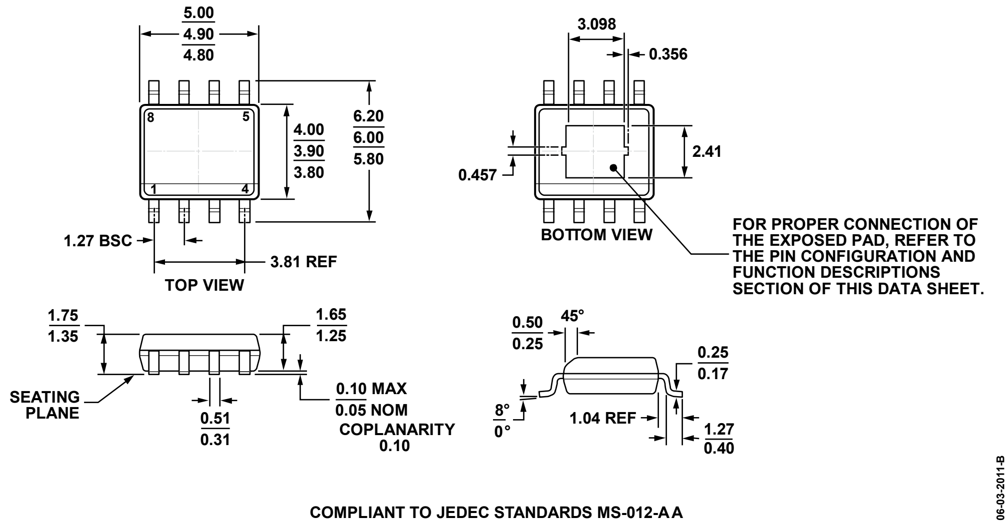


Figure 26. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Package	Package Description	Package Outline
AD8397ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD8397ARZ-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
AD8397ARZ-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8
AD8397ARDZ	−40°C to +85°C	8-Lead SOIC_N_EP	RD-8-2
AD8397ARDZ-REEL	−40°C to +85°C	8-Lead SOIC_N_EP	RD-8-2
AD8397ARDZ-REEL7	−40°C to +85°C	8-Lead SOIC_N_EP	RD-8-2

[1] Z = RoHS Compliant Part.

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