AD8023—SPECIFICATIONS (@ T_A = +25°C, V_S = ±7.5, C_{LOAD} = 10 pF, R_{LOAD} = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD8023A Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
Bandwidth (3 dB)	R_{FB} = 750 Ω No Peaking, G = +3			125		MHz
Bandwidth (0.1 dB)	No Peaking, G = +3			7		MHz
Slew Rate	5 V Step			1200		V/µs
Settling Time to 0.1%	0 V to ±6 V (6 V Step) C_{LOAD} = 300 pF R_{LOAD} > 1 kΩ, R_{FB} = 750 Ω T_A = +25°C to +70°C, R_S = 16.9 Ω			30		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	f_C = 5 MHz, R_L = 150 Ω, V_O = 2 p-p			–72		dBc
Input Voltage Noise	f = 10 kHz			2.0		nV/√Hz
Input Current Noise	f = 10 kHz ($-I_{IN}$)			14		pA/√Hz
Differential Gain (R_L = 150 Ω)	f = 3.58 MHz, G = +2, R_{FB} = 750 Ω			0.06		%
Differential Phase (R_L = 150 Ω)	f = 3.58 MHz, G = +2, R_{FB} = 750 Ω			0.02		Degrees
DC PERFORMANCE						
Input Offset Voltage	T_{MIN} to T_{MAX}		–5	2	5	mV
Offset Drift				2		µV/°C
Input Bias Current (–)	T_{MIN} to T_{MAX}		–45	15	45	µA
Input Bias Current (+)	T_{MIN} to T_{MAX}		–25	5	25	µA
Open-Loop Transresistance			67	111		kΩ
	T_{MIN} to T_{MAX}		50	111		kΩ
INPUT CHARACTERISTICS						
Input Resistance						
+Input	T_{MIN} to T_{MAX}			100		kΩ
–Input	T_{MIN} to T_{MAX}			75		Ω
Input Capacitance				2		pF
Input Common-Mode Voltage Range				±6.0		V
Common-Mode Rejection Ratio						
Input Offset Voltage			50	56		dB
–Input Current				0.2		µA/V
+Input Current				5		µA/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing						
R_L = 1 kΩ	V_{OL}–V_{EE}			0.8	1.0	V
	V_{CC}–V_{OH}			0.8	1.0	V
R_L = 150 Ω	V_{OL}–V_{EE}			1.0	1.3	V
	V_{CC}–V_{OH}			1.0	1.3	V
Output Current			50	70		mA
Short-Circuit Current				300		mA
Capacitive Load Drive				1000		pF
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz			70		dB
DC						
Input Offset Voltage			–5	0.3	5	mV
–Input Bias Current			–10	3	10	µA
POWER SUPPLY						
Operating Range	Single Supply		+4.2		+15	V
	Dual Supply		±2.1		±7.5	V
Quiescent Current/Amplifier				6.2		mA
				7.0	10.0	mA
	T_{MIN} to T_{MAX}					
	Power-Down			1.3	4.0	mA

Model	Conditions	V_S	AD8023A Min	Typ	Max	Units
POWER SUPPLY (Continued)						
Power Supply Rejection Ratio	V_S = ±2.5 V to ±7.5 V					dB
Input Offset Voltage			54	76		dB
–Input Current				0.03		µA/V
+Input Current				0.07		µA/V
DISABLE CHARACTERISTICS						
Off Isolation	f = 6 MHz			–70		dB
Off Output Capacitance	G = +1			12		pF
Turn-On Time				50		ns
Turn-Off Time	R_L = 150 Ω			30		ns
Switching Threshold		$V_{TH} - V_{EE}$		1.6		V

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 15.5 V Total
Internal Power Dissipation
Small Outline (R) . . . . 1.0 Watts (Observe Derating Curves)
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±3 V (Clamped)
Output Voltage Limit
Maximum . . . . . $+V_S$
Minimum . . . . . $-V_S$
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range
R Package . . . . . –65°C to +125°C
Operating Temperature Range
AD8023A . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8023AR	–40°C to +85°C	14-Lead Plastic SOIC	R-14
AD8023AR-REEL	–40°C to +85°C	13" Tape and Reel	R-14
AD8023AR-REEL7	–40°C to +85°C	7" Tape and Reel	R-14
AD8023ACHIPS	–40°C to +85°C	Die	

Maximum Power Dissipation

The maximum power that can be safely dissipated by the AD8023 is limited by the associated rise in junction temperature. The maximum safe junction temperature for the plastic encapsulated parts is determined by the glass transition temperature of the plastic, about 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8023 is internally short circuit protected, this may not be enough to guarantee that the maximum junction temperature is not exceeded under all conditions. To ensure proper operation, it is important to observe the derating curves.

It must also be noted that in (noninverting) gain configurations (with low values of gain resistor), a high level of input overdrive can result in a large input error current, which may result in a significant power dissipation in the input stage. This power must be included when computing the junction temperature rise due to total internal power.

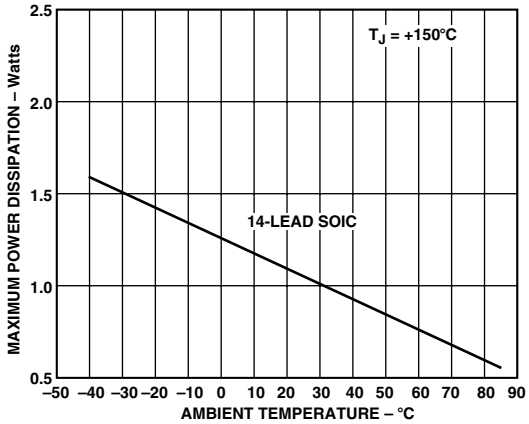


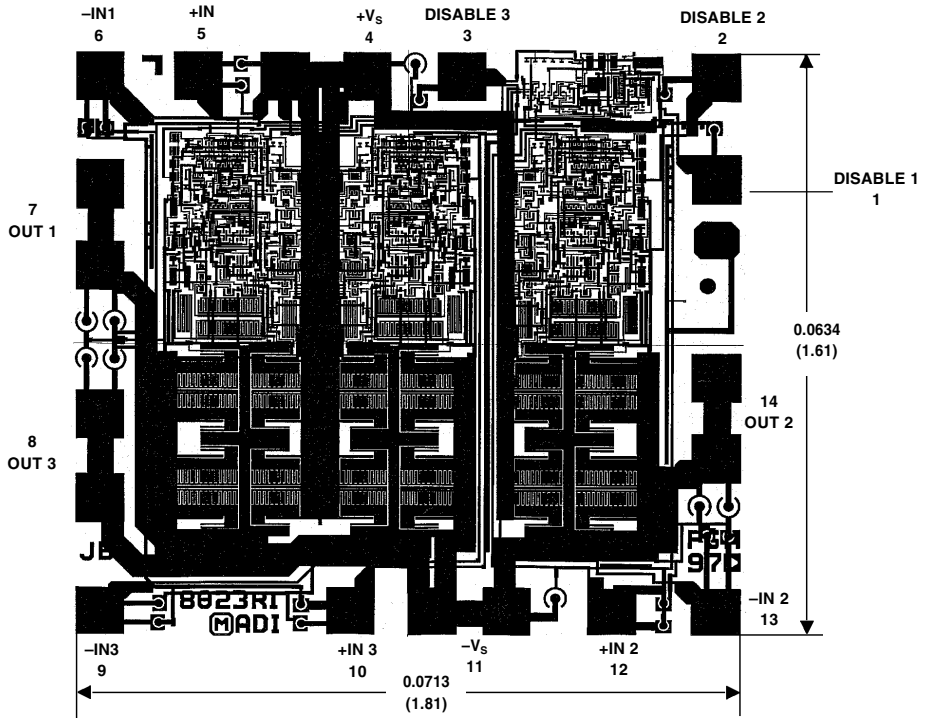
Figure 3. Maximum Power Dissipation vs. Ambient Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8023 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

METALIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Typical Performance Characteristics

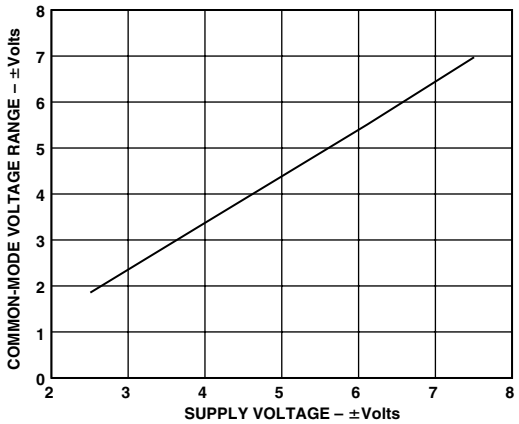


Figure 4. Input Common-Mode Voltage Range vs. Supply Voltage

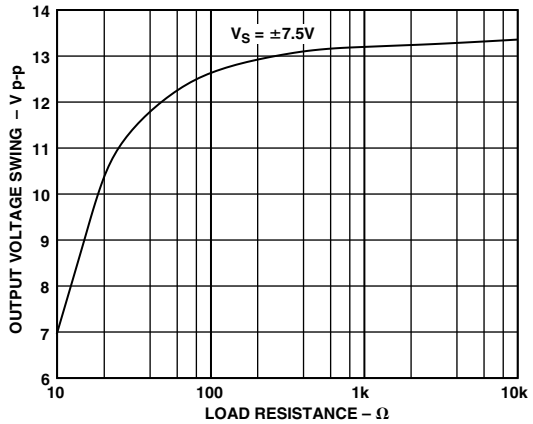


Figure 5. Output Voltage Swing vs. Load Resistance

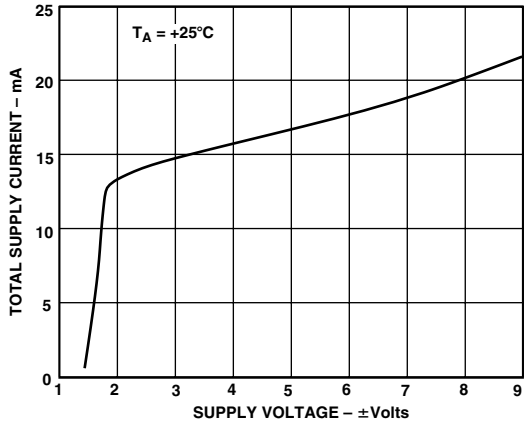


Figure 6. Total Supply Current vs. Supply Voltage

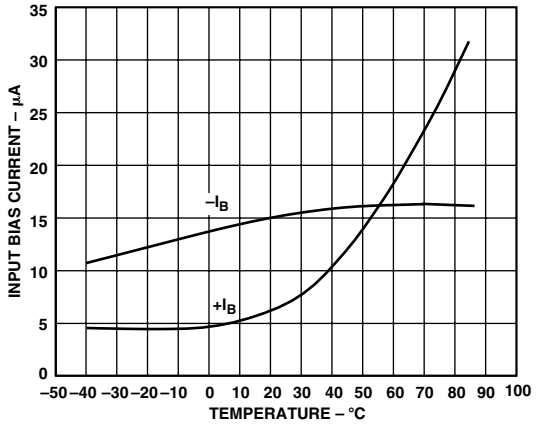


Figure 9. Input Bias Current vs. Temperature

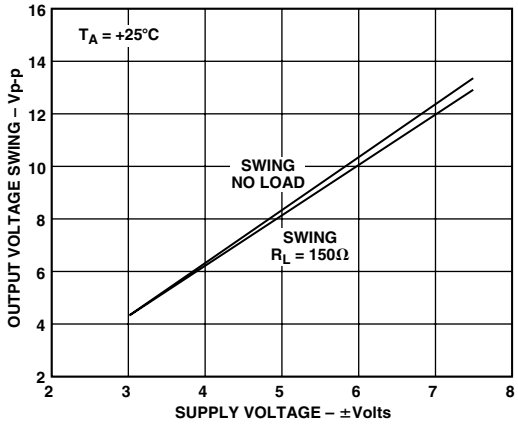


Figure 7. Output Voltage Swing vs. Supply Voltage

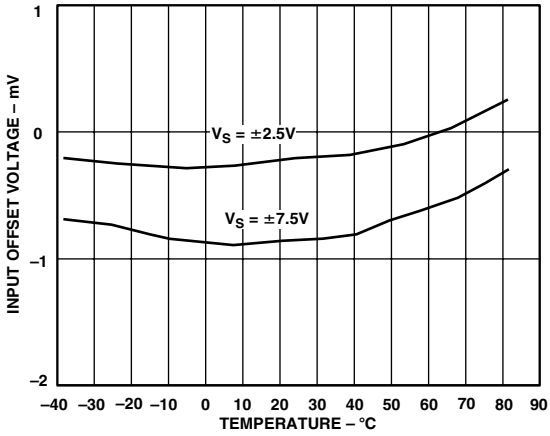


Figure 10. Input Offset Voltage vs. Temperature

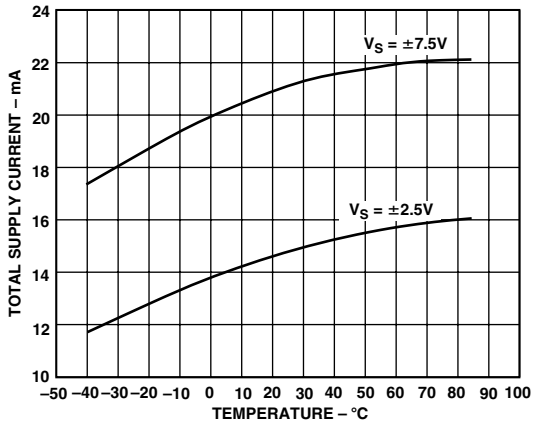


Figure 8. Total Supply Current vs. Temperature

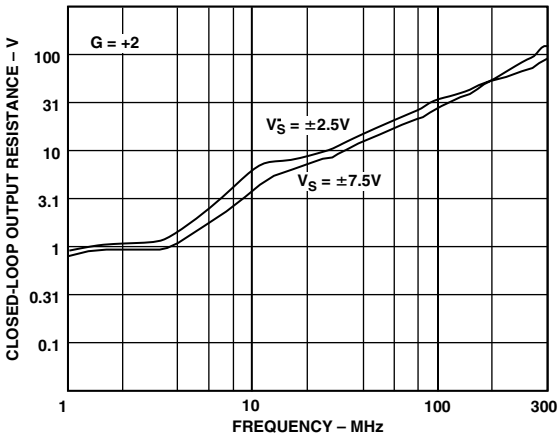


Figure 11. Closed-Loop Output Resistance vs. Frequency

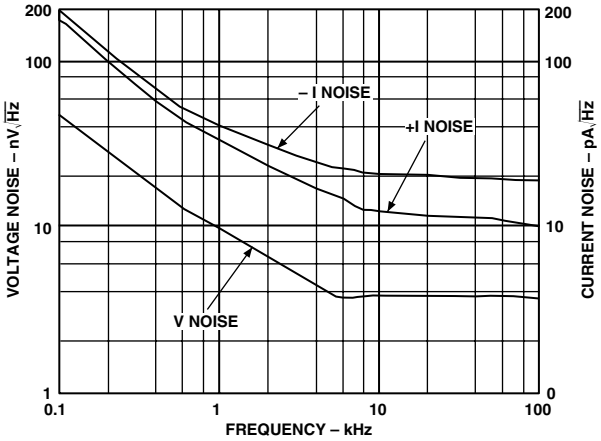


Figure 12. Input Current and Voltage Noise vs. Frequency

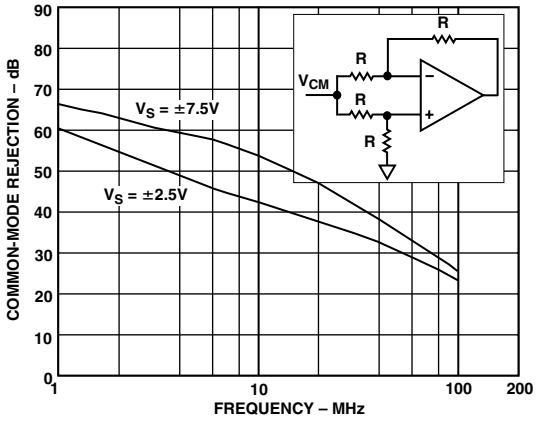


Figure 15. Common-Mode Rejection vs. Frequency

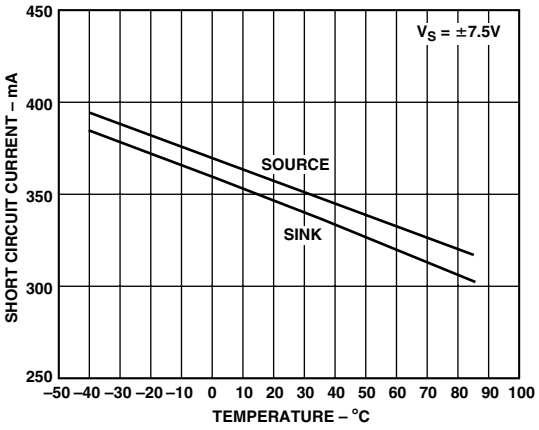


Figure 13. Short Circuit Current vs. Temperature

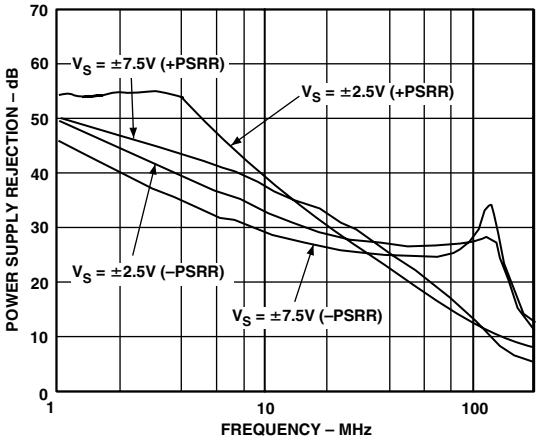


Figure 16. Power Supply Rejection Ratio vs. Frequency

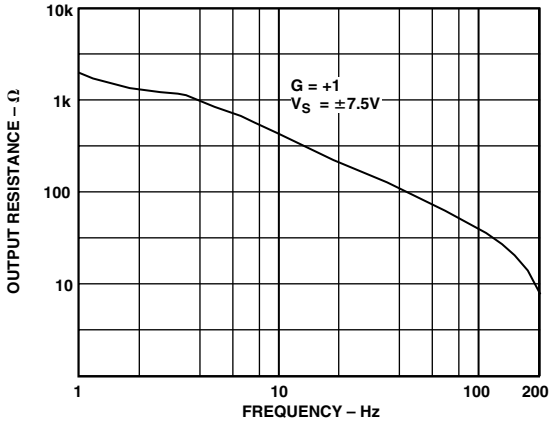


Figure 14. Output Resistance vs. Frequency, Disabled State

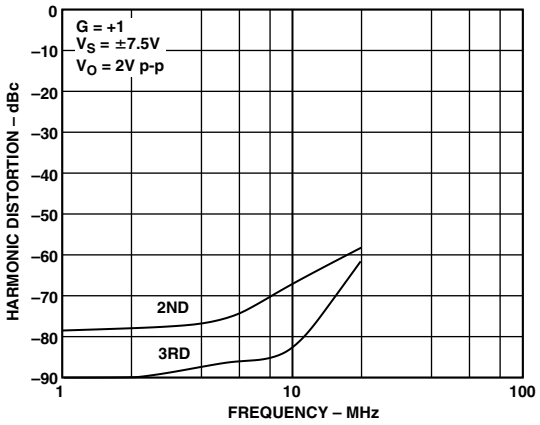


Figure 17. Harmonic Distortion vs. Frequency, R_L = 150 Ω

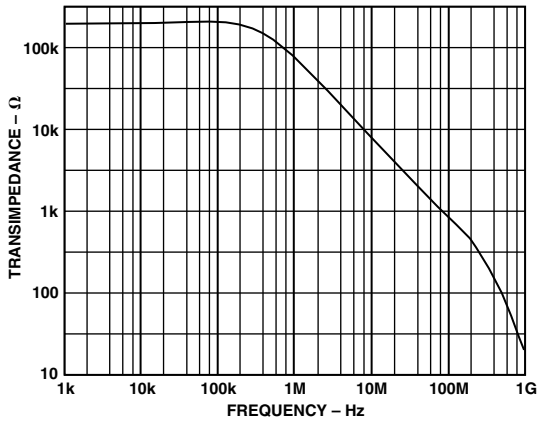


Figure 18. Open-Loop Transimpedance vs. Frequency

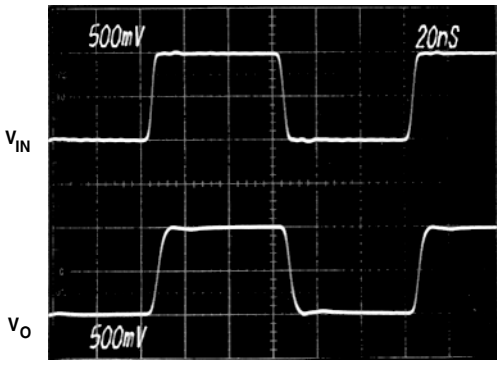


Figure 21. Small Signal Pulse Response, Gain = +1, (R_F = 2 kΩ, R_L = 150 Ω, V_S = ±7.5 V)

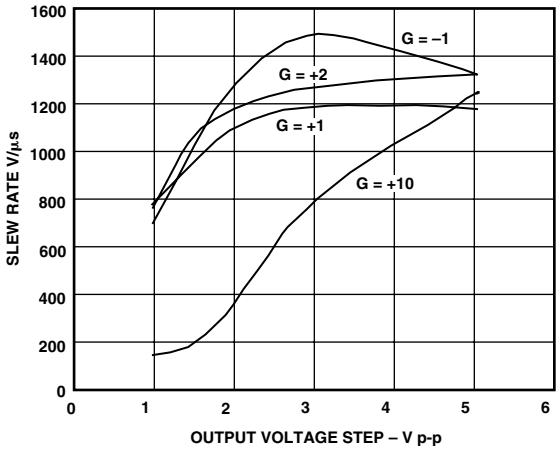


Figure 19. Slew Rate vs. Output Step Size

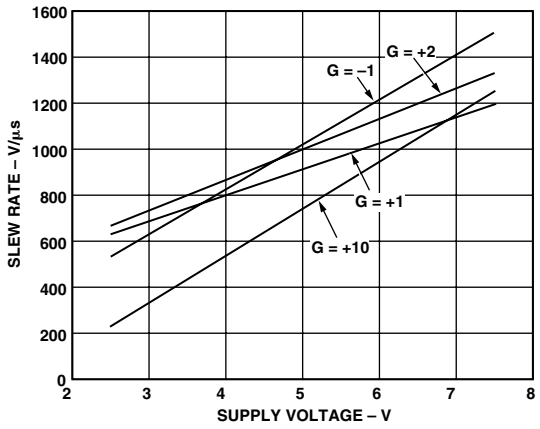


Figure 22. Maximum Slew Rate vs. Supply Voltage

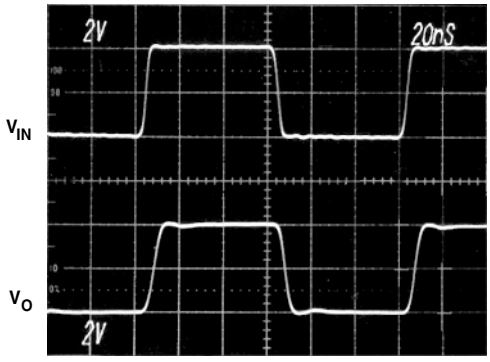


Figure 20. Large Signal Pulse Response, Gain = +1, (R_F = 2 kΩ, R_L = 150 Ω, V_S = ±7.5 V)

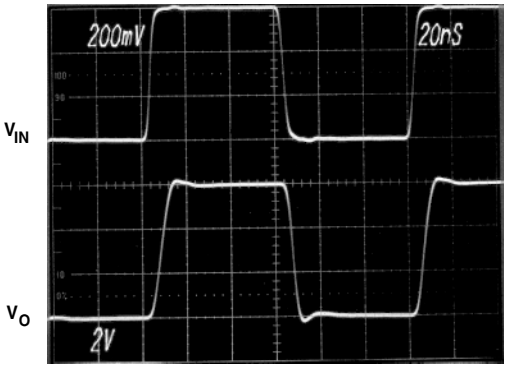


Figure 23. Large Signal Pulse Response, Gain = +10, (R_F = 274 Ω, R_L = 150 Ω, V_S = ±7.5 V)

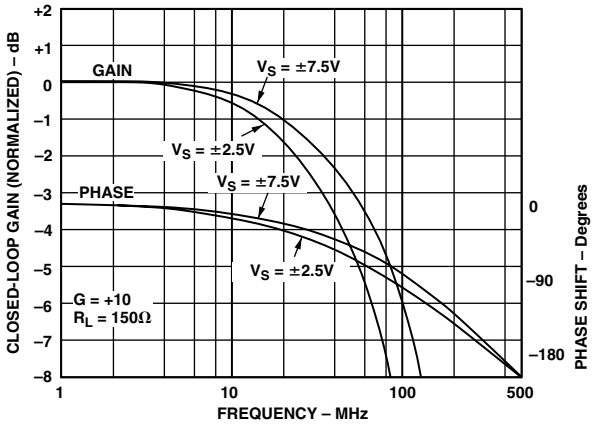


Figure 24. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 150 Ω

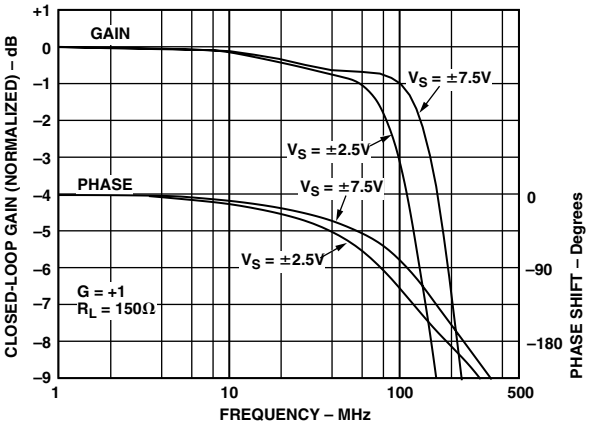


Figure 27. Closed-Loop Gain and Phase vs. Frequency, G = –1, R_L = 150 Ω

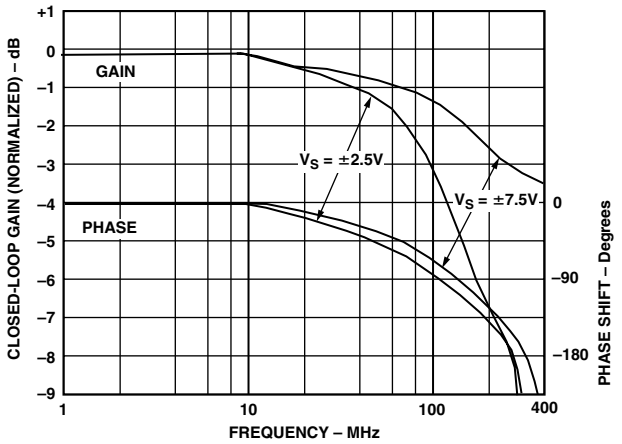


Figure 25. Closed-Loop Gain and Phase vs. Frequency, G = +1, R_L = 150 Ω

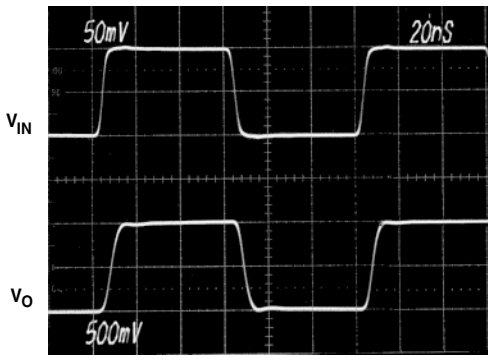


Figure 28. Small Signal Pulse Response, Gain = +10, (R_F = 274 Ω, R_L = 150 Ω, V_S = ±7.5 V)

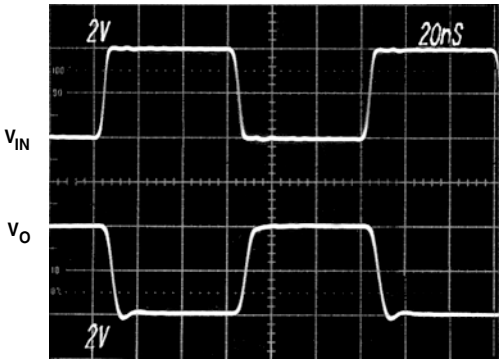


Figure 26. Large Signal Pulse Response, Gain = –1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±7.5 V)

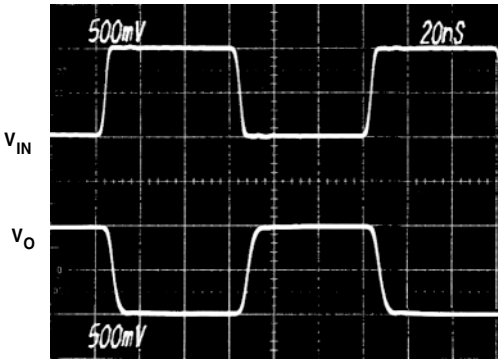


Figure 29. Small Signal Pulse Response, Gain = –1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±7.5 V)

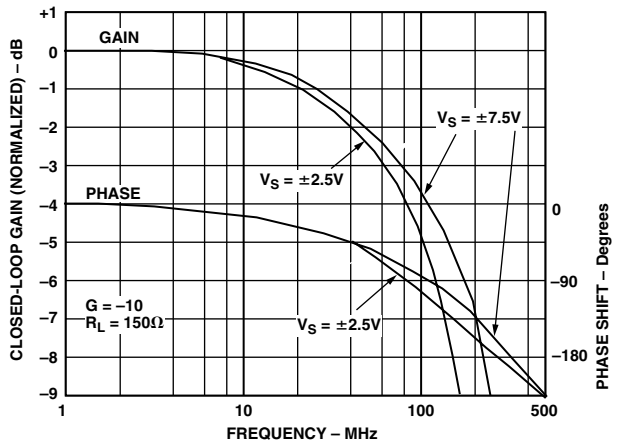


Figure 30. Closed-Loop Gain and Phase vs. Frequency, G = –10, R_L = 150 Ω

General

The AD8023 is a wide bandwidth, triple video amplifier that offers a high level of performance on less than 9.0 mA per amplifier of quiescent supply current. The AD8023 achieves bandwidth in excess of 200 MHz, with low differential gain and phase errors and high output current making it an efficient video amplifier.

The AD8023's wide phase margin coupled with a high output short circuit current make it an excellent choice when driving any capacitive load up to 300 pF.

It is designed to offer outstanding functionality and performance at closed-loop inverting or noninverting gains of one or greater.

Choice of Feedback and Gain Resistors

Because it is a current feedback amplifier, the closed-loop bandwidth of the AD8023 may be customized using different values of the feedback resistor. Table I shows typical bandwidths at different supply voltages for some useful closed-loop gains when driving a load of 150 Ω.

The choice of feedback resistor is not critical unless it is desired to maintain the widest, flattest frequency response. The resistors recommended in the table (chip resistors) are those that will result in the widest 0.1 dB bandwidth without peaking. In applications requiring the best control of bandwidth, 1% resistors are adequate. Resistor values and widest bandwidth figures are shown. Wider bandwidths than those in the table can be attained by reducing the magnitude of the feedback resistor (at the expense of increased peaking), while peaking can be reduced by increasing the magnitude of the feedback resistor.

Increasing the feedback resistor is especially useful when driving large capacitive loads as it will increase the phase margin of the closed-loop circuit. (Refer to the Driving Capacitive Loads section for more information.)

To estimate the –3 dB bandwidth for closed-loop gains of 2 or greater, for feedback resistors not listed in the following table, the following single pole model for the AD8023 may be used:

$$ACL \simeq \frac{G}{1 + SC_T\,(R_F + Gn\,rin)}$$

where: C_T = transcapacitance ≅ 1 pF
R_F = feedback resistor
G = ideal closed loop gain

$$Gn = \left(1 + \frac{R_F}{R_G}\right) = \text{noise gain}$$

rin = inverting input resistance ≅ 150 Ω
ACL = closed loop gain

The –3 dB bandwidth is determined from this model as:

$$f_3 \simeq \frac{1}{2\,\pi\,C_T(R_F + Gn\,rin)}$$

This model will predict –3 dB bandwidth to within about 10% to 15% of the correct value when the load is 150 Ω and V_S = ±7.5 V. For lower supply voltages there will be a slight decrease in bandwidth. The model is not accurate enough to predict either the phase behavior or the frequency response peaking of the AD8023.

It should be noted that the bandwidth is affected by attenuation due to the finite input resistance. Also, the open-loop output resistance of about 6 Ω reduces the bandwidth somewhat when driving load resistors less than about 150 Ω. (Bandwidths will be about 10% greater for load resistances above a couple hundred ohms.)

Table I. –3 dB Bandwidth vs. Closed-Loop Gain and Feedback Resistor, R_L = 150 Ω (SOIC)

V_S – Volts	Gain	R_F – Ohms	BW – MHz
±7.5	+1	2000	460
	+2	750	240
	+10	300	50
	–1	750	150
	–10	250	60
±2.5	+1	2000	250
	+2	1000	90
	+10	300	30
	–1	750	95
	–10	250	50

Driving Capacitive Loads

When used in combination with the appropriate feedback resistor, the AD8023 will drive any load capacitance without oscillation. The general rule for current feedback amplifiers is that the higher the load capacitance, the higher the feedback resistor required for stable operation. Due to the high open-loop transresistance and low inverting input current of the AD8023, the use of a large feedback resistor does not result in large closed-loop gain errors. Additionally, its high output short circuit current makes possible rapid voltage slewing on large load capacitors.

For the best combination of wide bandwidth and clean pulse response, a small output series resistor is also recommended. Table II contains values of feedback and series resistors which result in the best pulse responses. Figure 28 shows the AD8023 driving a 300 pF capacitor through a large voltage step with virtually no overshoot. (In this case, the large and small signal pulse responses are quite similar in appearance.)

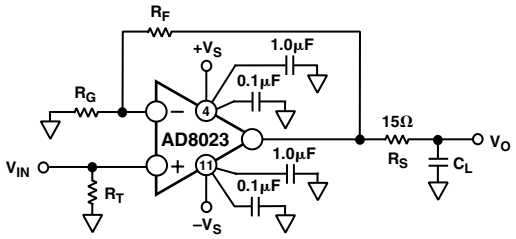


Figure 31. Circuit for Driving a Capacitive Load

Table II. Recommended Feedback and Series Resistors vs. Capacitive Load and Gain

C_L – pF	R_F – Ohms	R_S – Ohms G = 2	R_S – Ohms G ≥ 3
20	2k	0	0
50	2k	10	10
100	2k	15	15
200	3k	10	10
300	3k	10	10
≥500	3k	10	10

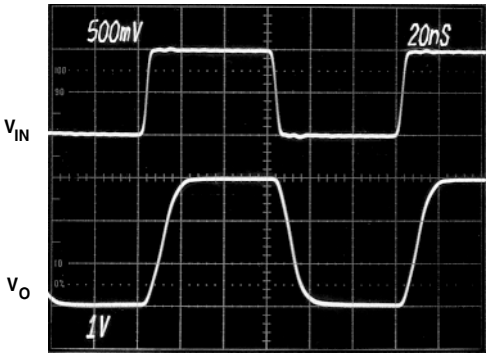


Figure 32. Pulse Response Driving a Large Load Capacitor. C_L = 300 pF, G = +3, R_F = 750 Ω, R_S = 16.9 Ω, R_L = 10 kΩ

Overload Recovery

The three important overload conditions are: input common-mode voltage overdrive, output voltage overdrive, and input current overdrive. When configured for a low closed-loop gain, this amplifier will quickly recover from an input common-mode voltage overdrive; typically in under 25 ns. When configured for a higher gain, and overloaded at the output, the recovery time will also be short. For example, in a gain of +10, with 50% overdrive, the recovery time of the AD8023 is about 20 ns (see Figure 31). For higher overdrive, the response is somewhat slower. For 100% overdrive, (in a gain of +10), the recovery time is about 80 ns.

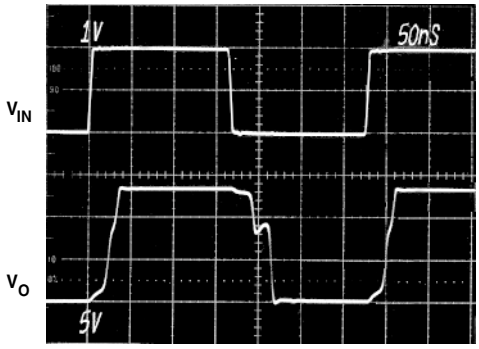


Figure 33. 50% Overload Recovery, Gain = +10, (R_F = 300 Ω, R_L = 1 kΩ, V_S = ±7.5 V)

As noted in the warning under Maximum Power Dissipation, a high level of input overdrive in a high noninverting gain circuit can result in a large current flow in the input stage. Though this current is internally limited to about 30 mA, its effect on the total power dissipation may be significant.

Disable Mode Operation

Pulling the voltage on any one of the Disable pins about 1.6 V up from the negative supply will put the corresponding amplifier into a disabled, powered down, state. In this condition, the amplifier's quiescent current drops to about 1.3 mA, its output becomes a high impedance, and there is a high level of isolation from input to output. In the case of a gain of two line driver for example, the impedance at the output node will be about the same as for a 1.5 kΩ resistor (the feedback plus gain resistors) in parallel with a 12 pF capacitor.

Leaving the Disable pin disconnected (floating) will leave the corresponding amplifier operational, in the enabled state. The input impedance of the disable pin is about 25 kΩ in parallel with a few picofarads. When driven to 0 V, with the negative supply at –7.5 V, about 100 µA flows into the disable pin.

When the disable pins are driven by complementary output CMOS logic, on a single 5 V supply, the disable and enable times are about 50 ns. When operated on dual supplies, level shifting will be required from standard logic outputs to the Disable pins. Figure 33 shows one possible method, which results in a negligible increase in switching time.

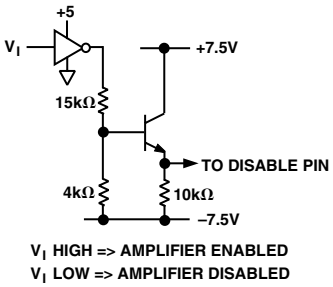


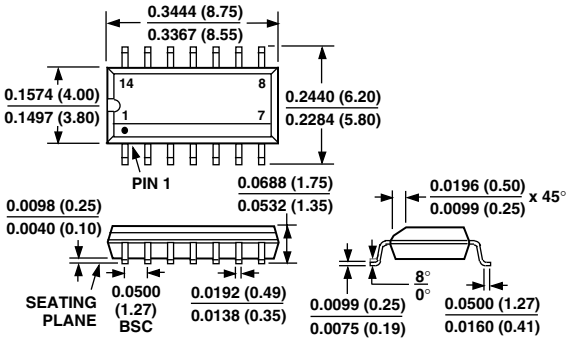
Figure 34. Level Shifting to Drive Disable Pins on Dual Supplies

The AD8023's input stages include protection from the large differential input voltages that may be applied when disabled. Internal clamps limit this voltage to about ±3 V. The high input to output isolation will be maintained for voltages below this limit.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Plastic SOIC
(R-14)



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