AD8011–SPECIFICATIONS

DUAL SUPPLY (@ T_A = 25°C, V_S = ±5 V, G = +2, R_F = 1 kΩ, R_L = 1 kΩ, unless otherwise noted.)

Parameter	Conditions	AD8011A Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O < 1 V p-p	G = +1	340	400		MHz
–3 dB Small Signal Bandwidth, V_O < 1 V p-p	G = +2	180	210		MHz
–3 dB Large Signal Bandwidth, V_O = 5 V p-p	G = +10, R_F = 500 Ω		57		MHz
Bandwidth for 0.1 dB Flatness	G = +2	20	25		MHz
Slew Rate	G = +2, V_O = 4 V Step		3500		V/µs
	G = –1, V_O = 4 V Step		1100		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		25		ns
Rise and Fall Time	G = +2, V_O = 2 V Step		0.4		ns
	G = –1, V_O = 2 V Step		3.7		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	f_C = 5 MHz, V_O = 2 V p-p, G = +2				
	R_L = 1 kΩ		–75		dB
	R_L = 150 Ω		–67		dB
Third Harmonic	R_L = 1 kΩ		–70		dB
	R_L = 150 Ω		–54		dB
Input Voltage Noise	f = 10 kHz		2		nV/√Hz
Input Current Noise	f = 10 kHz, +In		5		pA/√Hz
	–In		5		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 1 kΩ		0.02		%
	R_L = 150 Ω		0.02		%
Differential Phase Error	NTSC, G = +2, R_L = 1 kΩ		0.06		Degrees
	R_L = 150 Ω		0.3		Degrees
DC PERFORMANCE					
Input Offset Voltage			2	5	±mV
	T_{MIN}–T_{MAX}		2	6	±mV
Offset Drift			10		µV/°C
–Input Bias Current			5	15	±µA
	T_{MIN}–T_{MAX}			20	±µA
+Input Bias Current			5	15	±µA
	T_{MIN}–T_{MAX}			20	±µA
Open-Loop Transresistance		800	1300		kΩ
	T_{MIN}–T_{MAX}	550			kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		450		kΩ
Input Capacitance	+Input		2.3		pF
Input Common-Mode Voltage Range		3.8	4.1		±V
Common-Mode Rejection Ratio					
Offset Voltage	V_{CM} = ±2.5 V	–52	–57		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		3.9	4.1		±V
Output Resistance			0.1	0.3	Ω
Output Current	T_{MIN}–T_{MAX}	15	30		mA
Short-Circuit Current			60		mA
POWER SUPPLY					
Operating Range		±1.5		±6.0	V
Quiescent Current	T_{MIN}–T_{MAX}		1.0	1.3	mA
Power Supply Rejection Ratio	V_S = ±5 V ± 1 V	55	58		dB

Specifications subject to change without notice.

SINGLE SUPPLY (@ T_A = 25°C, V_S = 5 V, G = +2, R_F = 1 kΩ, V_{CM} = 2.5 V, R_L = 1 kΩ, unless otherwise noted.)

Parameter	Conditions	AD8011A Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	270	328		MHz
–3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +2	150	180		MHz
–3 dB Large Signal Bandwidth, V_O = 2.5 V p-p	G = +10, R_F = 500 Ω		57		MHz
Bandwidth for 0.1 dB Flatness	G = +2	15	20		MHz
Slew Rate	G = +2, V_O = 2 V Step		2000		V/µs
	G = –1, V_O = 2 V Step		500		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		29		ns
Rise and Fall Time	G = +2, V_O = 2 V Step		0.6		ns
	G = –1, V_O = 2 V Step		4		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	f_C = 5 MHz, V_O = 2 V p-p, G = +2				
	R_L = 1 kΩ		–84		dB
	R_L = 150 Ω		–67		dB
Third Harmonic	R_L = 1 kΩ		–76		dB
	R_L = 150 Ω		–54		dB
Input Voltage Noise	f = 10 kHz		2		nV/√Hz
Input Current Noise	f = 10 kHz, +In		5		pA/√Hz
	–In		5		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 1 kΩ		0.02		%
	R_L = 150 Ω		0.6		%
Differential Phase Error	NTSC, G = +2, R_L = 1 kΩ		0.06		Degrees
	R_L = 150 Ω		0.8		Degrees
DC PERFORMANCE					
Input Offset Voltage			2	5	mV
	T_{MIN}–T_{MAX}		2	6	mV
Offset Drift			10		µV/°C
–Input Bias Current			5	15	±µA
	T_{MIN}–T_{MAX}			20	±µA
+Input Bias Current			5	15	±µA
	T_{MIN}–T_{MAX}			20	±µA
Open-Loop Transresistance		800	1300		kΩ
	T_{MIN}–T_{MAX}	550			kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		450		kΩ
Input Capacitance	+Input		2.3		pF
Input Common-Mode Voltage Range		1.5 to 3.5	1.2 to 3.8		V
Common-Mode Rejection Ratio					
Offset Voltage	V_{CM} = 1.5 V to 3.5 V	–52	–57		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		1.2 to 3.8	0.9 to 4.1		+V
Output Resistance			0.1	0.3	Ω
Output Current	T_{MIN}–T_{MAX}	15	30		mA
Short-Circuit Current			50		mA
POWER SUPPLY					
Operating Range		+3		+12	V
Quiescent Current	T_{MIN}–T_{MAX}		0.8	1.15	mA
Power Supply Rejection Ratio	ΔV_S = ±1 V	55	58		dB

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Internal Power Dissipation[2]
Plastic DIP Package (N) . . . . . Observe Derating Curves
Small Outline Package (R) . . . . . Observe Derating Curves
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±2.5 V
Output Short-Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range (N, R) . . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Specification is for device in free air:
8-Lead PDIP Package: θ_{JA} = 90°C/W
8-Lead SOIC Package: θ_{JA} = 155°C/W

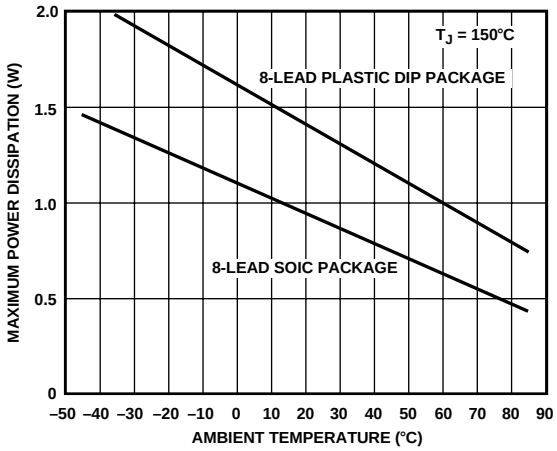


Figure 3. Maximum Power Dissipation vs. Temperature

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8011 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8011 is internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves (shown in Figure 3).

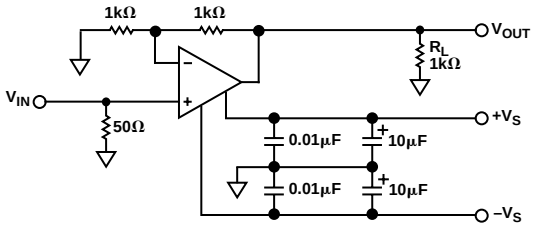


Figure 4. Test Circuit; Gain = +2

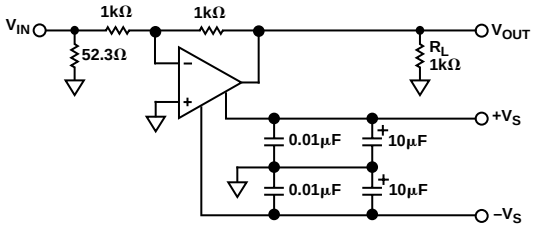


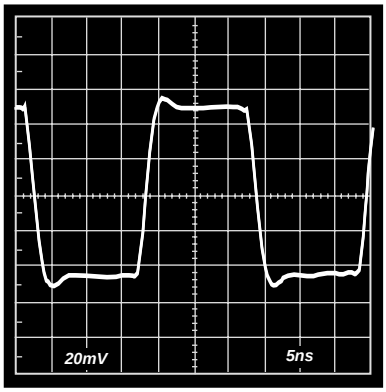
Figure 5. Test Circuit; Gain = –1

ORDERING GUIDE

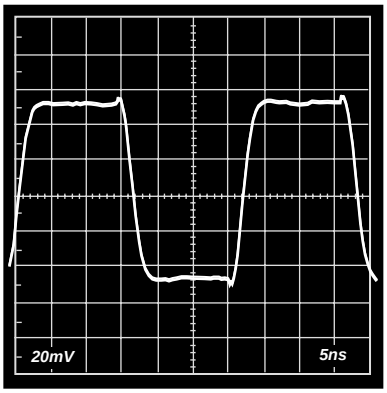
Model	Temperature Range	Package Description	Package Option
AD8011AN	–40°C to +85°C	8-Lead PDIP	N-8
AD8011AR	–40°C to +85°C	8-Lead SOIC	R-8
AD8011AR-REEL	–40°C to +85°C	13" Tape and Reel	R-8
AD8011AR-REEL7	–40°C to +85°C	7" Tape and Reel	R-8

CAUTION

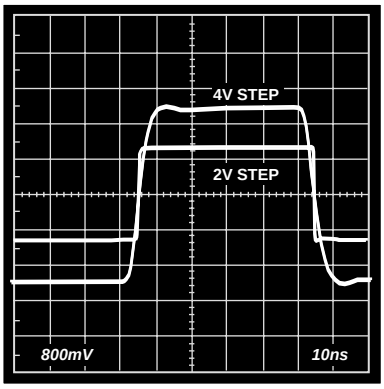
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8011 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



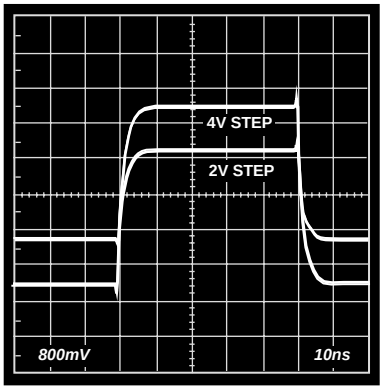
*TPC 1. 100 mV Step Response; G = +2, V_S = ±2.5 V or ±5 V



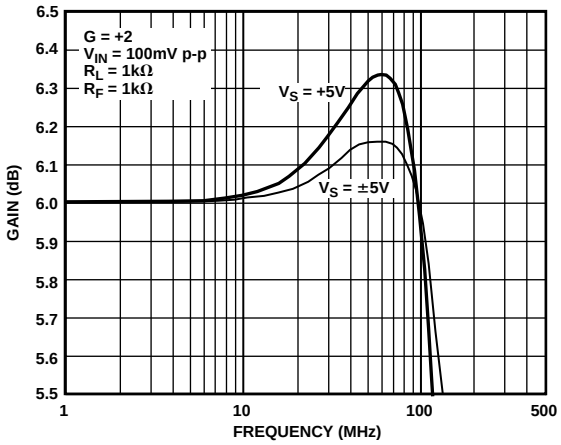
*TPC 4. 100 mV Step Response; G = –1, V_S = ±2.5 V or ±5 V



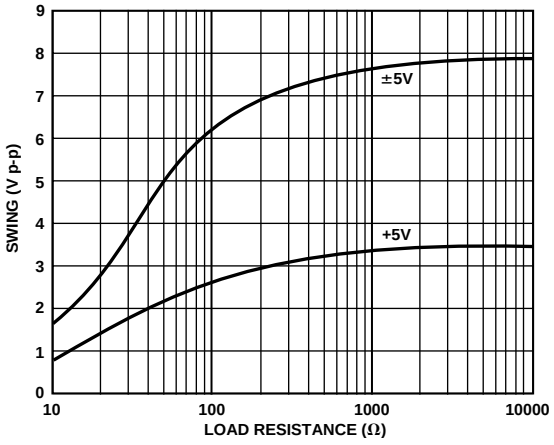
*TPC 2. Step Response; G = +2, V_S = ±2.5 V (2 V Step) and ±5 V (4 V Step)



*TPC 5. Step Response; G = –1, V_S = ±2.5 V (2 V Step) and ±5 V (4 V Step)

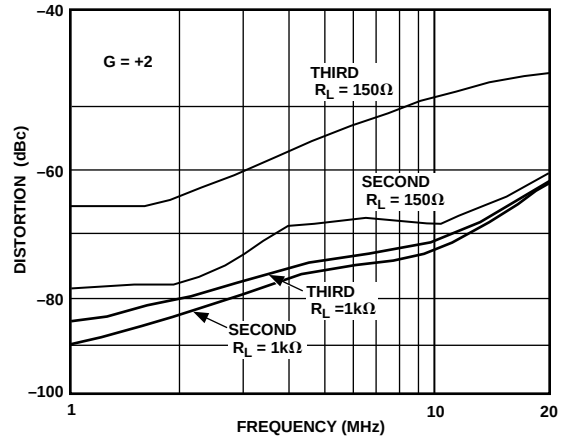


TPC 3. Gain Flatness; G = +2

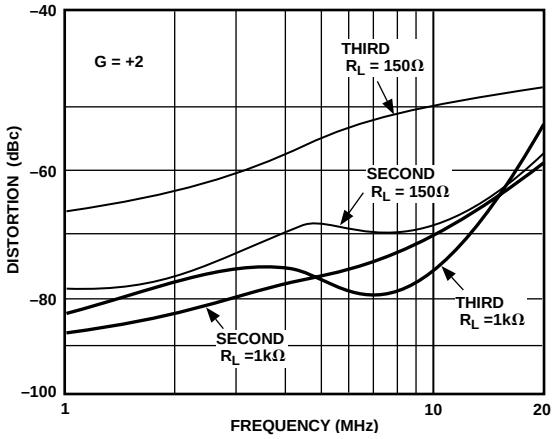


TPC 6. Output Voltage Swing vs. Load

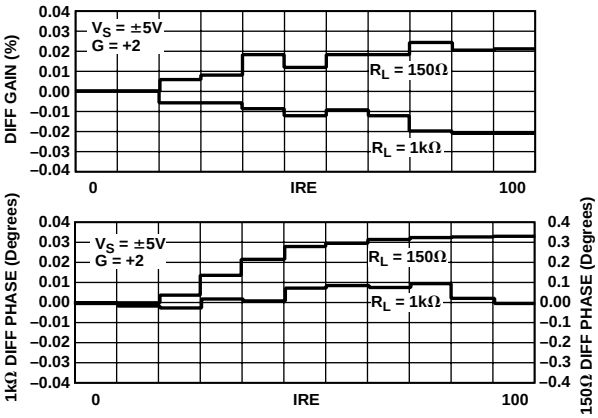
*NOTE: V_S = ±5 V operation is identical to V_S = +5 V single-supply operation.



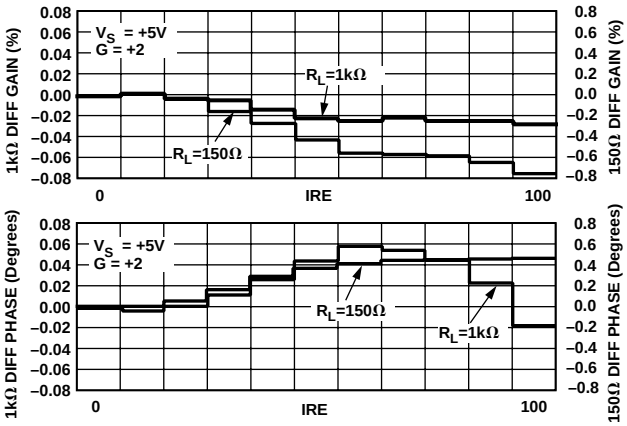
TPC 7. Distortion vs. Frequency; V_S = ±5 V



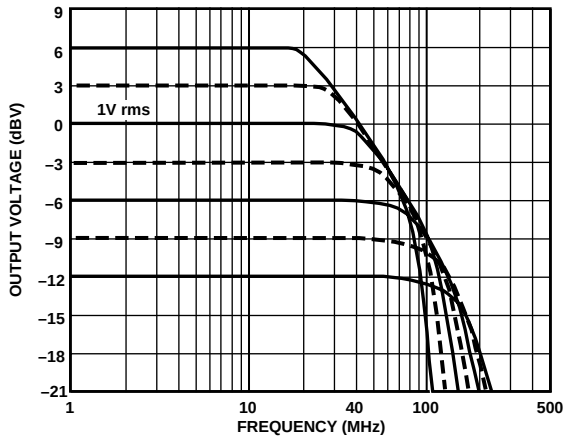
TPC 10. Distortion vs. Frequency; V_S = +5 V



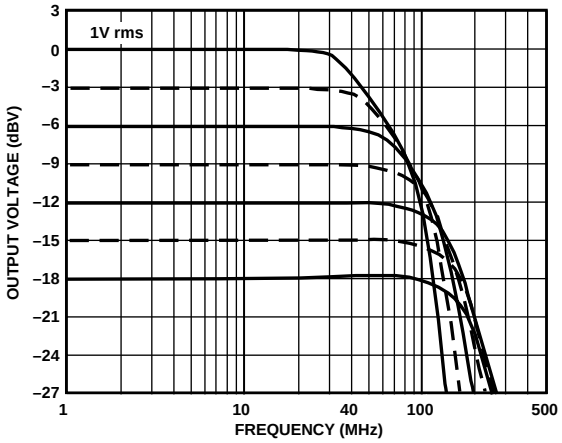
TPC 8. Diff Phase and Diff Gain; V_S = ±5 V



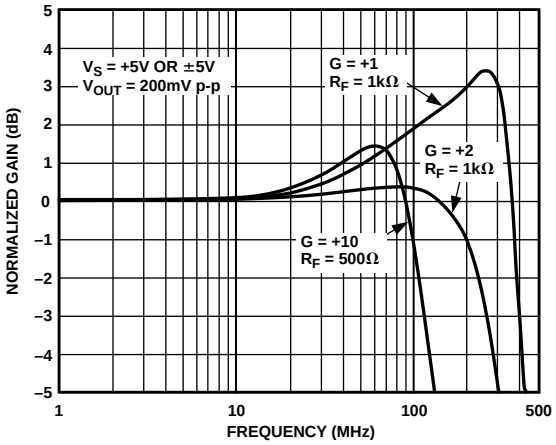
TPC 11. Diff Phase and Diff Gain; V_S = +5 V



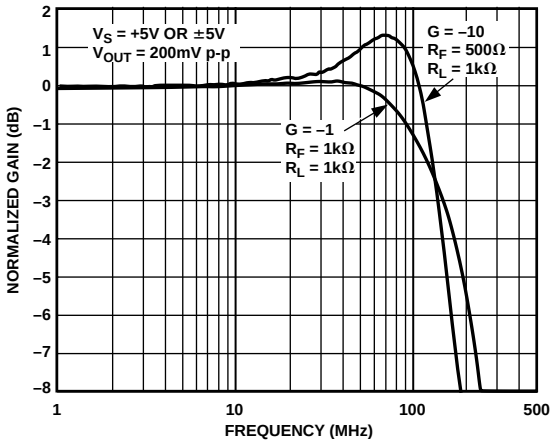
TPC 9. Large Signal Frequency Response; V_S = ±5 V, G = +2



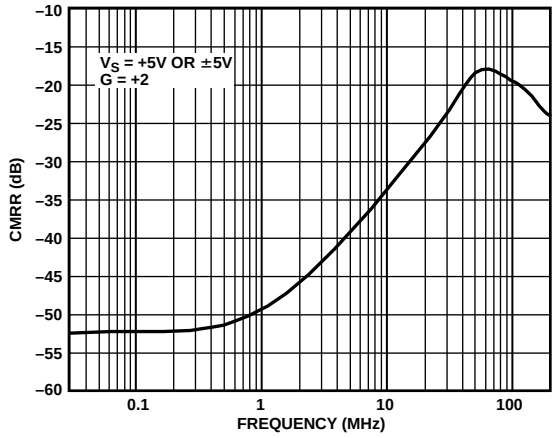
TPC 12. Large Signal Frequency Response; V_S = +5 V, G = +2



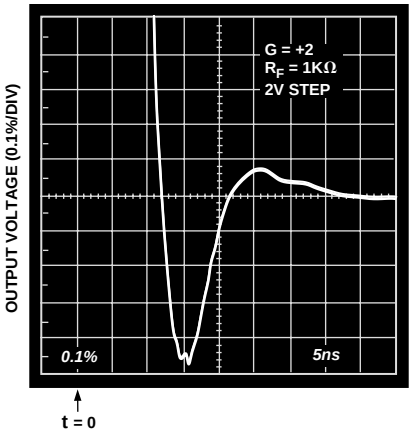
TPC 13. Frequency Response; G = +1, +2, +10; V_S = +5 V or ±5 V



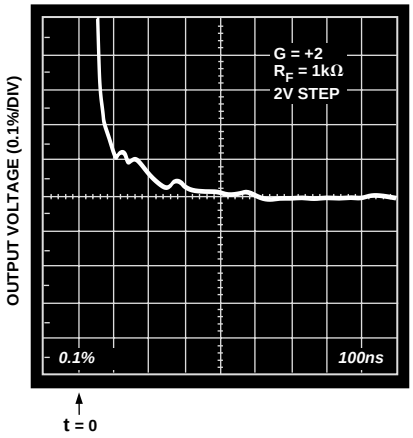
TPC 14. Frequency Response; G = –1, –10; V_S = +5 V or ±5 V



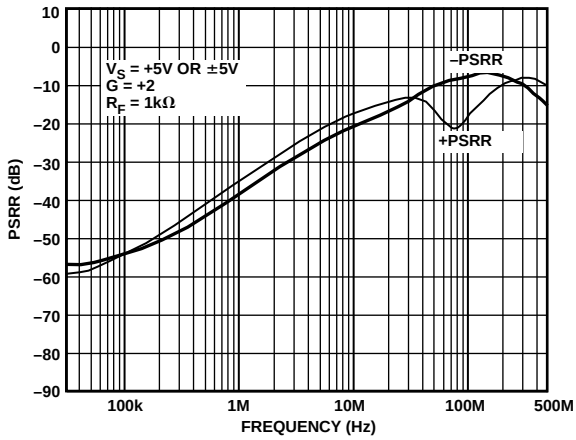
TPC 15. CMRR vs. Frequency; V_S = +5 V or ±5 V



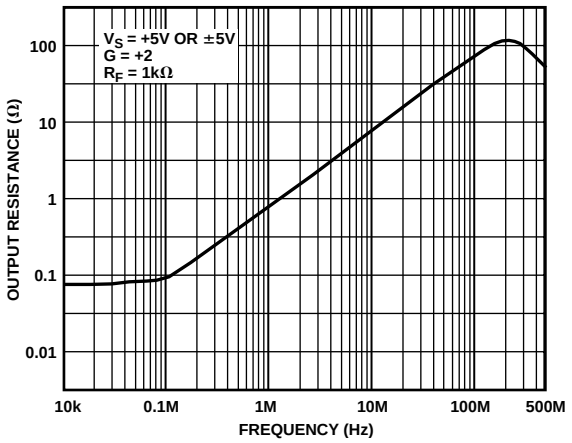
TPC 16. Short-Term Settling Time; V_S = +5 V or ±5 V



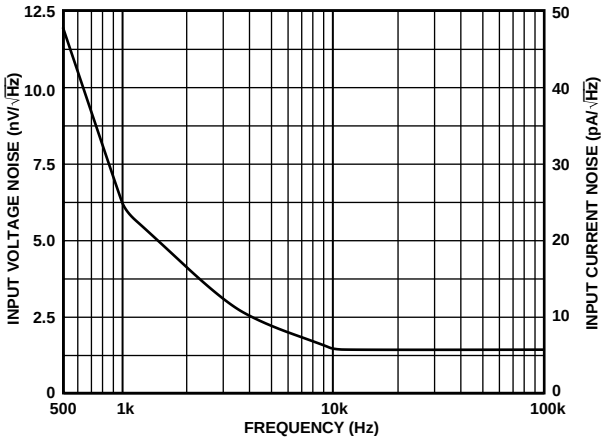
TPC 17. Long-Term Settling Time; V_S = +5 V or ±5 V



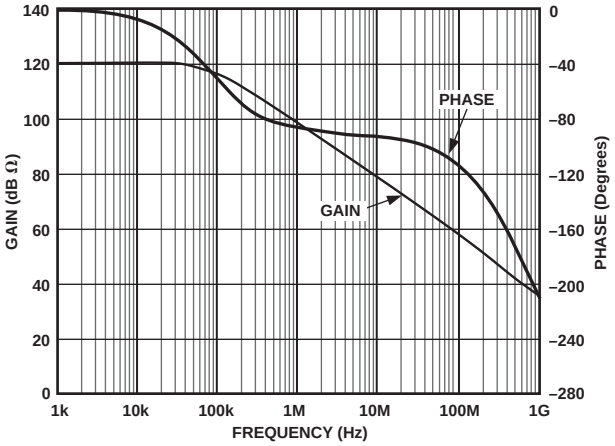
TPC 18. PSRR vs. Frequency; V_S = +5 V or ±5 V



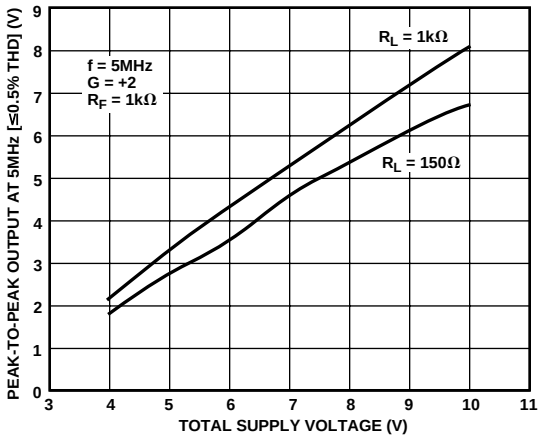
TPC 19. Output Resistance vs. Frequency; V_S = +5 V or ±5 V



TPC 21. Noise vs. Frequency; V_S = +5 V or ±5 V



TPC 20. Transimpedance Gain and Phase vs. Frequency



TPC 22. Output Swing vs. Supply

THEORY OF OPERATION

The AD8011 is a revolutionary generic high speed CF amplifier that attains new levels of BW, power, distortion, and signal swing capability. If these key parameters were combined as a figure of ac merit performance or [(frequency × V_{SIG})/(distortion × power)], no IC amplifier today would come close to the merit value of the AD8011 for frequencies above a few MHz. Its wide dynamic performance (including noise) is the result of both a new complementary high speed bipolar process and a new and unique architectural design. The AD8011 uses basically a two gain stage complementary design approach versus the traditional "single stage" complementary mirror structure sometimes referred to as the Nelson amplifier. Though twin stages have been tried before, they typically consumed high power since they were of a folded cascade design much like the AD9617. This design allows for the standing or quiescent current to add to the high signal or slew current induced stages much like the Nelson or single-stage design. Thus, in the time domain, the large signal output rise/fall time and slew rate is controlled typically by the small signal BW of the amplifier and the input signal step amplitude respectively, not the dc quiescent current of the gain stages (with the exception of input level shift diodes Q1/Q2). Using two stages versus one also allows for a higher overall gain bandwidth product (GBWP) for the same power, thus lower signal distortion and the ability to drive heavier external loads. In addition, the second gain stage also isolates (divides down) A3's input reflected load drive and the nonlinearities created resulting in relatively lower distortion and higher open-loop gain.

Overall, when *high* external load drive and low ac distortion is a requirement, a twin gain stage integrating amplifier like the AD8011 will provide superior results for lower power over the traditional single-stage complementary devices. In addition, being a CF amplifier, closed-loop BW variations versus external gain variations (varying RN) will be much lower compared to a VF op amp, where the BW varies inversely with gain. Another key attribute of this amplifier is its ability to run on a single 5 V supply due in part to its wide common-mode input and output voltage range capability. For 5 V supply operation, the device obviously consumes half the quiescent power (versus 10 V supply) with little degradation in its ac and dc performance characteristics. See Specifications.

DC GAIN CHARACTERISTICS

Gain stages A1/A1B and A2/A2B combined provide negative feedforward transresistance gain (see Figure 6). Stage A3 is a unity gain buffer that provides external load isolation to A2. Each stage uses a symmetrical complementary design. (A3 is also complementary though not explicitly shown.) This is done to reduce second order signal distortion and overall quiescent power as discussed previously. In the quasi dc to low frequency region, the closed-loop gain relationship can be approximated as

$G = 1 + R_F/R_N$ noninverting operation
$G = -R_F/R_N$ inverting operation

These basic relationships are common to all traditional operational amplifiers. Due to the inverting input error current (I_E) required to servo the output and the inverting $I_E \times R_I$ drop

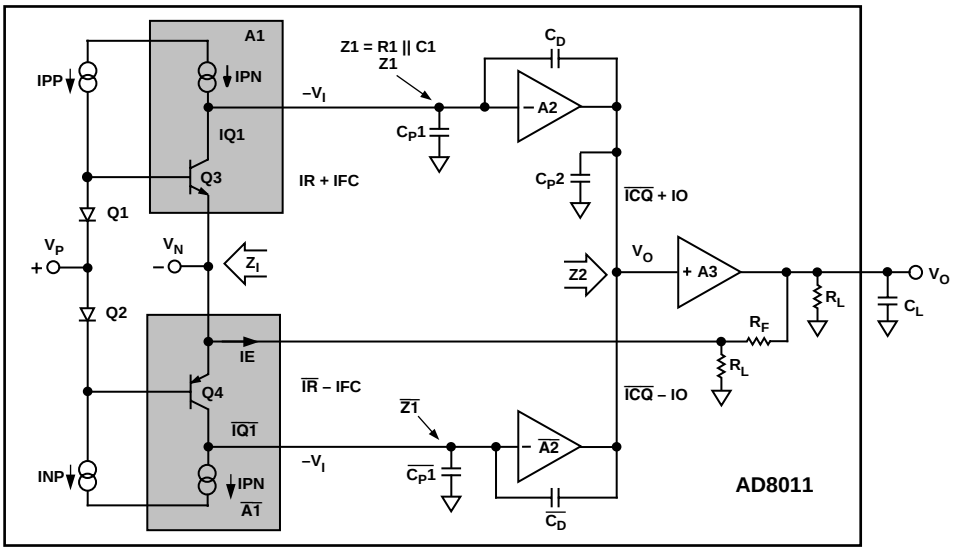


Figure 6. Simplified Block Diagram

(error current times the open-loop inverting input resistance) that results (see Figure 7), a more exact low frequency closed-loop transfer function can be described as

$$A_V = \frac{G}{1 + \frac{G \times R_I}{T_O} + \frac{R_F}{T_O}} = \frac{G}{1 + \frac{G}{A_O} + \frac{R_F}{T_O}}$$

for noninverting (G is positive).

$$A_V = \frac{G}{1 + \frac{1-G}{A_O} + \frac{R_F}{T_O}}$$

for inverting (G is negative).

where G is the ideal gain as previously described. With $R_I = T_O/A_O$ (open-loop inverting input resistance), the second expression (positive G) clearly relates to the classical voltage feedback *op amp* equation with T_O omitted due to its relatively much higher value and thus insignificant effect. A_O and T_O are the open-loop dc voltage and transresistance gains of the amplifier, respectively. These key transfer variables can be described as

$$A_O = \frac{R1 \times g_{mf} \times |A2|}{(1 - g_{mc} \times R1)}$$

and

$$T_O = \frac{R1 \times |A2|}{2}$$

Therefore

$$R_I = \frac{1 - g_{mc} \times R1}{2 \times g_{mf}}$$

where g_{mc} is the positive feedback transconductance (not shown) and $1/g_{mf}$ is the thermal emitter resistance of devices D1/D2 and Q3/Q4. The $g_{mc} \times R1$ product has a design value that results in a negative dc open-loop gain of typically –2500 V/V (see Figure 8).

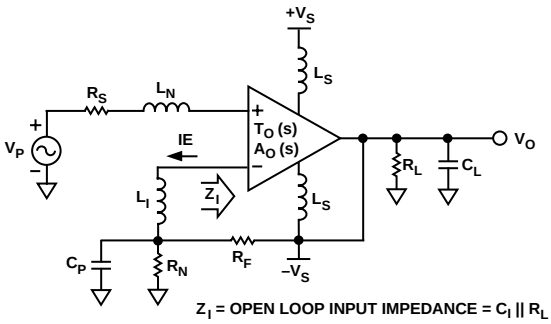


Figure 7. Z_I = Open-Loop Input Impedance

Though atypical of conventional CF or VF amps, this negative open-loop voltage gain results in an input referred error term (V_P–V_O/G = G/A_O + R_F/T_O) that will typically be negative for G, greater than +3/–4. As an example, for G = 10, A_O = –2500, and T_O = 1.2 MΩ, results in an error of –3 mV using the A_V derivation above.

This analysis assumes perfect current sources and infinite transistor V_As. (Q3, Q4 output conductances are assumed zero.) These assumptions result in actual versus model open-loop voltage gain and associated input referred error terms being less accurate for low gain (G) noninverting operation at the frequencies below the open-loop pole of the AD8011. This is primarily a result of the input signal (V_P) modulating the output conductances of Q3/Q4, resulting in R_I less negative than derived here. For inverting operation, the actual versus model dc error terms are relatively much less.

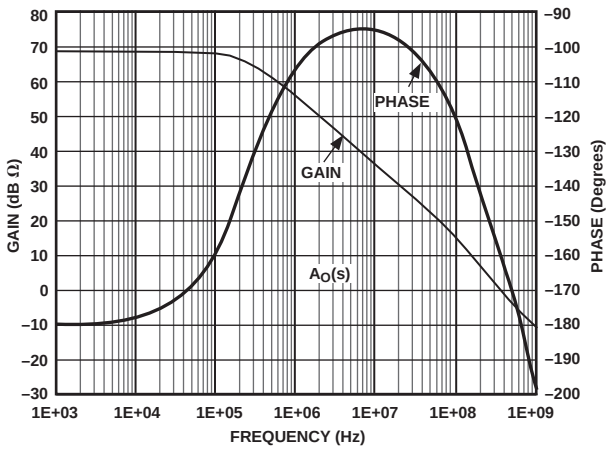


Figure 8. Open-Loop Voltage Gain and Phase

AC TRANSFER CHARACTERISTICS

The ac small signal transfer derivations below are based on a simplified single-pole model. Though inaccurate at frequencies approaching the closed-loop BW (CLBW) of the AD8011 at low noninverting external gains, they still provide a fair approximation and an intuitive understanding of its primary ac small signal characteristics.

For inverting operation and high noninverting gains, these transfer equations provide a good approximation to the actual ac performance of the device.

To accurately quantify the V_O versus V_P relationship, $A_O(s)$ and $T_O(s)$ need to be derived. This can be seen by the following nonexpanded noninverting gain relationship

$$V_O(s) / V_P(s) = \frac{G}{\frac{G}{A_O[s]} + \frac{R_F}{T_O[s]} + 1}$$

with

$$A_O(s) = \frac{R1 \times g_{mf} \times |A2|}{\frac{1 - g_{mc} \times R1}{S\tau 1}}$$

$$1 - g_{mc} \times R1$$

where R1 is the input resistance to A2/A2B, and τ1 (equal to CD × R1 × A2) is the open-loop dominate time constant,

and

$$T_O(s) = \frac{|A2| \times R1}{\frac{2}{s\tau 1 + 1}}$$

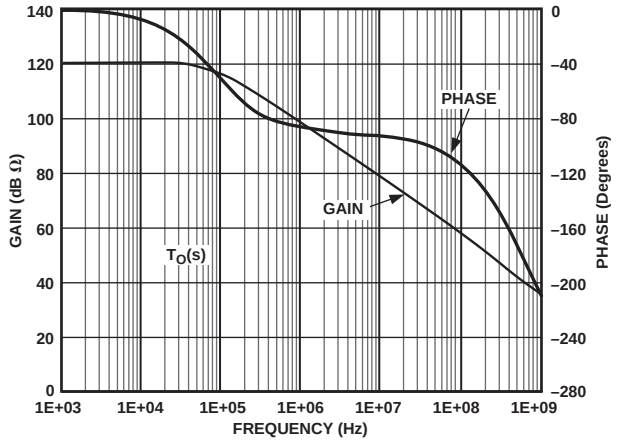


Figure 9. Open-Loop Transimpedance Gain

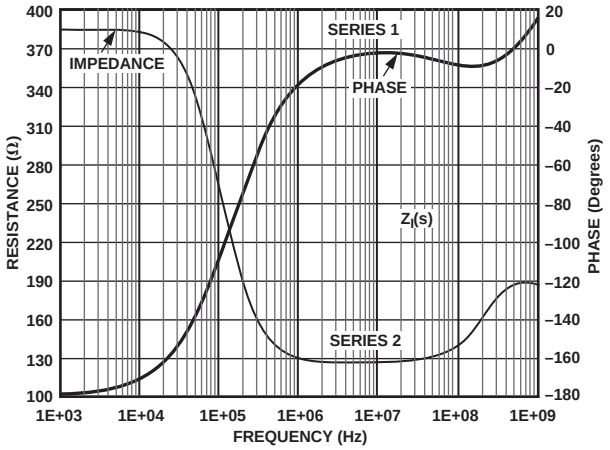


Figure 10. Open-Loop Inverting Input Impedance

Note that the ac open-loop plots in Figures 8, 9, and 10 are based on the full SPICE AD8011 simulations and do not include external parasitics (see equations below). Nevertheless, these ac loop equations still provide a good approximation to simulated and actual performance up to the CLBW of the amplifier. Typically, $g_{mc} \times R1$ is –4, resulting in $A_O(s)$ having a right half plane pole. In the time domain (inverse Laplace of A_O), it appears as unstable, causing V_O to exponentially rail out of its linear region. When the loop is closed however, the BW is greatly extended and the transimpedance gain, $T_O(s)$, *overrides* and directly controls the amplifiers stability behavior due to Z_I approaching $1/2\ g_{mf}$ for $s >> 1/\tau 1$ (see Figure 10). This can be seen by the $Z_I(s)$ and $A_V(s)$ noninverting transfer equations below.

$$Z_I(s) = \frac{(1 - g_{mc} \times R1)\left[\frac{S\tau 1}{1 - g_{mc} \times R1} + 1\right]}{2 \times g_{mf}\,(S\tau 1 + 1)}$$

$$A_V(s) = \frac{G}{\left[1 + \frac{G}{A_O} + \frac{R_F}{T_O}\right]\left[S\tau 1\left(\frac{G}{2\,g_{mf}\,T_O} + \frac{R_F}{T_O}\right) + 1\right]}$$

$Z_I(s)$ goes positive real and approaches $1/2\ g_{mf}$ as ω approaches $(g_{mc} \lfloor R1 - 1)/\tau 1$. This results in the input resistance for the $A_V(s)$ complex term being $1/2\ g_{mf}$, the parallel thermal emitter resistances of Q3/Q4. Using the computed CLBW from $A_V(s)$ and the nominal design values for the other parameters, results in a closed-loop 3 dB BW equal to the open-loop corner frequency $(1/2\ \pi\tau 1) \times 1/[G/(2\ g_{mf} \times T_O) + R_F/T_O]$. For a fixed R_F, the 3 dB BW is controlled by the R_F/T_O term for low gains and $G/(2\ g_{mf} \times T_O)$ for high gains. For example, using nominal design parameters and R_1 = 1 kΩ (which results in a nominal T_O of 1.2 MΩ), the computed BW is 80 MHz for G = 0 (inverting I-V mode with R_N removed) and 40 MHz for G = +10/–9.

DRIVING CAPACITIVE LOADS

The AD8011 was designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, the best settling response is obtained by the addition of a small series resistance as shown in Figure 11. The accompanying graph shows the optimum value for R_{SERIES} versus capacitive load. It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of R_{SERIES} and C_L.

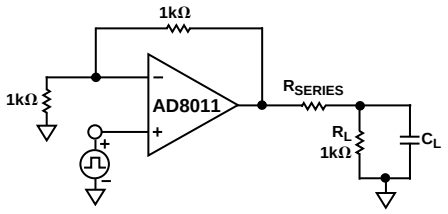


Figure 11. Driving Capacitive Load

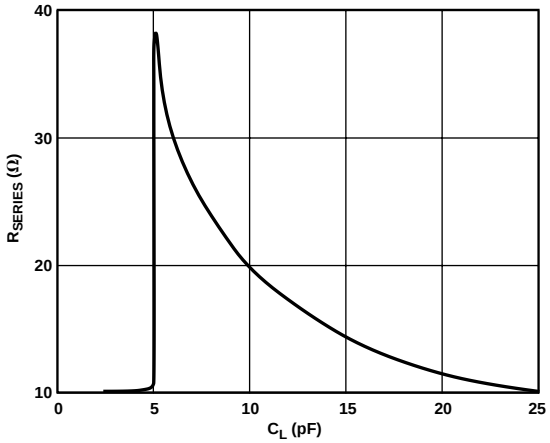


Figure 12. Recommended R_{SERIES} vs. Capacitive Load for ≤ 30 ns Settling to 0.1%

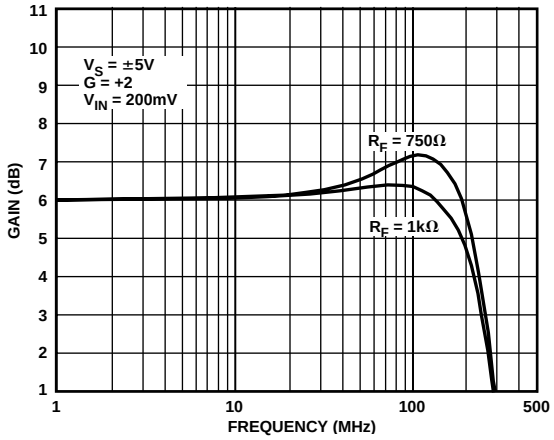


Figure 13. Flatness vs. Feedback

OPTIMIZING FLATNESS

As mentioned, the previous ac transfer equations are based on a simplified single-pole model. Due to the device's internal parasitics (primarily C_P1/C_P1B and C_P2 in Figure 6) and external package/board parasites (partially represented in Figure 12) the computed BW, using the previous V_O (s) equation, typically will be lower than the AD8011's measured small signal BW. See data sheet Bode plots.

With only internal parasitics included, the BW is extended due to the complex pole pairs created primarily by C_P1/C_P2B and C_P2 versus the single-pole assumption shown above. This results in a *design controlled*, closed-loop damping factor (ζ) of nominally 0.6 resulting in the CLBW increasing by approximately 1.3× higher than the computed single-pole value above *for optimized external gains of +2/–1*. As external noninverting gain (G) is increased, the actual closed-loop bandwidth versus the computed single-pole ac response is in closer agreement.

Inverting pin and external component capacitance (designated C_P) will further extend the CLBW due to the closed-loop zero created by C_P and $R_N \| R_F$ when operating in the noninverting mode. Using proper R_F component and layout techniques (see the Layout Considerations section), this capacitance should be about 1.5 pF. This results in a further incremental BW increase of almost 2× (versus the computed value) for G = +1 decreasing and approaching its complex pole pair BW for gains approaching +6 or higher. As previously discussed, the single-pole response begins to correlate well. Note that a pole is also created by 1/2 g_{mf} and C_P, which prevents the AD8011 from becoming unstable. This parasitic has the greatest effect on BW and peaking for low positive gains as the data sheet Bode plots clearly show. For inverting operation, C_P has relatively much less effect on CLBW variation.

Output pin and external component capacitance (designated C_L) will further extend the devices BW and can also cause peaking below and above the CLBW if too high. In the time domain, poor step settling characteristics (ringing up to about 2 GHz and excessive overshoot) can result. For high C_L values greater than about 5 pF, an external series *damping* resistor is recommended. For light loads, any output capacitance will reflect on A2's output (Z2 of buffer A3) as both added capacitance near the CLBW (CLBW > f_T/B) and eventually negative resistance at much higher frequencies. These added effects are proportional to the load C. This reflected capacitance and negative resistance has the effect of both reducing A2's phase margin and causing high frequency, L × C, peaking respectively. Using an external series resistor (as previously specified) reduces these unwanted effects by creating a reflected zero to A2's output, which will reduce the peaking and eliminate ringing. For heavy resistive loads, relatively more load C would be required to cause these same effects.

High inductive parasitics, especially on the supplies and inverting/noninverting inputs, can cause modulated low level R_F ringing on the output in the transient domain. Proper R_F component and board layout practices need to be observed. Relatively high parasitic lead inductance (roughly L >15 nh) can result in L × C underdamped ringing. Here L/C means all associated input pins, external components, and lead frame strays, including collector to substrate device capacitance. In the ac domain, this L × C resonance effect would typically not appear in the pass band of the amplifier but would appear in the open-loop response at frequencies well above the CLBW of the amplifier.

INCREASING BW AT HIGH GAINS

As presented previously, for a fixed R_F (feedback gain setting resistor), the AD8011 CLBW will decrease as R_N is reduced (increased G). This effect can be minimized by simply reducing R_F and partially restoring the devices optimized BW for gains greater than +2/–1. Note that the AD8011 is ac optimized (high BW and low peaking) for A_V = +2/–1 and R_F = 1 kΩ. Using this optimized G as a reference and the previous $V_O(s)$ equations, the following relationships result: $R_F = 1k\Omega + 2 - G/2$ *gm for* $G = 1 + R_F/R_N$ (noninverting) or $R_F = 1k\Omega + G + 1/2$ *gm for* $G = -R_F/R_N$ (inverting).

Using 1/2 gm equal to 120 Ω results in a R_F of 500 Ω for G = +5/–4 and a corresponding R_N of 125 Ω. This will extend the AD8011's BW to near its optimum design value of typically 180 MHz at R_L = 1 kΩ. In general, for gains greater than +7/–6, R_F should not be reduced to values much below 400 Ω or else ac peaking can result. Using this R_F value as the lower limit will result in BW restoration near its optimized value to the upper G values specified. Gains greater than about +7/–6 will result in CLBW reduction. The derivations above are just approximations.

DRIVING A SINGLE-SUPPLY A/D CONVERTER

New CMOS A/D converters are placing greater demands on the amplifiers that drive them. Higher re solutions, faster conversion rates, and input switching irregularities require superior settling characteristics. In addition, these devices run off a single 5 V supply and consume little power, so good single-supply operation with low power consumption are very important. The AD8011 is well positioned for driving this new class of A/D converters.

Figure 14 shows a circuit that uses an AD8011 to drive an AD876, a single-supply, 10-bit, 20 MSPS A/D converter that requires only 140 mW. Using the AD8011 for level shifting and driving, the A/D exhibits no degradation in performance compared to when it is driven from a signal generator.

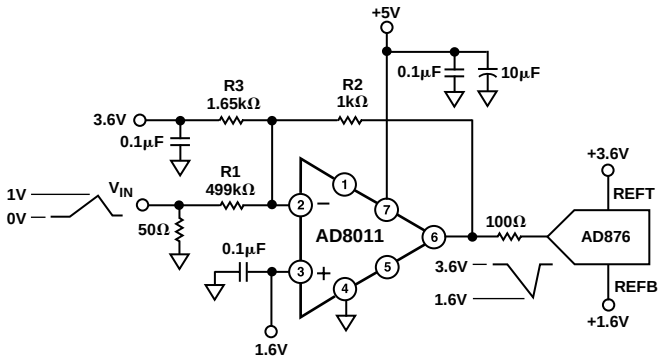


Figure 14. AD8011 Driving the AD876

The analog input of the AD876 spans 2 V centered at about 2.6 V. The resistor network and bias voltages provide the level shifting and gain required to convert the 0 V to 1 V input signal to a 3.6 V to 1.6 V range that the AD876 wants to see.

Biasing the noninverting input of the AD8011 at 1.6 V dc forces the inverting input to be at 1.6 V dc for linear operation of the amplifier. When the input is at 0 V, there is 3.2 mA flowing out of the summing junction via R1 (1.6 V/499 Ω). R3 has a current of 1.2 mA flowing into the summing junction (3.6 V – 1.6 V)/1.65 kΩ. The difference of these two currents (2 mA) must flow through R2. This current flows toward the summing junction and requires that the output be 2 V higher than the summing junction or at 3.6 V.

When the input is at 1 V, there is 1.2 mA flowing into the summing junction through R3 and 1.2 mA flowing out through R1. These currents balance and leave no current to flow through R2. Thus, the output is at the same potential as the inverting input or 1.6 V.

The input of the AD876 has a series MOSFET switch that turns on and off at the sampling rate. This MOSFET is connected to a hold capacitor, internal to the device. The on impedance of the MOSFET is about 50 Ω, while the hold capacitor is about 5 pF.

In a worst-case condition, the input voltage to the AD876 will change by a full-scale value (2 V) in one sampling cycle. When the input MOSFET turns on, the output of the op amp will be connected to the charged hold capacitor through the series resistance of the MOSFET. Without any other series resistance, the instantaneous current that flows would be 40 mA. This would cause settling problems for the op amp.

The series 100 Ω resistor limits the current that flows instantaneously to about 13 mA after the MOSFET turns on. This resistor cannot be made too large or the high frequency performance will be affected.

The sampling MOSFET of the AD876 is closed for only half of each cycle or for 25 ns. Approximately seven time constants are required for settling to 10 bits. The series 100 Ω resistor, the 50 Ω on resistance, and the hold capacitor create a 750 ps time constant. These values leave a comfortable margin for settling. Obtaining the same results with the op amp A/D combination as compared to driving with a signal generator indicates that the op amp is settling fast enough.

Overall, the AD8011 provides adequate buffering for the AD876 A/D converter without introducing distortion greater than that of the A/D converter by itself.

LAYOUT CONSIDERATIONS

The specified high speed performance of the AD8011 requires careful attention to board layout and component selection. Table I shows the recommended component values for the AD8011. Proper R_F design techniques and low parasitic component selection are mandatory.

Table I. Typical Bandwidth vs. Gain Setting Resistors

Gain	R_F (Ω)	R_G (Ω)	R_T (Ω)	Small Signal –3 dB BW (MHz), V_S = ±5 V
–1	1000	1000	52.3	150
–2	1000	499	54.9	130
–10	499	49.9		140
+1	1000		49.9	400
+2	1000	1000	49.9	250
+10	422	47.5	49.9	100
+6	1000	200	49.9	70
+6	500	100	49.9	170

R_T chosen for 50 Ω characteristic input impedance. R_O chosen for characteristic output impedance.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

Chip capacitors should be used for supply bypassing (see Figure 15). One end should be connected to the ground plane and the other within 1/8 in. of each power pin. An additional tantalum electrolytic capacitor (4.7 μF – 10 μF) should be connected in parallel.

The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance greater than 1.5 pF at the inverting input will significantly affect high speed performance when operating at low noninverting gains.

Stripline design techniques should be used for long signal traces (greater than about 1 in.). These should be designed with the proper system characteristic impedance and be properly terminated at each end.

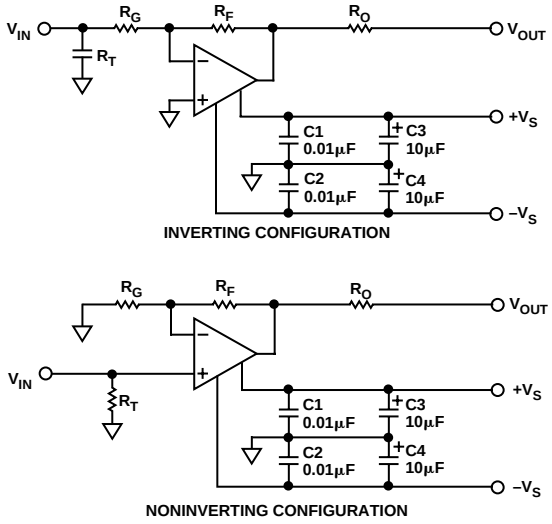
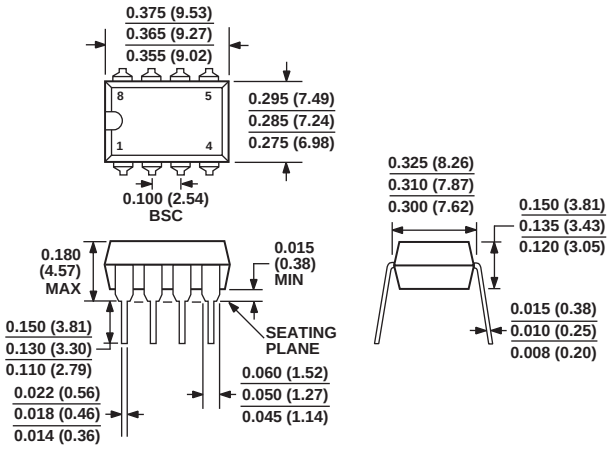


Figure 15. Inverting and Noninverting Configurations

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)

Dimensions shown in inches and (millimeters)

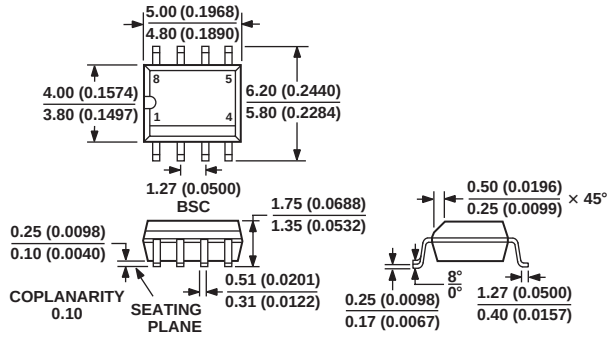


COMPLIANT TO JEDEC STANDARDS MO-095AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package [SOIC]
(R-8)

Dimensions shown in millimeters and (inches)



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Revision History

Location	Page
7/03—Data Sheet changed from REV. B to REV. C.	
Deleted all references to evaluation board	Universal
Format updated	Universal
Renumbered figures	Universal
Changes to Figure 1	1
Updated ORDERING GUIDE	4
Changes to TPC 9 and 12	6
Changes to TPC 13 and 14	7
Changes to TPC 21	8
Updated OUTLINE DIMENSIONS	16

C01048–0–7/03(C)