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8/2014—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM (AD5592R-1)

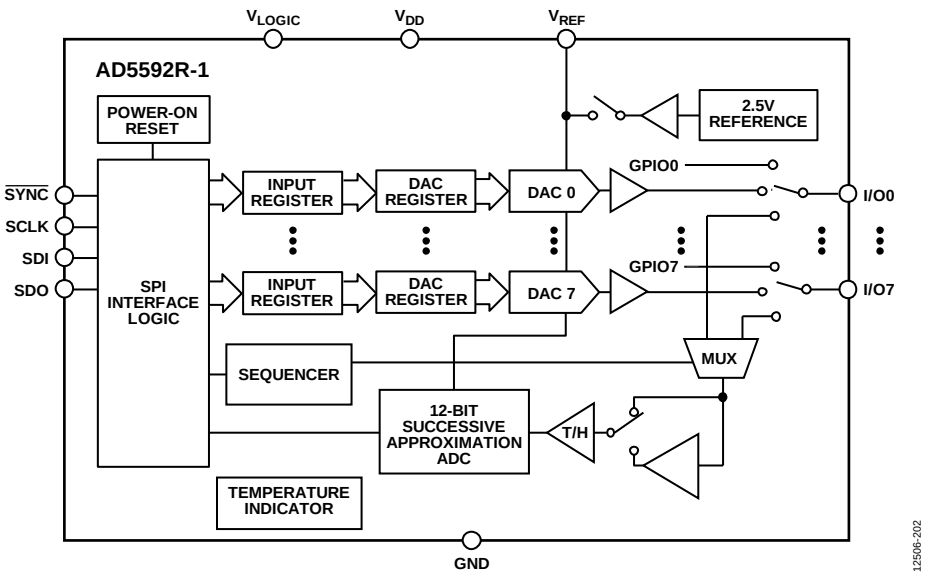


Figure 2. AD5592R-1 Functional Block Diagram

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, V_{REF} = 2.5 V (external), R_L = 2 kΩ to GND, C_L = 200 pF to GND, T_A = T_{MIN} to T_{MAX}, temperature range = −40°C to +105°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
ADC PERFORMANCE					f_{IN} = 10 kHz sine wave
Resolution		12		Bits	
Input Range	0		V_{REF}	V	When using the internal ADC buffer, there is a dead band of 0 V to 5 mV
	0		2 × V_{REF}	V	
Integral Nonlinearity (INL)	−2		+2	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	
Offset Error			±5	mV	
Gain Error			0.3	% FSR	
Throughput Rate[2]			400	kSPS	
Track Time (t_{TRACK})[2]	500			ns	
Conversion Time (t_{CONV})[2]			2	µs	
Signal-to-Noise Ratio (SNR)		69		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		67		dB	V_{DD} = 5.5 V, input range = 0 V to V_{REF}
		61		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Signal-to-Noise-and-Distortion (SINAD) Ratio		69		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		67		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		60		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Total Harmonic Distortion (THD)		−91		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		−89		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		−72		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Peak Harmonic or Spurious Noise (SFDR)		91		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		91		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		72		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Aperture Delay[2]		15		ns	V_{DD} = 3 V
		12		ns	V_{DD} = 5 V
Aperture Jitter[2]		50		ps	
Channel-to-Channel Isolation		−95		dB	f_{IN} = 5 kHz
Input Capacitance		45		pF	
Full Power Bandwidth		8.2		MHz	At 3 dB
		1.6		MHz	At 0.1 dB
DAC PERFORMANCE[3]					
Resolution		12		Bits	
Output Range	0		V_{REF}	V	
	0		2 × V_{REF}	V	
Integral Nonlinearity (INL)	−1		+1	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	
Offset Error	−3		+3	mV	
Offset Error Drift[2]		8		µV/°C	
Gain Error			±0.2	% FSR	Output range = 0 V to V_{REF}
			±0.1	% FSR	Output range = 0 V to 2 × V_{REF}
Zero Code Error		0.65	2	mV	
Total Unadjusted Error		±0.03	±0.25	% FSR	Output range = 0 V to V_{REF}
		±0.015	±0.1		Output range = 0 V to 2 × V_{REF}
Capacitive Load Stability[2]			2	nF	R_{LOAD} = ∞
			10	nF	R_{LOAD} = 1 kΩ
Resistive Load	1			kΩ	
Short-Circuit Current		25		mA	

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
DC Crosstalk[2]	−4		+4	µV	Due to single channel, full-scale output change
DC Output Impedance		0.2		Ω	
DC Power Supply Rejection Ratio (PSRR)[2]		0.15		mV/V	DAC code = midscale, V_{DD} = 3 V ± 10% or 5 V ± 10%
Load Impedance at Rails[4]		25		Ω	
Load Regulation		200		µV/mA	V_{DD} = 5 V ± 10%, DAC code = midscale, −10 mA ≤ I_{OUT} ≤ +10 mA
		200		µV/mA	V_{DD} = 3 V ± 10%, DAC code = midscale, −10 mA ≤ I_{OUT} ≤ +10 mA
Power-Up Time		7		µs	Coming out of power-down mode, V_{DD} = 5 V
AC SPECIFICATIONS					
Slew Rate		1.25		V/µs	Measured from 10% to 90% of full scale
Settling Time		6		µs	¼ scale to ¾ scale settling to 1 LSB
DAC Glitch Impulse		2		nV-sec	
DAC to DAC Crosstalk		1		nV-sec	
Digital Crosstalk		0.1		nV-sec	
Analog Crosstalk		1		nV-sec	
Digital Feedthrough		0.1		nV-sec	
Multiplying Bandwidth		240		kHz	DAC code = full scale, output range = 0 V to V_{REF}
Output Voltage Noise Spectral Density		200		nV/√Hz	DAC code = midscale, output range = 0 V to 2 × V_{REF}, measured at 10 kHz
Signal-to-Noise Ratio (SNR)		81		dB	
Peak Harmonic or Spurious Noise (SFDR)		77		dB	
Signal-to-Noise-and-Distortion (SINAD) Ratio		74		dB	
Total Harmonic Distortion (THD)		−76		dB	
REFERENCE INPUT					
V_{REF} Input Voltage	1		V_{DD}	V	
DC Leakage Current	−1		+1	µA	No I/Ox pins configured as DACs
Reference Input Impedance		12		kΩ	DAC output range = 0 V to 2 × V_{REF}
		24		kΩ	DAC output range = 0 V to V_{REF}
REFERENCE OUTPUT					
V_{REF} Output Voltage	2.495	2.5	2.505	V	At ambient
V_{REF} Temperature Coefficient		20		ppm/°C	
Capacitive Load Stability		5		µF	R_L = 2 kΩ
Output Impedance[2]		0.15		Ω	V_{DD} = 2.7 V
		0.7		Ω	V_{DD} = 5 V
Output Voltage Noise		10		µV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density		240		nV/√Hz	At ambient, f = 10 kHz, C_L = 10 nF
Line Regulation		20		µV/V	At ambient, sweeping V_{DD} from 2.7 V to 5.5 V
		10		µV/V	At ambient, sweeping V_{DD} from 2.7 V to 3.3 V
Load Regulation					
Sourcing		210		µV/mA	At ambient, −5 mA ≤ load current ≤ +5 mA
Sinking		120		µV/mA	At ambient, −5 mA ≤ load current ≤ +5 mA
Output Current Load Capability		±5		mA	V_{DD} ≥ 3 V
GPIO OUTPUT					
I_{SOURCE}, I_{SINK}		1.6		mA	
Output Voltage					
High (V_{OH})	V_{DD} − 0.2			V	I_{SOURCE} = 1 mA
Low (V_{OL})			0.4	V	I_{SOURCE} = 1 mA

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
GPIO INPUT					
Input Voltage					
High (V_{IH})	$0.7 \times V_{DD}$			V	
Low (V_{IL})			$0.3 \times V_{DD}$	V	
Input Capacitance		20		pF	
Hysteresis		0.2		V	
Input Current		±1		µA	
LOGIC INPUTS					
AD5592R Input Voltage					
High (V_{INH})	$0.7 \times V_{DD}$			V	
Low (V_{INL})			$0.3 \times V_{DD}$	V	
AD5592R-1 Input Voltage					
High (V_{INH})	$0.7 \times V_{LOGIC}$			V	
Low (V_{INL})			$0.3 \times V_{LOGIC}$	V	
Input Current (I_{IN})	−1		+1	µA	Typically 10 nA, $\overline{RESET}$ = 1 µA typical
Input Capacitance (C_{IN})			10	pF	
LOGIC OUTPUT (SDO)					
Output High Voltage (V_{OH})					
AD5592R	$V_{DD} - 0.2$			V	I_{SOURCE} = 200 µA, V_{DD} = 2.7 V to 5. 5 V
AD5592R-1	$V_{LOGIC} - 0.2$			V	I_{SOURCE} = 200 µA, V_{DD} = 2.7 V to 5. 5 V
Output Low Voltage (V_{OL})			0.4	V	I_{SINK} = 200 µA
Floating-State Output Capacitance		10		pF	
TEMPERATURE SENSOR[2]					
Resolution		12		Bits	
Operating Range	−40		+105	°C	
Accuracy		±3		°C	5 sample averaging
Track Time			5	µs	ADC buffer enabled
			20	µs	ADC buffer disabled
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD}			2.7	mA	Digital inputs = 0 V or V_{DD}, I/O0 to I/O7 configured as DACs and ADCs, internal reference on, ADC buffer on, DAC code = 0xFFF, range is 0 V to 2 × V_{REF} for DACs and ADCs
Power-Down Mode			3.5	µA	
V_{DD} = 5 V (Normal Mode)		1.6		mA	I/O0 to I/O7 are DACs, internal reference, gain = 2
		1		mA	I/O0 to I/O7 are DACs, external reference, gain = 2
		2.4		mA	I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 2
		1.1		mA	I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 2
		1		mA	I/O0 to I/O7 are ADCs, internal reference, gain = 2
		0.75		mA	I/O0 to I/O7 are ADCs, external reference, gain = 2
		0.5		mA	I/O0 to I/O7 are general-purpose outputs
		0.5		mA	I/O0 to I/O7 are general-purpose inputs
		0.5		mA	I/O0 to I/O3 are general-purpose outputs, I/O4 to I/O7 are general-purpose inputs

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
V_{DD} = 3 V (Normal Mode)		1.1		mA	I/O0 to I/O7 are DACs, internal reference, gain = 1
		1		mA	I/O0 to I/O7 are DACs, external reference, gain = 1
		1.1		mA	I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 1
		0.78		mA	I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 1
		0.75		mA	I/O0 to I/O7 are ADCs, internal reference, gain = 1
		0.5		mA	I/O0 to I/O7 are ADCs, external reference, gain = 1
		0.45		mA	I/O0 to I/O7 are general-purpose outputs
		0.45		mA	I/O0 to I/O7 are general-purpose inputs
V_{LOGIC}	1.62		V_{DD}	V	AD5592R-1 only
I_{LOGIC}			3	µA	AD5592R-1 only

[1] All specifications expressed in decibels are referred to full-scale input (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise noted.
[2] Guaranteed by design and characterization; not production tested.
[3] DC specifications tested with the outputs unloaded, unless otherwise noted. Linearity calculated using a code range of 8 to 4095. There is an upper dead band of 10 mV when $V_{REF} = V_{DD}$.
[4] When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV (see Figure 33).

TIMING CHARACTERISTICS

Guaranteed by design and characterization, not production tested; all input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 3. AD5592R Timing Characteristics

Parameter	2.7 V ≤ V_{DD} < 3 V	3 V ≤ V_{DD} ≤ 5.5 V	Unit	Test Conditions/Comments
t_1	33	20	ns min	SCLK cycle time, write operation
	50	50	ns min	SCLK cycle time, read operation
t_2	16	10	ns min	SCLK high time
t_3	16	10	ns min	SCLK low time
t_4	15	10	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
	2	2	µs max	$\overline{SYNC}$ falling edge to SCLK falling edge setup time[1]
t_5	7	7	ns min	Data setup time
t_6	5	5	ns min	Data hold time
t_7	15	10	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	30	30	ns min	Minimum $\overline{SYNC}$ high time for register write operations
	60	60	ns min	Minimum $\overline{SYNC}$ high time for register read operations
t_9	0	0	ns min	$\overline{SYNC}$ rising edge to next SCLK falling edge
t_{10}	25	25	ns max	SCLK rising edge to SDO valid
t_{11}	250	250	ns min	$\overline{RESET}$ low pulse width (not shown in Figure 4)

[1] When reading an ADC conversion.

Table 4. AD5592R-1 Timing Characteristics

Parameter	1.62 V ≤ V_{LOGIC} < 3 V	3 V ≤ V_{LOGIC} ≤ 5.5 V	Unit	Test Conditions/Comments
t_1	33	20	ns min	SCLK cycle time, write operation
	65	50	ns min	SCLK cycle time, read operation
t_2	16	10	ns min	SCLK high time
t_3	16	10	ns min	SCLK low time
t_4	15	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
	2	2	µs max	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	7	7	ns min	Data setup time
t_6	5	5	ns min	Data hold time
t_7	15	10	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	30	30	ns min	Minimum $\overline{SYNC}$ high time for write operations
	60	60	ns min	Minimum $\overline{SYNC}$ high time for register read operations
t_9	0	0	ns min	$\overline{SYNC}$ rising edge to next SCLK falling edge
t_{10}	56	25	ns max	SCLK rising edge to SDO valid

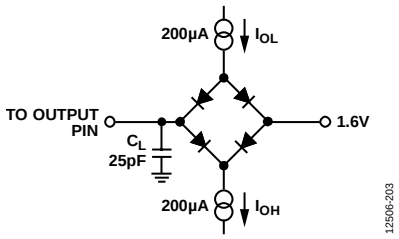


Figure 3. Load Circuit for Logic Output (SDO) Timing Specifications

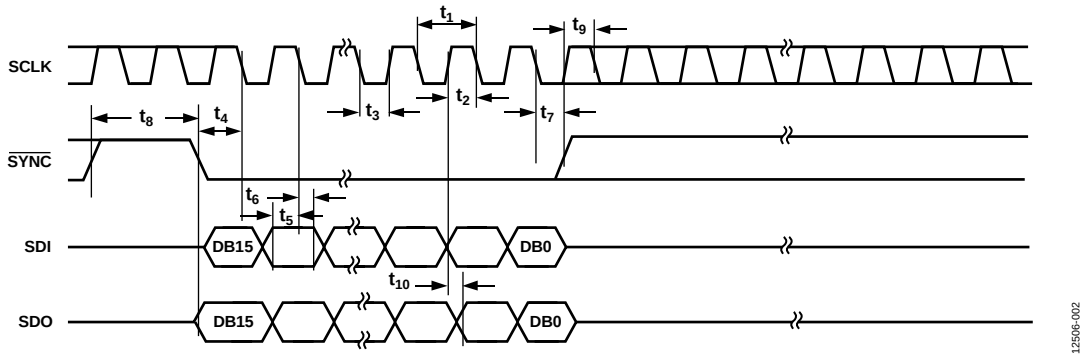


Figure 4. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to + 7 V
V_{LOGIC} to GND	−0.3 V to + 7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
AD5592R	
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
AD5592R-1	
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Ball WLCSP	60	°C/W
16-Lead LFCSP	137	°C/W
16-Lead TSSOP	112	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

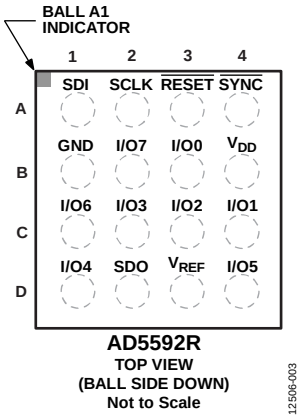


Figure 5. AD5592R 16-Ball WLCSP Pin Configuration

Table 7. AD5592R 16-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	SDI	Data In. Logic input. Data that is to be written to the DACs and control registers is provided on this input and is clocked into the register on the falling edge of SCLK.
A2	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz when writing to the DACs. SCLK has a maximum speed of 20 MHz when performing a conversion or clocking data from the AD5592R.
A3	$\overline{\text{RESET}}$	Asynchronous Reset Pin. Tie this pin high for normal operation. When this pin is brought low, the AD5592R is reset to its default configuration.
A4	$\overline{\text{SYNC}}$	Synchronization. Active low control input. $\overline{\text{SYNC}}$ is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, data is transferred in on the falling edges of the next 16 clocks.
B1	GND	Ground Reference Point for All Circuitry on the AD5592R.
B2	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. The function of this pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16). I/O7 can also be configured as a $\overline{\text{BUSY}}$ signal to indicate when an ADC conversion is taking place (see Table 30 and Table 31).
B3, C4, C3, C2, D1, D4, C1	I/O0 to I/O6	Input/Output 0 Through Input/Output 6. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16).
B4	V_{DD}	Power Supply Input. The AD5592R operates from 2.7 V to 5.5 V, and this pin must be decoupled with a 0.1 µF capacitor to GND.
D2	SDO	Data Out. Logic output. The conversion results from the ADC, register reads, and temperature sensor information are provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The MSB is placed on the SDO pin on the falling edge of $\overline{\text{SYNC}}$. Because the SCLK can idle high or low, the next bit is clocked out on the first rising edge of SCLK that follows a falling edge SCLK while $\overline{\text{SYNC}}$ is low (see Figure 4).
D3	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on this pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5592R. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.

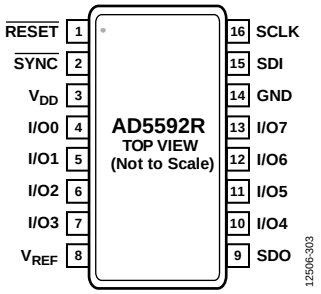


Figure 6. AD5592R 16-Lead TSSOP Pin Configuration

Table 8. AD5592R 16-Lead TSSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
15	SDI	Data In. Logic input. Data that is to be written to the DACs and control registers is provided on this input and is clocked into the register on the falling edge of SCLK.
16	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz when writing to the DACs. SCLK has a maximum speed of 20 MHz when performing a conversion or clocking data from the AD5592R.
1	$\overline{\text{RESET}}$	Asynchronous Reset Pin. Tie this pin high for normal operation. When this pin is brought low, the AD5592R is reset to its default configuration.
2	$\overline{\text{SYNC}}$	Synchronization. Active low control input. $\overline{\text{SYNC}}$ is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, data is transferred in on the falling edges of the next 16 clocks.
14	GND	Ground Reference Point for All Circuitry on the AD5592R.
13	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. The function of this pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16). I/O7 can also be configured as a $\overline{\text{BUSY}}$ signal to indicate when an ADC conversion is taking place (see Table 30 and Table 31).
4, 5, 6, 7, 10, 11, 12	I/O0 to I/O6	Input/Output 0 Through Input/Output 6. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16).
3	V_{DD}	Power Supply Input. The AD5592R operates from 2.7 V to 5.5 V, and this pin must be decoupled with a 0.1 µF capacitor to GND.
9	SDO	Data Out. Logic output. The conversion results from the ADC, register reads, and temperature sensor information are provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The MSB is placed on the SDO pin on the falling edge of $\overline{\text{SYNC}}$. Because the SCLK can idle high or low, the next bit is clocked out on the first rising edge of SCLK that follows a falling edge SCLK while $\overline{\text{SYNC}}$ is low (see Figure 4).
8	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on this pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5592R. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.

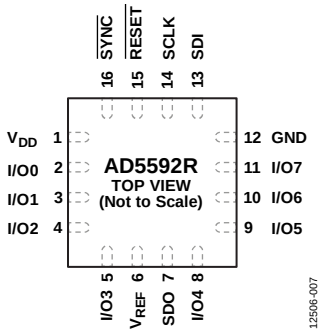


Figure 7. AD5592R 16-Lead LFCSP Pin Configuration

Table 9. AD5592R 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The AD5592R operates from 2.7 V to 5.5 V, and this pin must be decoupled with a 0.1 µF capacitor to GND.
2, 3, 4, 5, 8, 9, 10	I/O0 to I/O6	Input/Output 0 Through Input/Output 6. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16).
6	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on this pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5592R. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.
7	SDO	Data Out. Logic output. The conversion results from the ADC, register reads, and temperature sensor information are provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The MSB is placed on the SDO pin on the falling edge of $\overline{SYNC}$. Because the SCLK can idle high or low, the next bit is clocked out on the first rising edge of SCLK that follows a falling edge SCLK while $\overline{SYNC}$ is low (see Figure 4).
11	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. The function of this pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16). I/O7 can also be configured as a $\overline{BUSY}$ signal to indicate when an ADC conversion is taking place (see Table 30 and Table 31).
12	GND	Ground Reference Point for All Circuitry on the AD5592R.
13	SDI	Data In. Logic input. Data that is to be written to the DACs and control registers is provided on this input and is clocked into the register on the falling edge of SCLK.
14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz when writing to the DACs. SCLK has a maximum speed of 20 MHz when performing a conversion or clocking data from the AD5592R.
15	$\overline{RESET}$	Asynchronous Reset Pin. Tie this pin high for normal operation. When this pin is brought low, the AD5592R is reset to its default configuration.
16	$\overline{SYNC}$	Synchronization. Active low control input. $\overline{SYNC}$ is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, data is transferred in on the falling edges of the next 16 clocks.

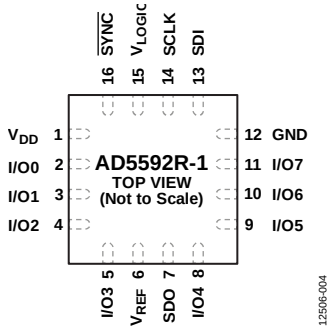


Figure 8. AD5592R-1 16-Lead LFCSP Pin Configuration

Table 10. AD5592R-1 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The AD5592R-1 operates from 2.7 V to 5.5 V, and this pin must be decoupled with a 0.1 µF capacitor to GND.
2 to 5, 8 to 10	I/O0 to I/O6	Input/Output 0 Through Input/Output 6. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16).
6	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on this pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5592R-1. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.
7	SDO	Data Out. Logic output. The conversion results from the ADC, register reads, and temperature sensor information are provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The MSB is placed on the SDO pin on the falling edge of $\overline{SYNC}$. Because the SCLK can idle high or low, the next bit is clocked out on the first rising edge of SCLK that follows a falling edge SCLK while $\overline{SYNC}$ is low (see Figure 4).
11	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. The function of this pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16). I/O7 can also be configured as a $\overline{BUSY}$ signal to indicate when an ADC conversion is taking place (see Table 30 and Table 31).
12	GND	Ground Reference Point for All Circuitry on the AD5592R-1.
13	SDI	Data In. Logic input. Data to be written to the DACs and control registers is provided on this input and is clocked into the register on the falling edge of SCLK.
14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz when writing to the DACs. SCLK has a maximum speed of 20 MHz when performing a conversion or clocking data from the AD5592R-1.
15	V_{LOGIC}	Interface Power Supply. The voltage of this pin ranges from 1.62 V to 5.5 V.
16	$\overline{SYNC}$	Synchronization. Active low control input. $\overline{SYNC}$ is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, data is transferred in on the falling edges of the next 16 clocks.

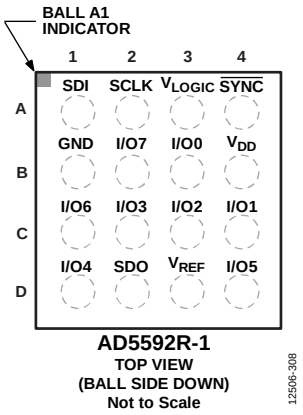


Figure 9. AD5592R-1 16-Ball WLCSP Pin Configuration

Table 11. AD5592R-1 16-Lead WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
B4	V_{DD}	Power Supply Input. The AD5592R-1 operates from 2.7 V to 5.5 V, and this pin must be decoupled with a 0.1 µF capacitor to GND.
B3, C4, C3, C2, D1, D4, C1	I/O0 to I/O6	Input/Output 0 Through Input/Output 6. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16).
D3	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on this pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5592R-1. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.
D2	SDO	Data Out. Logic output. The conversion results from the ADC, register reads, and temperature sensor information are provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The MSB is placed on the SDO pin on the falling edge of $\overline{SYNC}$. Because the SCLK can idle high or low, the next bit is clocked out on the first rising edge of SCLK that follows a falling edge SCLK while $\overline{SYNC}$ is low (see Figure 4).
B2	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. The function of this pin is determined by programming the I/Ox pin configuration registers (see Table 15 and Table 16). I/O7 can also be configured as a $\overline{BUSY}$ signal to indicate when an ADC conversion is taking place (see Table 30 and Table 31).
B1	GND	Ground Reference Point for All Circuitry on the AD5592R-1.
A1	SDI	Data In. Logic input. Data to be written to the DACs and control registers is provided on this input and is clocked into the register on the falling edge of SCLK.
A2	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz when writing to the DACs. SCLK has a maximum speed of 20 MHz when performing a conversion or clocking data from the AD5592R-1.
A3	V_{LOGIC}	Interface Power Supply. The voltage of this pin ranges from 1.62 V to 5.5 V.
A4	$\overline{SYNC}$	Synchronization. Active low control input. $\overline{SYNC}$ is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, data is transferred in on the falling edges of the next 16 clocks.

TYPICAL PERFORMANCE CHARACTERISTICS

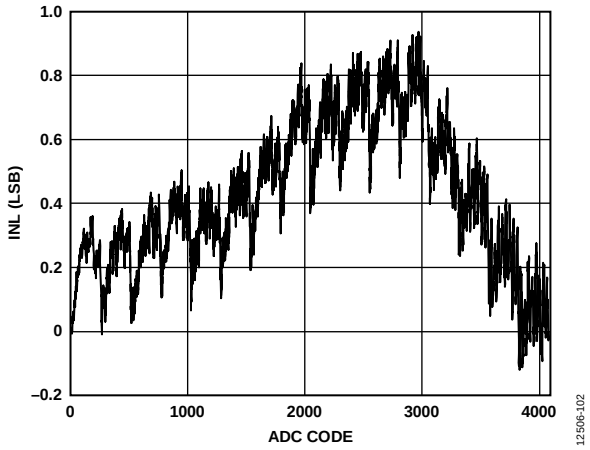


Figure 10. ADC INL, V_{DD} = 5.5 V

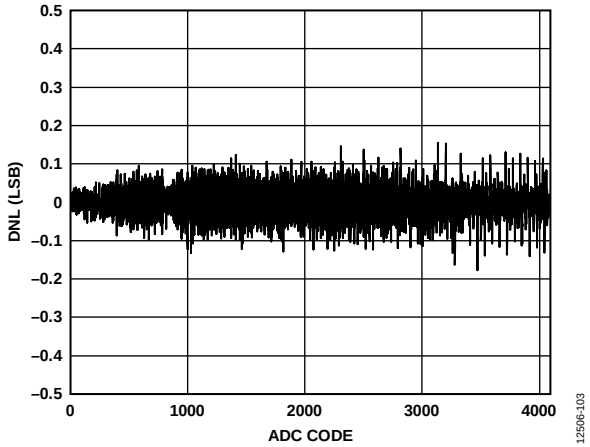


Figure 11. ADC DNL, V_{DD} = 5.5 V

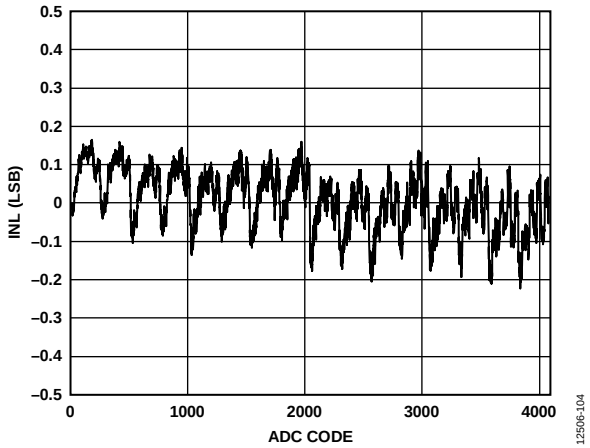


Figure 12. ADC INL, V_{DD} = 2.7 V

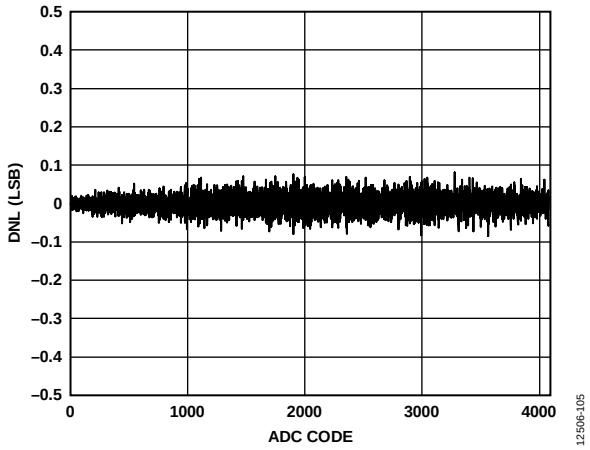


Figure 13. ADC DNL, V_{DD} = 2.7 V

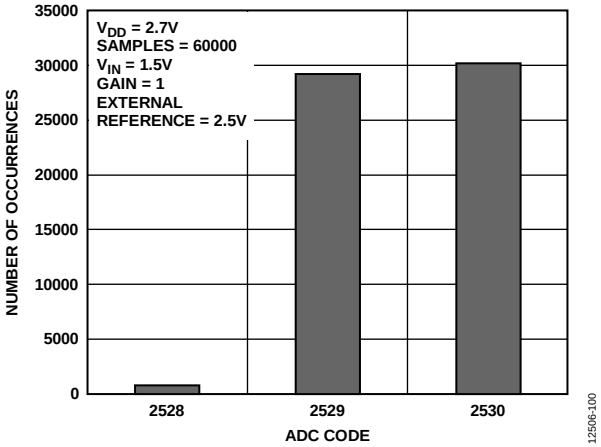


Figure 14. Histogram of ADC Codes, V_{DD} = 2.7 V

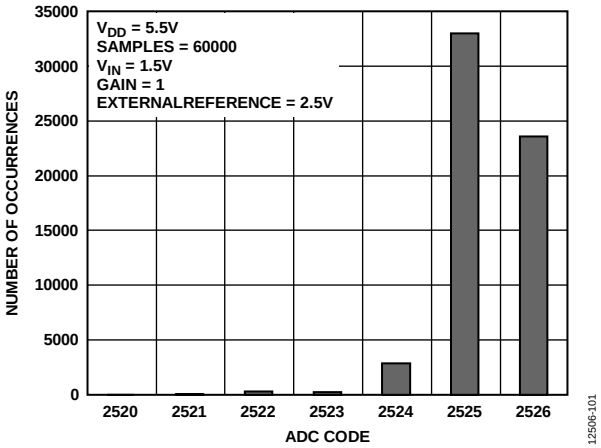


Figure 15. Histogram of ADC Codes, V_{DD} = 5.5 V

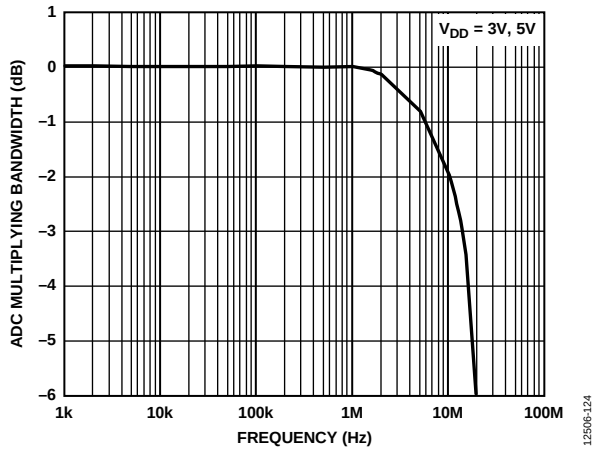


Figure 16. ADC Multiplying Bandwidth

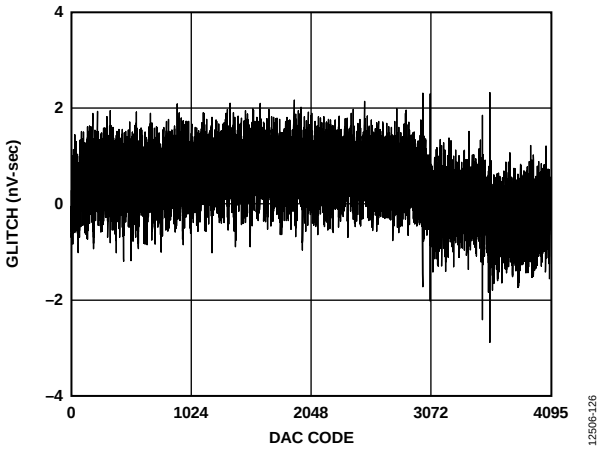


Figure 19. DAC Adjacent Code Glitch

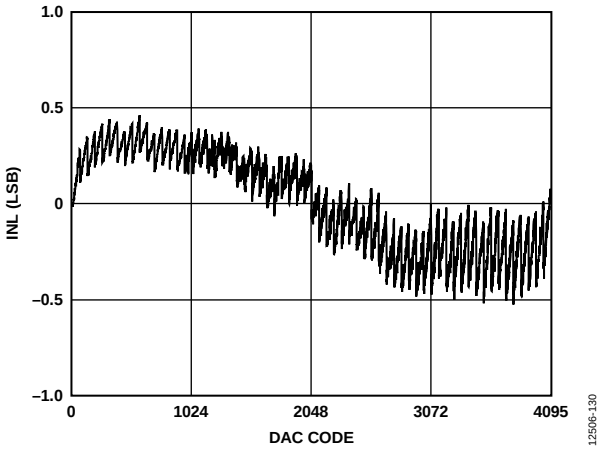


Figure 17. DAC INL

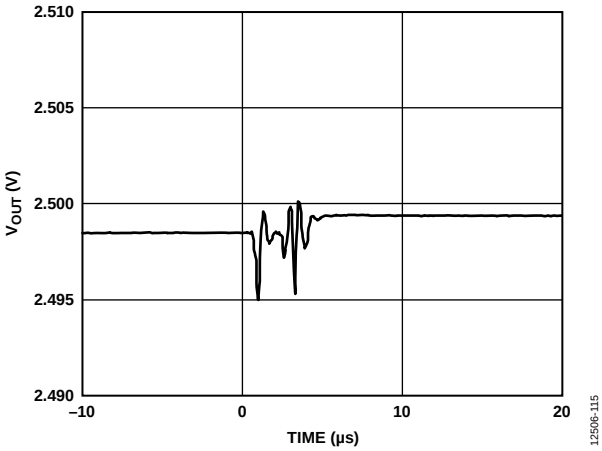


Figure 20. DAC Digital-to-Analog Glitch (Rising)

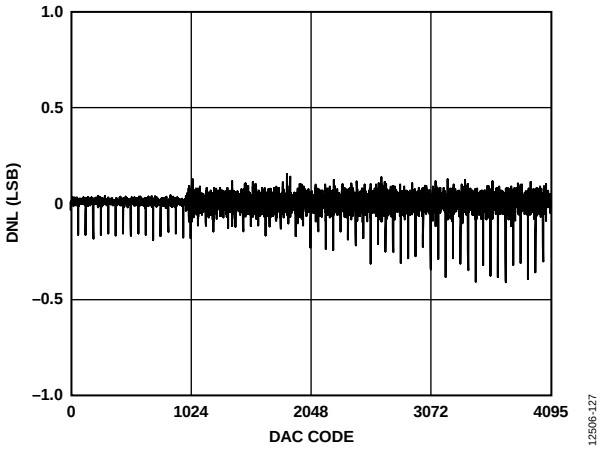


Figure 18. DAC DNL

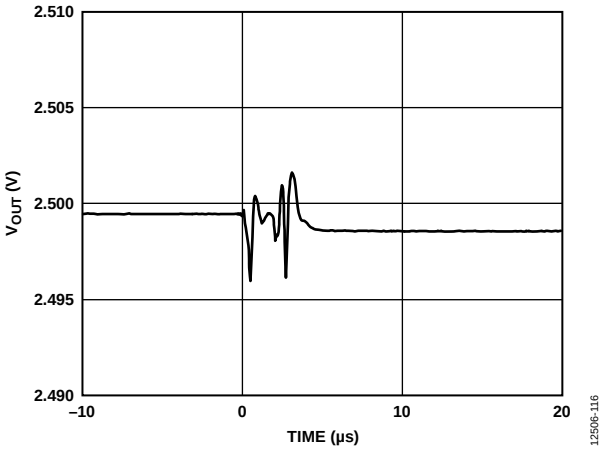


Figure 21. DAC Digital-to-Analog Glitch (Falling)

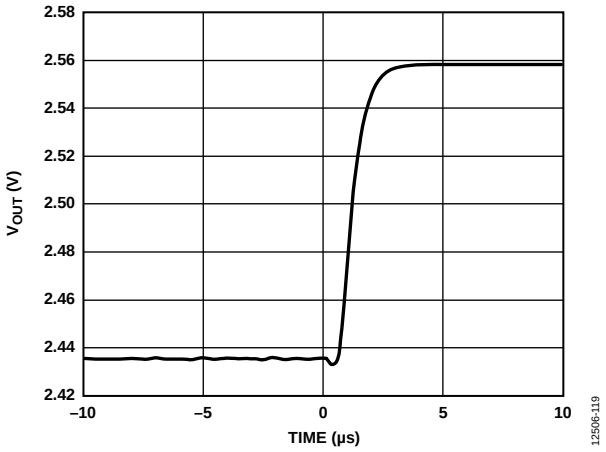


Figure 22. DAC Settling Time (100 Code Change, Rising Edge)

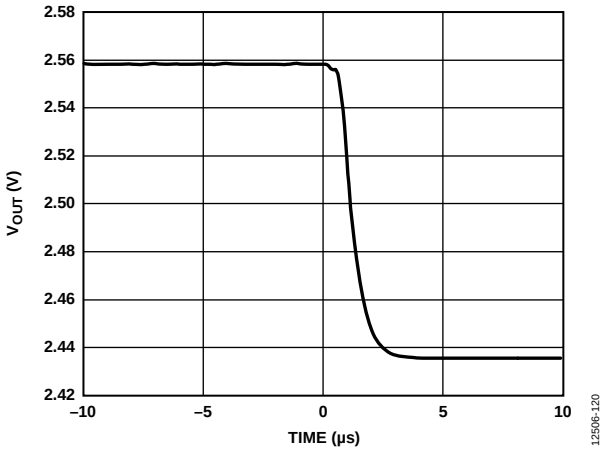


Figure 23. DAC Settling Time (100 Code Change, Falling Edge)

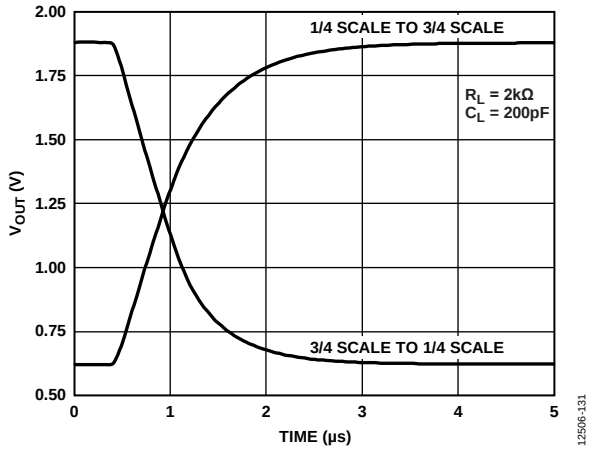


Figure 24. DAC Settling Time, Output Range = 0 V to V_{REF}

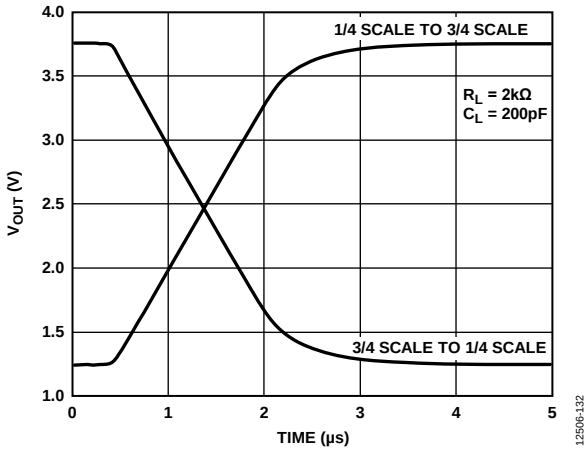


Figure 25. DAC Settling Time, Output Range = 0 V to 2 × V_{REF}

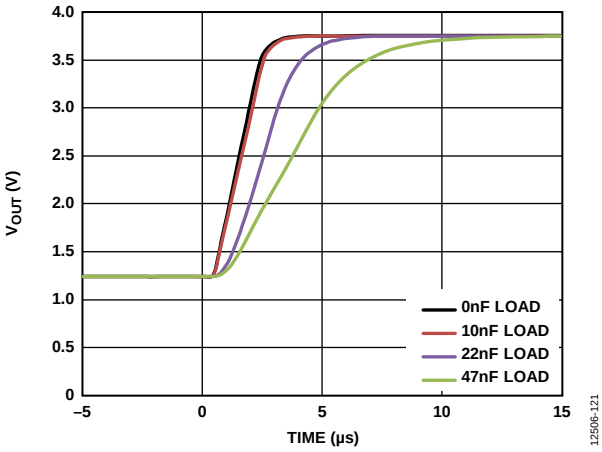


Figure 26. DAC Settling Time for Various Capacitive Loads

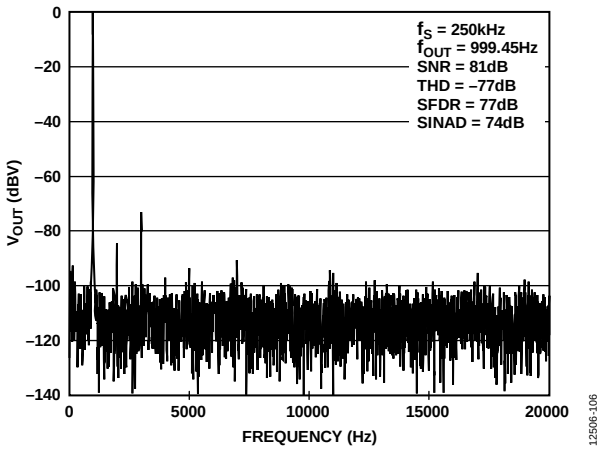


Figure 27. DAC Sine Wave Output, Output Range = 0 V to 2 × V_{REF}, Bandwidth = 0 Hz to 20 kHz

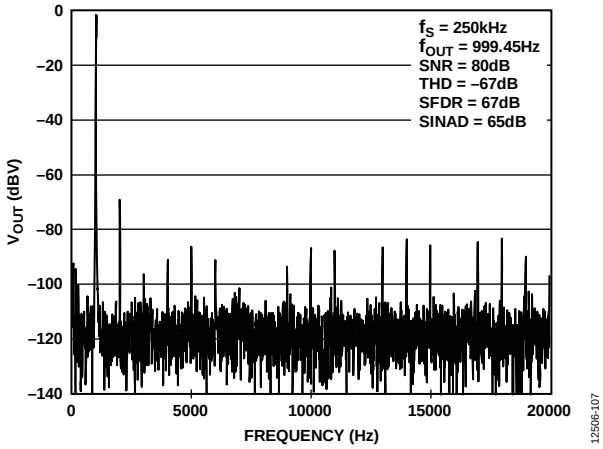


Figure 28. DAC Sine Wave Output, Output Range = 0 V to V_{REF}, Bandwidth = 0 Hz to 20 kHz

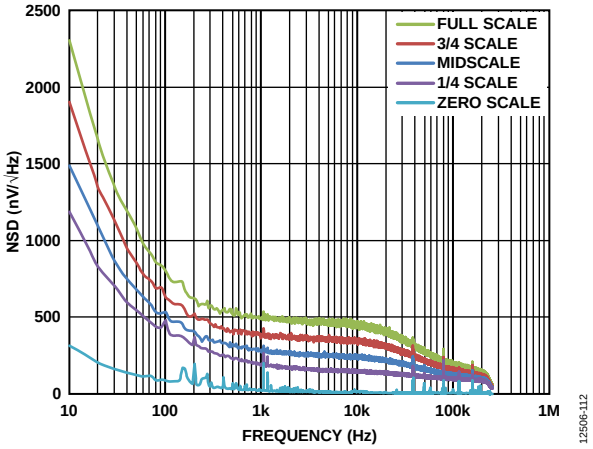


Figure 31. DAC Output Noise Spectral Density (NSD)

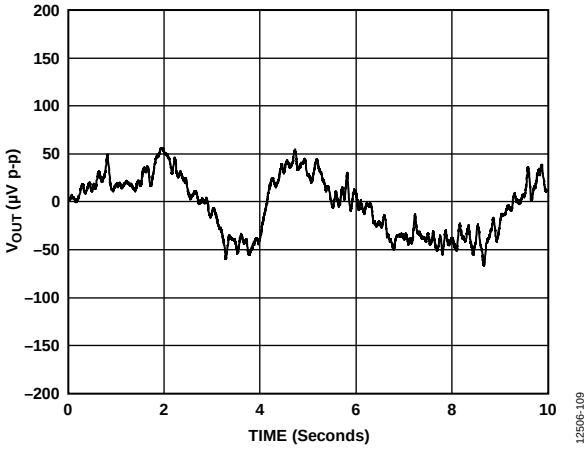


Figure 29. DAC 1/f Noise with External Reference

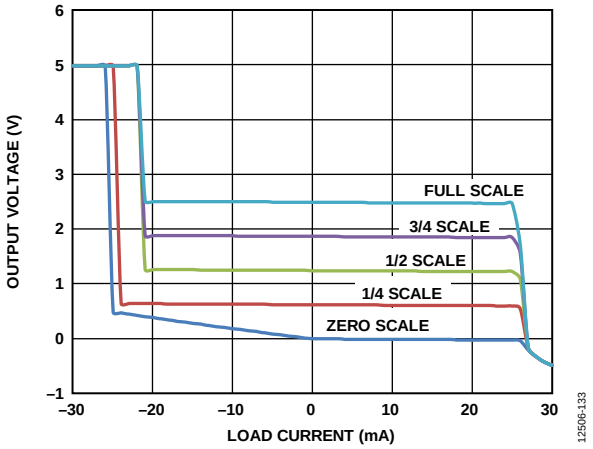


Figure 32. DAC Output Sink and Source Capability, Output Range = 0 V to V_{REF}

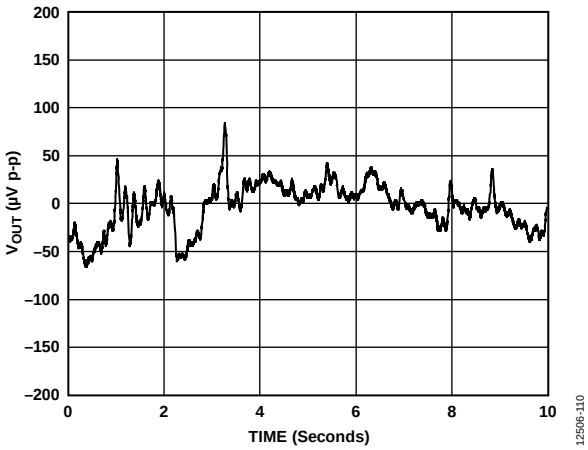


Figure 30. DAC 1/f Noise with Internal Reference

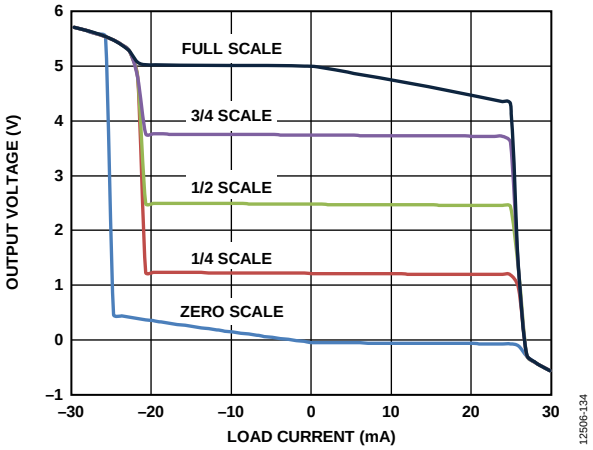


Figure 33. DAC Output Sink and Source Capability, Output Range = 0 V to 2 × V_{REF}

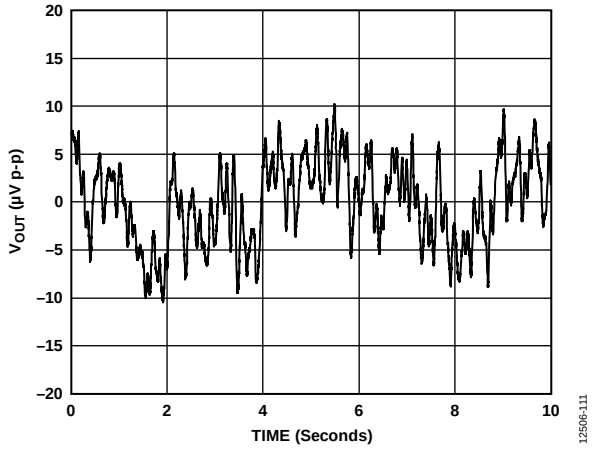


Figure 34. Internal Reference 1/f Noise

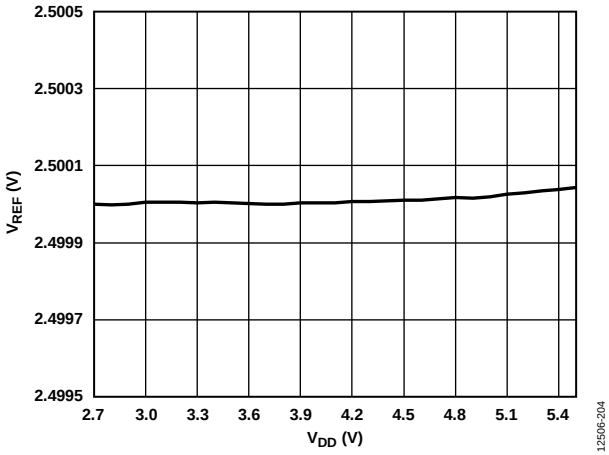


Figure 36. Reference Line Regulation

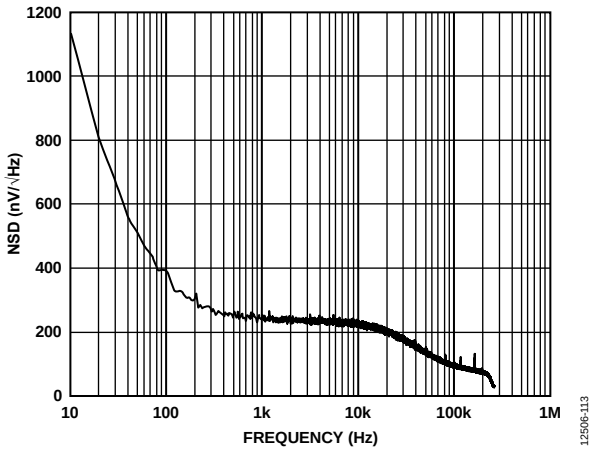


Figure 35. Reference Noise Spectral Density (NSD)

TERMINOLOGY

ADC TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The end-points of the transfer function are zero scale, a point that is 1 LSB below the first code transition, and full scale, a point that is 1 LSB above the last code transition.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
Offset error is the deviation of the first code transition (00 … 000) to (00 … 001) from the ideal, that is, AGND + 1 LSB.

Offset Error Match
Offset error match is the difference in offset error between any two channels.

Gain Error
Gain error is the deviation of the last code transition (111 … 110) to (111 … 111) from the ideal (that is, V_{REF} − 1 LSB) after the offset error has been adjusted out.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale, 5 kHz sine wave signal to all nonselected ADC input channels and determining how much that signal is attenuated in the selected channel. This specification is the worst case across all ADC channels for the AD5592R/AD5592R-1.

Track-and-Hold Acquisition Time
The track-and-hold amplifier enters hold mode on the falling edge of $\overline{\text{SYNC}}$ and returns to track mode when the conversion is complete. The track-and-hold acquisition time is the minimum time required for the track-and-hold amplifier to remain in track mode for its output to reach and settle to within ±1 LSB of the applied input signal, given a step change to the input signal.

Signal-to-Noise-and-Distortion (SINAD) Ratio
SINAD is the measured ratio of signal-to-noise-and-distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical SINAD ratio for an ideal N-bit converter with a sine wave input is given by

$$SINAD\ (\text{dB}) = 6.02N + 1.76$$

Thus, for a 12-bit converter, SINAD is 74 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD5592R/AD5592R-1, it is defined as

$$THD\ (\text{dB}) = 20 \times \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise (SFDR)
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

DAC TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 17.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 18.

Zero Code Error
Zero code error is a measurement of the output error when zero code (0x000) is loaded to the DAC register. Ideally, the output is 0 V. The zero code error is always positive in the AD5592R/AD5592R-1 because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero code error is expressed in mV.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % FSR.

Offset Error Drift
Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in µV/°C.

Gain Temperature Coefficient
Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error
Offset error is a measurement of the difference between V_{OUT} (actual) and V_{OUT} (ideal), expressed in mV, in the linear region of the transfer function. Offset error can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for a full-scale output of the DAC. It is measured in mV/V. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the rising edge of $\overline{\text{SYNC}}$.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FF to 0x800).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Noise Spectral Density
Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC maintained at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in µV/mA.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa), then executing a software LDAC (see Table 45 and Table 46), and monitoring the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth; the multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The voltage reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows:

$$TC = \left[\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(NOM)} \times Temp\ Range} \right] \times 10^6$$

where:

$V_{REF(MAX)}$ is the maximum reference output measured over the total temperature range.

$V_{REF(MIN)}$ is the minimum reference output measured over the total temperature range.

$V_{REF(NOM)}$ is the nominal reference output voltage, 2.5 V.

Temp Range is the specified temperature range of −40°C to +105°C.

THEORY OF OPERATION

The AD5592R/AD5592R-1 are 8-channel configurable analog and digital input/output ports. The AD5592R/AD5592R-1 have eight pins that can be independently configured as a 12-bit DAC output channel, a 12-bit ADC input channel, a digital input pin, or a digital output pin.

The function of each pin is determined by programming the ADC, DAC, or GPIO configuration registers as appropriate. See the Configuring the AD5592R/AD5592R-1 section and Table 16 for more information.

DAC SECTION

The AD5592R/AD5592R-1 contain eight 12-bit DACs and implement a segmented string DAC architecture with an internal output buffer. Figure 37 shows the internal block diagram of the DAC architecture.

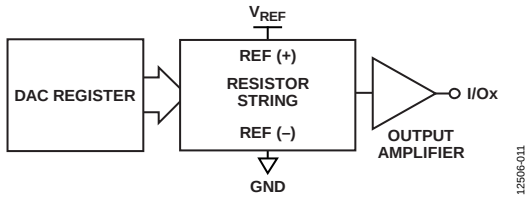


Figure 37. Internal Block Diagram of the DAC Architecture

The DAC channels have a shared gain bit that sets the output range as 0 V to V_{REF} or 0 V to 2 × V_{REF}. Because the gain bit is shared by all channels, it is not possible to set different output ranges on a per channel basis. The input coding to the DAC is straight binary. The ideal output voltage is given by

$$V_{OUT} = G \times V_{REF} \times \left(\frac{D}{2^N} \right)$$

where:
D is the decimal equivalent of the binary code (0 to 4095) that is loaded to the DAC register.
G = 1 for an output range of 0 V to V_{REF}, or G = 2 for an output range of 0 V to 2 × V_{REF}.
N = 12.

Resistor String

The simplified segmented resistor string DAC structure is shown in Figure 38. The code loaded to the DAC register determines the switch on the string that is connected to the output buffer.

Because each resistance in the string has the same value, R, the string DAC is guaranteed monotonic.

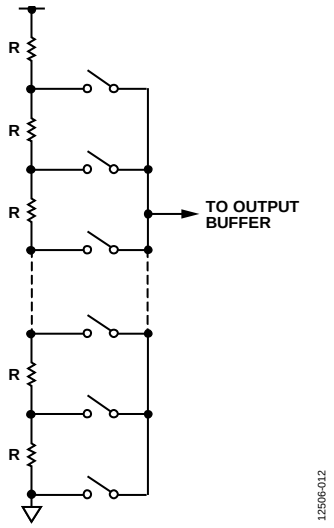


Figure 38. Simplified Resistor String Structure

Output Buffer

The output buffer is designed as an input/output rail-to-rail buffer. The output buffer can drive 2 nF capacitance with a 1 kΩ resistor in parallel. The slew rate is 1.25 V/µs with a ¼ to ¾ scale settling time of 6 µs. By default, the DAC outputs update directly after data has been written to the input register. The LDAC register is used to delay the updates until additional channels have been written to, if required. See the Readback and LDAC Mode Register section for more information.

ADC SECTION

The 12-bit, single-supply ADC is capable of throughput rates of 400 kSPS. The ADC is preceded by a multiplexer that switches selected I/Ox pins to the ADC. A sequencer is included to automatically switch the multiplexer to the next selected channel. Channels are selected for conversion by writing to the ADC sequence register. When the write to the ADC sequence register has completed, the first channel in the conversion sequence is put into track mode. Allow each channel to track the input signal for a minimum of 500 ns. The first $\overline{\text{SYNC}}$ falling edge following the write to the ADC sequence register begins the conversion of the first channel in the sequence. The next $\overline{\text{SYNC}}$ falling edge starts a conversion on the second channel in the sequence and also begins to clock the first ADC result onto the serial interface. ADC data is clocked out of the AD5592R in a 16-bit frame. D15 is 0 to indicate that the data contains ADC data, D14 to D12 is the binary representation of the ADC address, and D11 to D0 is the ADC result (see Table 12).

Each conversion takes 2 µs, and the conversion must be completed before another conversion is initiated. Only write to the AD5592R/AD5592R-1 when no conversion is taking place. I/O7 can be configured as a $\overline{\text{BUSY}}$ signal to indicate when a conversion is taking place. $\overline{\text{BUSY}}$ goes low while a conversion is in progress, and high when an ADC result is available. The ADC has an input range selection bit (Bit D5 in the general-purpose control register), which sets the input range as 0 V to V_{REF} or 0 V to 2 × V_{REF}. All input channels share the same range. The output coding of the ADC is straight binary. It is possible to set each I/Ox pin as both a DAC and an ADC. When an I/Ox pin is set as both a DAC and an ADC, the primary function is that of the DAC. If the pin is selected for inclusion in an ADC conversion sequence, the voltage on the pin is converted and made available via the serial interface, allowing the DAC voltage to be monitored.

Calculating ADC Input Current

The current flowing into the I/Ox pins configured as ADC inputs vary with the sampling rate (f_S), the voltage difference between successive channels (V_{DIFF}), and whether buffered or unbuffered mode is used. Figure 39 shows a simplified version of the ADC input structure. When a new channel is selected for conversion, the 5.8 pF capacitor must be charged or discharged of the voltage that was on the previously selected channel. The time required by the charge or discharge depends on the voltage difference between the two channels. This affects the input impedance of the multiplexer and therefore the input current flowing into the I/Ox pins. In buffered mode, Switch S1 is open and Switch S2 is closed, in which case the U1 buffer is directly driving the 23.1 pF capacitor, and its charging time is negligible. In unbuffered mode, Switch S1 is closed and Switch S2 is closed. In unbuffered mode, the 23.1 pF capacitor must be charged from the I/Ox pins, which contributes to the input current. For applications where the ADC input current is too high, an external input buffer may be required. The choice of buffer is a function of the particular application.

Calculate the input current for buffered mode as follows:

$$f_S \times C \times V_{DIFF} + 1 \text{ nA}$$

where:
f_S is the ADC sample rate in Hertz.
C is the sampling capacitance in Farads.
V_{DIFF} is the voltage change between successive channels.
1 nA is the dc leakage current associated with buffered mode.

Calculate the input current for unbuffered mode as follows:

$$f_S \times C \times V_{DIFF}$$

An example solution is as follows: for the ADC input current in buffered mode, where I/O0 = 0.5 V, I/O1 = 2 V, and f_S = 10 kHz,

$$(10{,}000 \times 5.8 \times 10^{-12} \times 1.5) + 1 \text{ nA} = 88 \text{ nA}$$

Under the same conditions, the ADC input current in unbuffered mode is as follows:

$$(10{,}000 \times 28.9 \times 10^{-12} \times 1.5) = 433.5 \text{ nA}$$

Table 12. ADC Conversion Format

MSB				LSB
D15	**D14**	**D13**	**D12**	**D11 to D0**
0	ADC address			12-bit ADC data

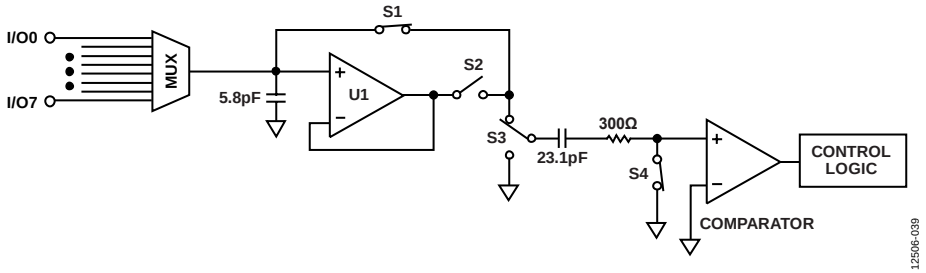


Figure 39. ADC Input Structure

GPIO SECTION

Each of the eight I/Ox pins can be configured as a general-purpose digital input pin by programming the GPIO read configuration register or as a digital output pin by programming the GPIO write configuration register. When an I/Ox pin is configured as an output, the pin can be set high or low by programming the GPIO write data register. Logic levels for general-purpose outputs are relative to V_{DD} and GND. When an I/Ox pin is configured as an input, its status can be determined by setting Bit D10 in the GPIO read configuration register (see Table 37). The next SPI operation clocks out the state of the GPIO pins. When an I/Ox pin is set as an output, it is possible to read its status by also setting it as an input pin. When reading the status of the I/Ox pins set as inputs, the status of an I/Ox pin set as both an input and output pin is also returned.

INTERNAL REFERENCE

The AD5592R/AD5592R-1 contain an on-chip 2.5 V reference. The reference is powered down by default and is enabled by setting Bit D9 in the power-down register to 1 (see Table 43). When the on-chip reference is powered up, the reference voltage appears on the V_{REF} pin and may be used as a reference source for other components. When the internal reference is used, it is recommended to decouple the internal reference to GND using a 100 nF capacitor. It is recommended that the internal reference be buffered before using it elsewhere in the system. When the reference is powered down, an external reference must be connected to the V_{REF} pin. Suitable external reference sources for the AD5592R/AD5592R-1 include the AD780, AD1582, ADR431, REF193, and ADR391.

$\overline{\text{RESET}}$ FUNCTION

The AD5592R/AD5592R-1 have an asynchronous $\overline{\text{RESET}}$ pin. For normal operation, $\overline{\text{RESET}}$ is tied high. A falling edge on $\overline{\text{RESET}}$ resets all registers to their default values and reconfigures the I/Ox pins to their default values (85 kΩ pull-down to GND). The reset function takes 250 µs maximum; do not write new data to the AD5592R/AD5592R-1 during this time. The AD5592R/AD5592R-1 have a software reset that performs the same function as the $\overline{\text{RESET}}$ pin. The reset function is activated by writing 0x5AC to the reset register (see Table 44).

TEMPERATURE INDICATOR

The AD5592R/AD5592R-1 contain an integrated temperature indicator, which can be read to provide an estimation of the die temperature. The temperature reading can be used in fault detection where a sudden rise in die temperature may indicate a fault condition such as a shorted output. Temperature readback is enabled by setting Bit D8 in the ADC sequence register to 1 (see Table 28). The temperature result is then added to the ADC sequence. The temperature result has an address of 0b1000; take care that this result is not confused with the readback from DAC0. The temperature conversion takes 5 µs with the ADC buffer enabled and 20 µs when the buffer is disabled. Calculate the temperature by using the following formulae:

For ADC gain = 1,

$$Temperature\ (°C) = 25 + \frac{\left(ADC\ Code - \left(0.5/V_{REF}\right) \times 4095\right)}{\left(2.654 \times \left(2.5/V_{REF}\right)\right)}$$

For ADC gain = 2,

$$Temperature\ (°C) = 25 + \frac{\left(ADC\ Code - \left(0.5/\left(2 \times V_{REF}\right)\right) \times 4095\right)}{\left(1.327 \times \left(2.5/V_{REF}\right)\right)}$$

The range of codes returned by the ADC when reading from the temperature indicator is approximately 645 to 1035, corresponding to a temperature between −40°C to +105°C. The accuracy of the temperature indicator, averaged over five samples, is typically 3°C.

SERIAL INTERFACE

The AD5592R/AD5592R-1 have a serial interface ($\overline{SYNC}$, SCLK, SDI, and SDO), which is compatible with SPI standards, as well as with most DSPs. The input shift register is 16 bits wide (see Table 13). The MSB (D15) determines what type of write function is required. When D15 is 0, a write to the control register is selected. The control register address is selected by D14 to D11. D10 and D9 are reserved and are 0s. D8 to D0 set the data that is written to the selected control register. When D15 is 1, data is written to a DAC channel (assuming that channel has been set to be a DAC). D14 to D12 select which DAC is addressed. D11 to D0 is the 12-bit data loaded to the selected DAC, with D11 being the MSB of the DAC data. Table 14 shows the control register map for the AD5592R/AD5592R-1. The register map allows the operation of each of the I/Ox pins to be configured. ADCs can be selected for inclusion in sampling sequences. DACs can be updated individually or simultaneously (see the LDAC Mode Operation section). GPIO settings are also controlled via the register map.

POWER-UP TIME

When power is applied to the AD5592R/AD5592R-1, the power-on reset block begins to configure the device and to load the registers with their default values. The configuration process takes 250 µs; do not write to any of the registers during this time.

WRITE MODE

Figure 4 shows the read and write timing for the AD5592R/AD5592R-1. A write sequence begins by bringing the $\overline{SYNC}$ line low. Data on SDI is clocked into the 16-bit shift register on the falling edge of SCLK. After the 16th falling clock edge, the last data bit is clocked in. $\overline{SYNC}$ is brought high, and the programmed function is executed (that is, a change in a DAC input register or a change in a control register). $\overline{SYNC}$ must be brought high for a minimum of 20 ns before the next write. All interface pins must be operated close to the V_{DD} or V_{LOGIC} rails to minimize power consumption in the digital input buffers.

READ MODE

The AD5592R/AD5592R-1 allow data readback from the ADCs and control registers via the serial interface. ADC conversions are automatically clocked out on the serial interface as part of a sequence or as a single ADC conversion. Reading from a register first requires a write to the readback and LDAC mode register to select the register to read back. The contents of the selected register are clocked out on the next 16 SCLKs following a falling edge of $\overline{SYNC}$. Note that due to timing requirements of t_{10} (25 ns), the maximum speed of the SPI interface during a read operation must not exceed 20 MHz.

Table 13. Input Shift Register Format

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	Control register address				0	0	Control register data								
1	DAC address				12-bit DAC data										

Table 14. Control Register Map

MSB (D15)	Address (D14 to D11)	Name	Description	Default Value
0	0000	NOP	No operation	0x000
0	0001	DAC readback	Selects and enables DAC readback	0x000
0	0010	ADC sequence register	Selects ADCs for conversion	0x000
0	0011	General-purpose control register	DAC and ADC control register	0x000
0	0100	ADC pin configuration	Selects which pins are ADC inputs	0x000
0	0101	DAC pin configuration	Selects which pins are DAC outputs	0x000
0	0110	Pull-down configuration	Selects which pins have a 85 kΩ pull-down resistor to GND	0x0FF
0	0111	Readback and LDAC mode	Selects the operation of the Load DAC (LDAC) function and/or which configuration register is read back	0x000
0	1000	GPIO write configuration[1]	Selects which pins are general-purpose outputs	0x000
0	1001	GPIO write data	Writes data to the general-purpose outputs	0x000
0	1010	GPIO read configuration	Selects which pins are general-purpose inputs	0x000
0	1011	Power-down/reference control	Powers down DACs and enables/disables the reference	0x000
0	1100	GPIO open-drain configuration	Selects open-drain or push/pull for general-purpose outputs	0x000
0	1101	Three-state configuration	Selects which pins are three-state	0x000
0	1110	Reserved	Reserved	
0	1111	Software reset	Resets the AD5592R/AD5592R-1	0x000
1	XXX[2]	DAC write	Writes to addressed DAC register	0x000

[1] This register is also used to set I/O7 as a $\overline{BUSY}$ output.
[2] D14 to D11 is the DAC register address (see Table 13).

CONFIGURING THE AD5592R/AD5592R-1

The AD5592R/AD5592R-1 I/Ox pins are configured by writing to a series of configuration registers. The control registers are accessed when the MSB of a serial write is 0, as shown in Table 13. The control register map for the AD5592R/AD5592R-1 is shown in Table 14. At power-up, the I/Ox pins are configured as 85 kΩ pull-down resistors connected to GND.

The input/output channels of the AD5592R/AD5592R-1 can be configured to operate as DAC outputs, ADC inputs, digital outputs, digital inputs, three-state, or connected to GND with 85 kΩ pull-down resistors. When configured as digital outputs, the I/Ox pins have the additional option of being configured as push/pull or open-drain. The input/output channels are configured by writing to the appropriate configuration registers, as shown in Table 15 and Table 16. To assign a particular function to an input/output channel, the user writes to the appropriate register and sets the corresponding bit to 1. For example, setting Bit D0 in the DAC configuration register to 1 configures I/O0 as a DAC (see Table 20).

In the event that the bit for an input/output channel is set in multiple configuration registers, the input/output channel takes the function dictated by the last write operation. The exceptions to this rule are that an I/Ox pin can be set as both a DAC and an ADC or as a digital input and output. When an I/Ox pin is configured as a DAC and ADC, its primary function is as a DAC, and the ADC can measure the voltage being provided by the DAC. This feature can monitor the output voltage to detect short circuits or overload conditions.

When a pin is configured as both a general-purpose input and output, the primary function is as an output pin. This configuration allows the status of the output pin to be determined by reading the GPIO register. Figure 40 shows a typical configuration example where I/O0 and I/O1 are configured as ADCs, I/O2 and I/O3 are configured as DACs, I/O4 is a general-purpose output pin, I/O5 is a general-purpose input pin, and I/O6 and I/O7 are three-state.

The general-purpose control register also contains other functions associated with the DAC and ADC, such as the lock configuration bit. When the lock configuration bit is set to 1, any writes to the pin configuration registers are ignored, thus preventing the function of the I/Ox pins from being changed.

The I/Ox pins can be reconfigured at any time when the AD5592R/ AD5592R-1 is in an idle state, that is, no ADC conversions are taking place and no registers are being read back. The lock configuration bit must also be 0.

Table 15. I/Ox Pin Configuration Registers

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Register address				Reserved			IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0

Table 16. Bit Descriptions for the I/Ox Pin Configuration Registers

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Selects which pin configuration register is addressed. 0100: ADC pin configuration. 0101: DAC pin configuration. 0110: pull-down configuration. (Default condition at power-up.) 1000: GPIO write configuration. 1010: GPIO read configuration. 1100: GPIO open-drain configuration. 1101: three-state configuration.
D10 to D8	Reserved	Reserved. Set these bits to 0.
D7 to D0	IO7 to IO0	Enable register function on selected I/Ox pin. 0: no function selected. 1: set the selected I/Ox pin to the register function.

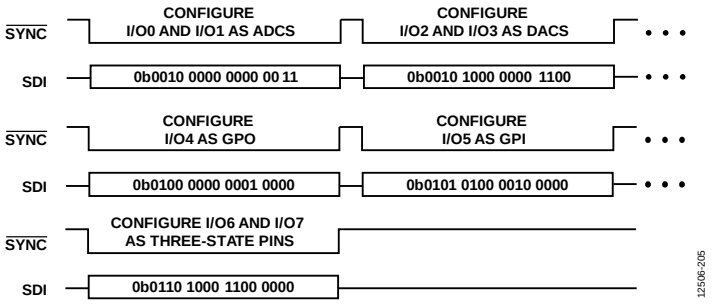


Figure 40. Typical Configuration Example

GENERAL-PURPOSE CONTROL REGISTER

The general-purpose control register enables or disables certain functions associated with the DAC, ADC, and I/Ox pin configuration (see Table 17 and Table 18). The general-purpose control register sets the gain of the DAC and ADC. Bit D5 sets the input range for the ADC, and Bit D4 sets the output range of the DAC.

The general-purpose control register also enables/disables the ADC buffer and precharge function (see the ADC Section for more details). The register can also be used to lock the I/Ox pin configuration to prevent accidental change. When Bit D7 is set to 1, writes to the configuration registers are ignored.

Table 17. General-Purpose Control Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Register address				Reserved	ADC buffer precharge	ADC buffer enable	Lock	All DACs	ADC range	DAC range	Reserved			

Table 18. Bit Descriptions for the General-Purpose Control Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b0011.
D10	Reserved	Reserved. Set this bit to 0.
D9	ADC buffer precharge	ADC buffer precharge. 0: ADC buffer is not used to precharge the ADC. If the ADC buffer is enabled, it is always powered up (default). 1: ADC buffer is used to precharge the ADC. If the ADC buffer is enabled, it is powered up while the conversion takes place and then powered down until the next conversion takes place.
D8	ADC buffer enable	ADC buffer enable. 0: ADC buffer is disabled (default). 1: ADC buffer is enabled.
D7	Lock	Lock configuration. 0: the contents of the I/Ox pin configuration registers can be changed (default). 1: the contents of the I/Ox pin configuration registers cannot be changed.
D6	All DACs	Write all DACs. 0: for future DAC writes, the DAC address bits determine which DAC is written to (default). 1: for future DAC writes, the DAC address bits are ignored, and all channels configured as DACs are updated with the same data.
D5	ADC range	ADC input range select. 0: ADC gain is 0 V to V_{REF} (default). 1: ADC gain is 0 V to 2 × V_{REF}.
D4	DAC range	DAC output range select. 0: DAC output range is 0 V to V_{REF} (default). 1: DAC output range is 0 V to 2 × V_{REF}.
D3 to D0	Reserved	Reserved. Set these bits to 0.

DAC WRITE OPERATION

To set a pin as a DAC, set the appropriate bit in the DAC pin configuration register to 1 (see Table 19 and Table 20). For example, setting Bit 0 to Bit 1 enables I/O0 as a DAC output. Data is written to a DAC when the MSB (D15) of the serial write is 1. D14, D13, and D12 determine which DAC is addressed, and D11 to D0 contain the 12-bit data to be written to the DAC, as shown in Table 21 and Table 22. Data is written to the selected DAC input register. Data written to the input register can be automatically copied to the DAC register, if required. Data is transferred to the DAC register based on the setting of the LDAC mode register (see Table 45 and Table 46).

LDAC Mode Operation

When the LDAC mode bits (D1 and D0) are 00 respectively, new data is automatically transferred from the input register to the DAC register, and the analog output updates. When the LDAC mode bits are 01, data remains in the input register. This LDAC mode allows writes to input registers without affecting the analog outputs. When the input registers have been loaded with the desired values, setting the LDAC mode bits to 10 transfers the values in the input registers to the DAC registers, and the analog outputs update simultaneously. The LDAC mode bits then revert back to 01, assuming their previous setting was 01. See Table 45 and Table 46.

Table 19. DAC Pin Configuration Register

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	Register address				Reserved			DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

Table 20. Bit Descriptions for the DAC Pin Configuration Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b0101.
D10 to D8	Reserved	Reserved. Set these bits to 0.
D7 to D0	DAC7 to DAC0	Select I/Ox pins as DAC outputs. 1: I/Ox is a DAC output. 0: I/Ox function is determined by the pin configuration registers (default).

Table 21. DAC Write Register

MSB **LSB**

D15	D14	D13	D12	D11 (MSB)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	DAC address			12-bit DAC data											

Table 22. Bit Descriptions for the DAC Data Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 1.
D14 to D12	DAC address	Bit D14 to Bit D12 select the DAC register to which the data in D11 to D0 is loaded. 000: DAC0 001: DAC1 010: DAC2 011: DAC3 100: DAC4 101: DAC5 110: DAC6 111: DAC7
D11 to D0	12-bit DAC data	12-bit DAC data.

DAC READBACK

The input register of each DAC can be read back via the SPI interface. Reading back the DAC register value can be used to confirm that the data was received correctly before writing to the LDAC register, or to check what value was last loaded to a DAC. Data can only be read back from a DAC when there is no ADC conversion sequence taking place.

To read back a DAC input register, it is first necessary to enable the readback function and select which DAC register is required. This is achieved by writing to the DAC read back register (shown in Table 23 and Table 24). Set the D4 and D3 bits to 1 to enable the readback function. The D2 to D0 bits select which DAC data is required. The DAC data is clocked out of the AD5592R/AD5592R-1 on the subsequent SPI operation. Figure 41 shows an example of setting I/O3, configured as a DAC, to midscale. The input data is then read back. D14 to D12 contain the address of the DAC register being read back, and D15 is 1.

Table 23. DAC Readback Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Register address				Reserved						Enable DAC readback		DAC channel		

Table 24. Bit Descriptions for the DAC Readback Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b0001.
D10 to D5	Reserved	Reserved. Set these bits to 0.
D4 and D3	Enable DAC readback	Enable readback of the DAC input register. 11: readback enabled. 00: readback disabled (default).
D2 to D0	DAC channel	Select DAC channel. 000: DAC0 001: DAC1 … 110: DAC6 111: DAC7

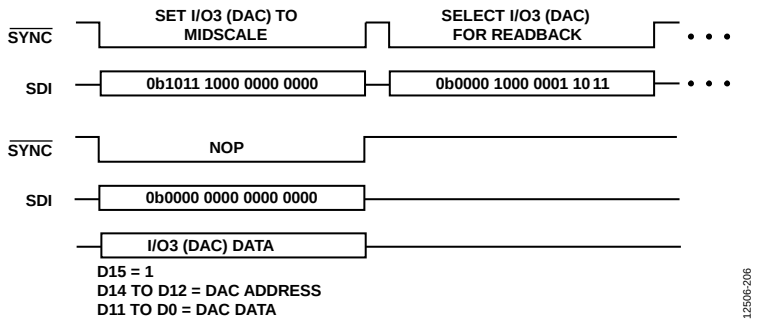


Figure 41. DAC Readback Operation

ADC OPERATION

To set a pin as an ADC, set the appropriate bit in the ADC pin configuration register to 1 (see Table 25 and Table 26). For example, setting Bit 0 to Bit 1 enables I/O0 as an ADC input. The ADC channels of the AD5592R/AD5592R-1 operate as a traditional multichannel ADC, where each serial transfer selects the next channel for conversion. Writing to the ADC sequence register (see Table 27 and Table 28) selects the ADC channels to be included in the sequence, and the REP bit determines if the sequence is repeated. The $\overline{\text{SYNC}}$ signal is used to frame the write to the converter on the SDI pin. The data that appears on the SDO pin during the initial write to the ADC sequence register is invalid. When the sequence register is written to, the ADC begins to track the first channel in the sequence. Tracking takes 500 ns; do not initiate a conversion until this time has passed. The next $\overline{\text{SYNC}}$ falling edge initiates a conversion on the selected channel. The subsequent $\overline{\text{SYNC}}$ falling edge begins clocking out the ADC result and also initiates the next conversion. The ADC operates with one cycle latency, thus the conversion result corresponding to each conversion is available one serial read cycle after the cycle in which the conversion was initiated.

If more than one channel is selected in the ADC sequence register, the ADC converts all selected channels sequentially in ascending order on successive $\overline{\text{SYNC}}$ falling edges. Once all the selected channels in the control register are converted, the ADC repeats the sequence if the REP bit is set. If the REP bit is clear, the ADC goes three-state. Figure 42 to Figure 45 show typical ADC modes of operation. I/O7 can be configured as a $\overline{\text{BUSY}}$ output pin to indicate when a conversion result is available. $\overline{\text{BUSY}}$ goes low while a conversion takes place and goes high when the conversion result is available. The conversion result is clocked out on the SDO pin on the following read/write operation. For an ADC conversion, D15 is 0, D14 to D12 contain the ADC address, and D11 to D0 contain the 12-bit conversion result, as shown in Table 29.

Changing an ADC Sequence

The channels included in an ADC sequence can be changed by first stopping an existing conversion sequence (see Figure 46). The ADC conversion sequence is stopped by clearing the REP, TEMP, and ADC7 to ADC0 bits in the ADC sequence register to 0.

As the command to stop the sequence is written, an ADC conversion is also taking place. This conversion must finish before a new sequence can be written to the ADC sequence register. Allow a minimum of 2 µs between starting the write to end the current sequence and starting the write to select a new sequence. After selecting the new sequence, allow an ADC track time of 500 ns before initiating the next conversion.

Table 25. ADC Pin Configuration Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Register address				Reserved			ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

Table 26. Bit Descriptions for the ADC Pin Configuration Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b0100.
D10 to D8	Reserved	Reserved. Set these bits to 0.
D7 to D0	ADC7 to ADC0	Select I/Ox pins as ADC inputs. 1: I/Ox is an ADC input. 0: I/Ox function is determined by the pin configuration registers (default).

Table 27. ADC Sequence Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Register address				Reserved	REP	TEMP	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

Table 28. Bit Descriptions for the ADC Sequence Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b0010.
D10	Reserved	Reserved. Set these bits to 0.
D9	REP	ADC sequence repetition. 0: sequence repetition disabled (default). 1: sequence repetition enabled.
D8	TEMP	Include temperature indicator in ADC sequence. 0: disable temperature indicator readback (default). 1: enable temperature indicator readback.
D7 to D0	ADC7 to ADC0	Include ADC channels in conversion sequence. 0: the selected ADC channel is not included in the conversion sequence. 1: include the selected ADC channel in the conversion sequence.

Table 29. ADC Conversion Result

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	ADC address[1]			12-bit ADC result											

[1] The ADC addresses are as follows: 000 = ADC0 … 111 = ADC7.

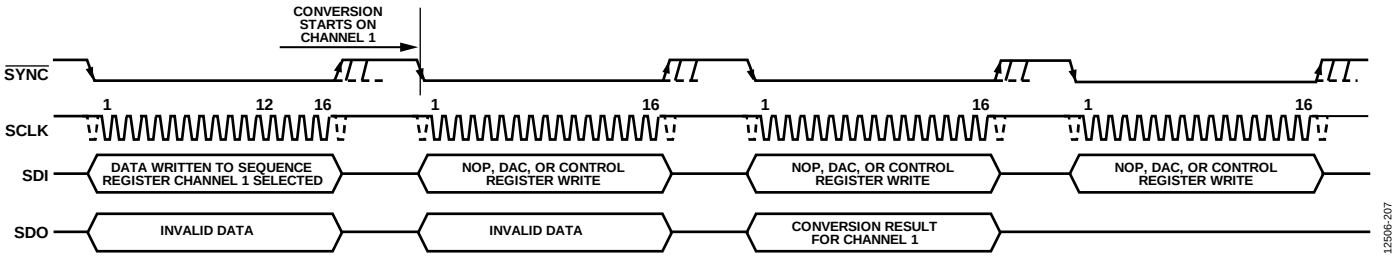


Figure 42. Single-Channel ADC Conversion Sequence, No Repeat

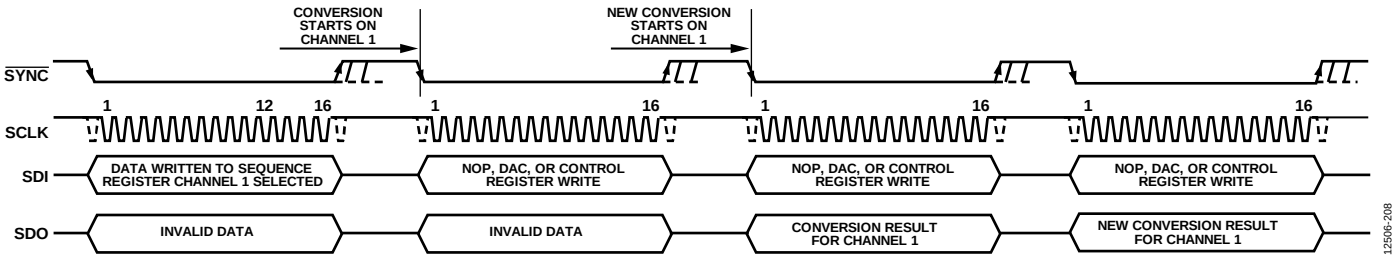


Figure 43. Single-Channel, Repeating, ADC Conversion Sequence

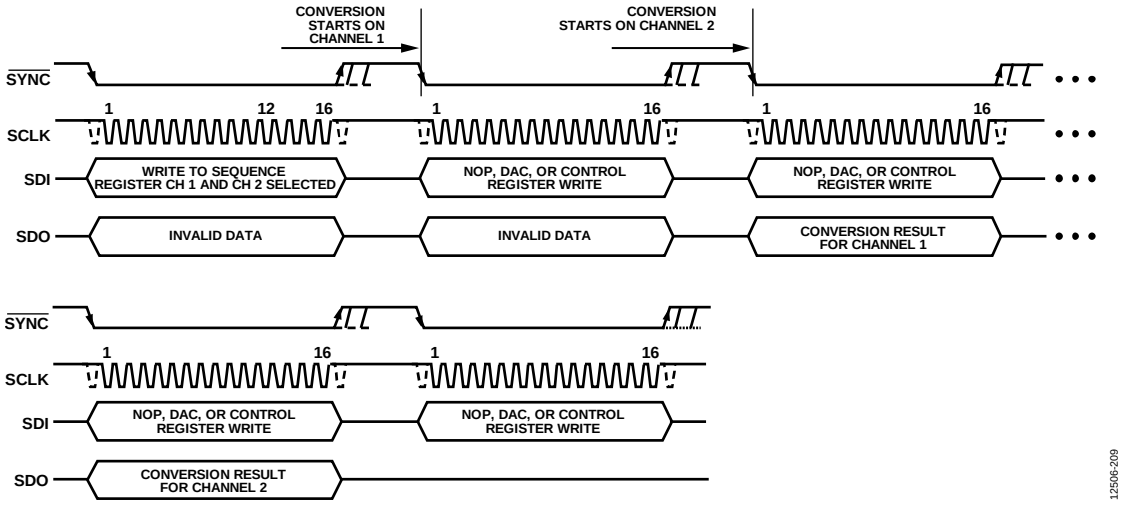


Figure 44. Multichannel ADC Conversion Sequence, No Repeat

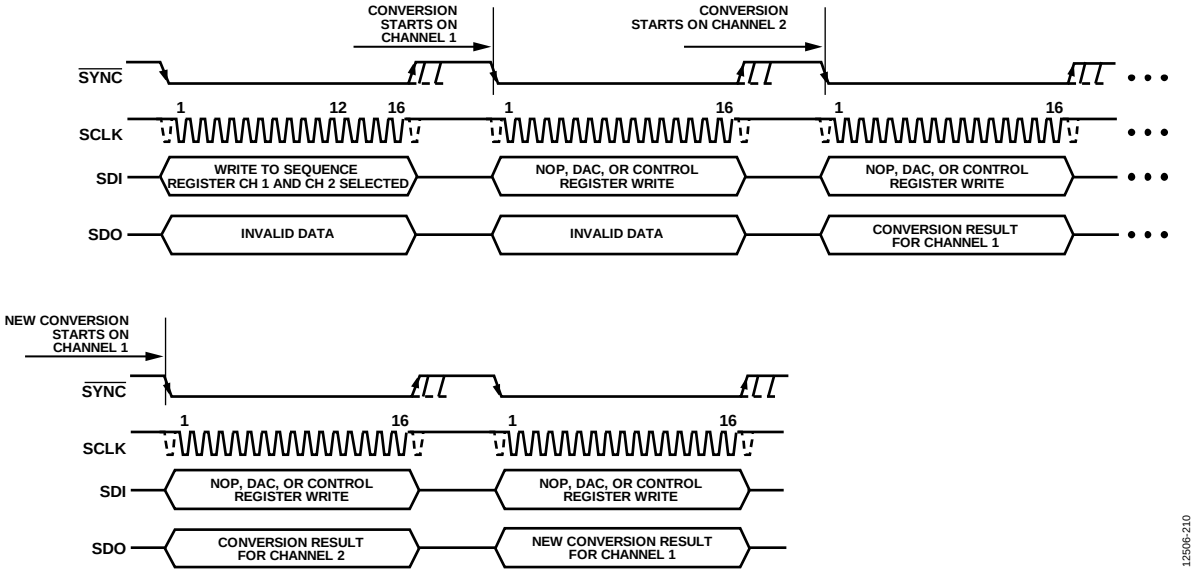


Figure 45. Multichannel, Repeating, ADC Conversion Sequence

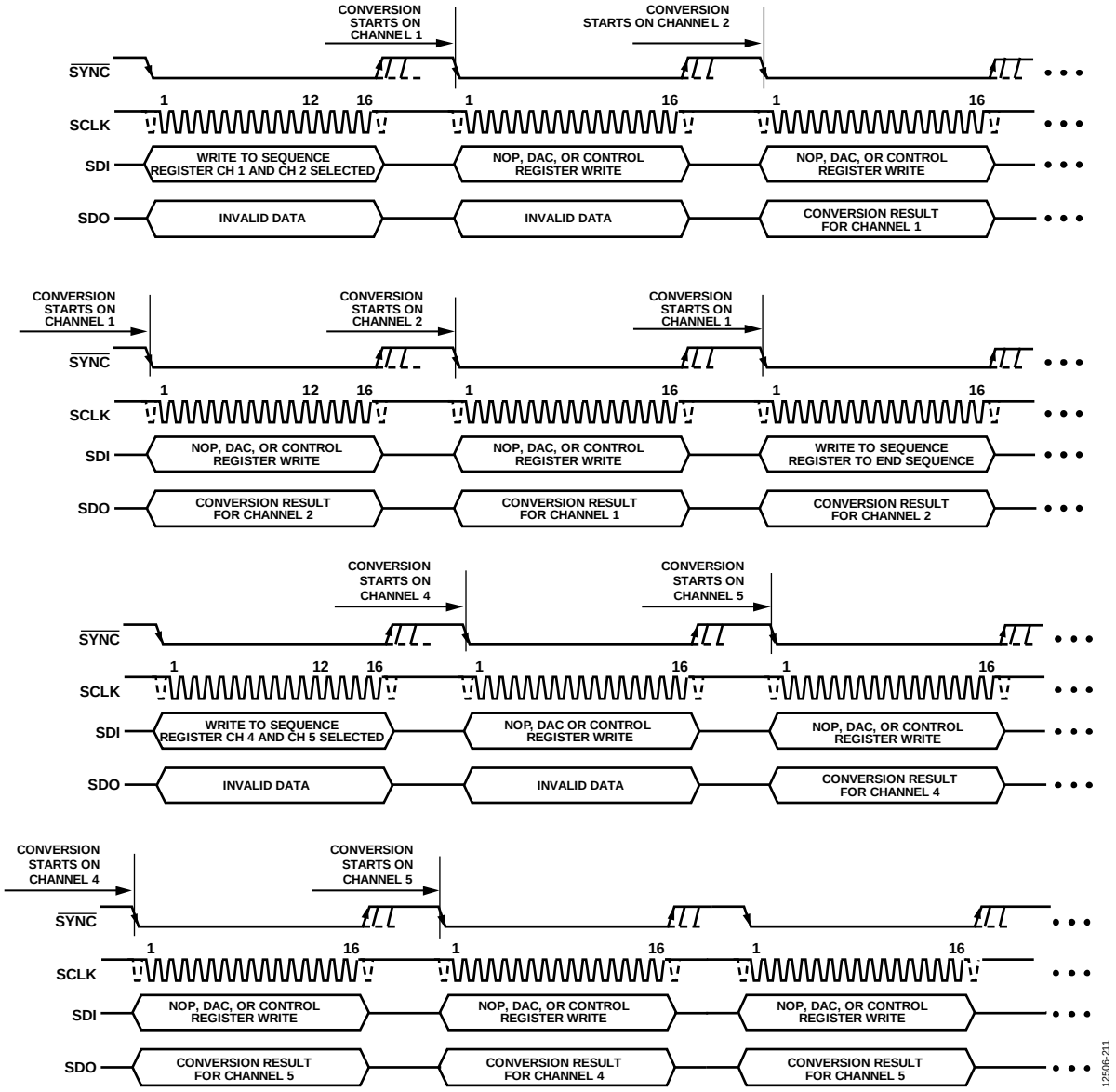


Figure 46. Changing a Multichannel, Repeating, ADC Conversion Sequence

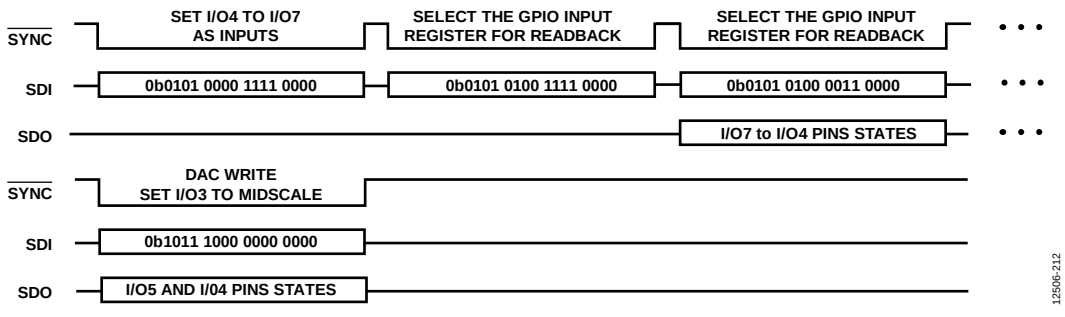


Figure 47. Configuring and Reading General-Purpose Input Pins

GPIO OPERATION

Each of the I/Ox pins of the AD5592R/AD5592R-1 can operate as a general-purpose, digital input or output pin. The function of the pins is determined by writing to the appropriate bit in the GPIO read configuration and GPIO write configuration registers.

Setting Pins as Outputs

To set a pin as a general-purpose output, set the appropriate bit in the GPIO write configuration register to 1 (see Table 30 and Table 31). For example, setting Bit 0 to Bit 1 enables I/O0 as a general-purpose output. The state of the output pin is controlled by setting or clearing the bits in the GPIO write data register (see Table 34). A data bit is ignored if it is written to a location that is not configured as an output.

The outputs can be independently configured as push/pull or open-drain outputs. When in a push/pull configuration, the output is driven to V_{DD} or GND, as determined by the data in the GPIO write data register. To set a pin as an open-drain output, set the appropriate bit in the GPIO open-drain configuration register to 1 (see Table 32 and Table 33). When in an open-drain configuration, the output is driven to GND when a data bit in the GPIO write data register sets the pin low. When the pin is set high, the output is not driven and must be pulled high by an external resistor. Open-drain configuration allows for multiple output pins to be tied together. If all the pins are normally high, the open-drain configuration allows for one pin to pull down the others pins. This method is commonly used where multiple pins are used to trigger an alarm or an interrupt pin.

To change the state of the I/Ox pins, a write to the GPIO write data register is required. Setting a bit to 1 gives a Logic 1 on the selected output. Clearing a bit to 0 gives a Logic 0 on the selected output.

Setting Pins as Inputs

To set a pin as a general-purpose input, set the appropriate bit in the GPIO read configuration register to 1 (see Table 36 and Table 37). For example, setting Bit 0 to Bit 1 enables I/O0 as a general-purpose input. To read the state of the general-purpose inputs, write to the GPIO read and configuration register to set Bit D10 to 1 and also any of Bit D7 to Bit D0 that correspond to a general-purpose input pin. The following SPI operation clocks out the state of any pins set as general-purpose inputs. Figure 47 shows an example where I/O4 to I/O7 are set as general-purpose inputs. I/O3 is assumed to be a DAC. To read the status of I/O7 to I/O4, Bit D10 and Bit D7 to Bit D4 are set to 1. To read the status of I/O5 and I/O4, only Bit D10, Bit D5, and Bit D4 need to be set to 1. The status of I/O7 and I/O6 are not read, and Bit D7 and Bit D6 are read as 0. Figure 47 also has a write to a DAC to show that other operations can be included when reading the status of the general-purpose pins.

Table 30. GPIO Write Configuration Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Register address				Reserved		Enable $\overline{\text{BUSY}}$	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Table 31. Bit Descriptions for the GPIO Write Configuration Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b1000.
D10 to D9	Reserved	Reserved. Set this bit to 0.
D8	Enable $\overline{\text{BUSY}}$	Enable the I/O7 pin as $\overline{\text{BUSY}}$. 0: Pin I/O7 is not configured as $\overline{\text{BUSY}}$. 1: Pin I/O7 is configured as $\overline{\text{BUSY}}$. D7 must also be set to 1 to enable the I/O7 pin as an output.
D7 to D0	GPIO7 to GPIO0	Select I/Ox pins as GPIO outputs. 1: I/Ox is a general-purpose output pin. 0: I/Ox function is determined by the pin configuration registers (default).

Table 32.GPIO Open-Drain Configuration Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Register address				Reserved			Open Drain 7	Open Drain 6	Open Drain 5	Open Drain 4	Open Drain 3	Open Drain 2	Open Drain 1	Open Drain 0

Table 33. Bit Descriptions for the GPIO Open-Drain Configuration Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b1100.
D10 to D8	Reserved	Reserved. Set these bits to 0.
D7 to D0	Open Drain 7 to Open Drain 0	Set output pins as open-drain. The pins must also be set as digital output pins. See Table 31. 1: I/Ox is an open-drain output pin. 0: I/Ox is a push/pull output pin (default).

Table 34. GPIO Write Data Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Register address				Reserved			GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Table 35. Bit Descriptions for the GPIO Write Data Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b1001.
D10 to D8	Reserved	Reserved. Set these bits to 0.
D7 to D0	GPIO7 to GPIO0	Set state of output pins. 1: I/Ox is a Logic 1. 0: I/Ox is a Logic 0.

Table 36. GPIO Read Configuration Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Register address				Enable readback	Reserved		GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Table 37. Bit Descriptions for the GPIO Read Configuration Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b1010.
D10	Enable readback	Enable GPIO readback. 1: the next SPI operation clocks out the state of the GPIO pins. 0: Bit D7 to Bit D0 determine which pins are set as general-purpose inputs.
D9 to D8	Reserved	Reserved. Set these bits to 0.
D7 to D0	GPIO7 to GPIO0	Set I/Ox pins as GPIO inputs. 1: I/Ox is a general-purpose input pin. 0: I/Ox function is determined by the pin configuration registers (default).

THREE-STATE PINS

The I/Ox pins can be set to three-state by writing to the three-state configuration register, as shown in Table 38 and Table 39.

85 kΩ PULL-DOWN RESISTOR PINS

The I/Ox pins can be connected to GND via a pull-down resistor (85 kΩ) by setting the appropriate bits in the pull-down configuration register, as shown in Table 40 and Table 41.

Table 38. Three-State Configuration Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Register address				Reserved			TSO7	TSO6	TSO5	TSO4	TSO3	TSO2	TSO1	TSO

Table 39. Bit Descriptions for the Three-State Configuration Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b1101.
D10 to D8	Reserved	Reserved. Set these bits to 0.
D7 to D0	TSO7 to TSO0	Set I/Ox pins as three-state outputs. 1: I/Ox is a three-state output pin. 0: I/Ox function is determined by the pin configuration registers (default).

Table 40. Pull-Down Configuration Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Register address				Reserved			Pull Down 7	Pull Down 6	Pull Down 5	Pull Down 4	Pull Down 3	Pull Down 2	Pull Down 1	Pull Down 0

Table 41. Bit Descriptions for the Pull-Down Configuration Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b0110.
D10 to D8	Reserved	Reserved. Set these bits to 0.
D7 to D0	Pull Down 7 to Pull Down 0	Set I/Ox pins as weak pull-down outputs. 1: I/Ox is connected to GND via an 85 kΩ pull-down resistor. 0: I/Ox function is determined by the pin configuration registers (default).

POWER-DOWN MODE

The AD5592R/AD5592R-1 have a power configuration register to reduce the power consumption when certain functions are not needed. The power-down register allows any channels set as DACs to be individually placed in a power-down state. When in a power-down state, the DAC outputs are three-state. When a DAC channel is put back into normal mode, the DAC output returns to its previous value. The internal reference and its buffer are powered down by default and are enabled by setting the EN_REF bit in the power-down register. The internal reference voltage then appears at the V_{REF} pin.

There is no dedicated power-down function for the ADC, but the ADC is automatically powered down if none of the I/Ox pins are selected as ADCs. The PD_ALL bit powers down all the DACs, the reference and its buffer, and the ADC simultaneously. Table 42 and Table 43 show the power-down register.

Table 42. Power-Down/Reference Control Register

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	Register address				PD_ALL	EN_REF	Reserved	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Table 43. Bit Descriptions for the Power-Down/Reference Control Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b1011.
D10	PD_ALL	Power down DACs and internal reference. 0: the reference and DACs power-down states are determined by D9 and D7 to D0 (default). 1: the reference, DACs and ADC are powered down.
D9	EN_REF	Enable internal reference. 0: the reference and its buffer are powered down (default). Set this bit if an external reference is used. 1: the reference and its buffer are powered up. The reference is available on the V_{REF} pin.
D8	Reserved	Reserved. Set this bit to 0.
D7 to D0	PD7 to PD0	Power down DACs. 0: the channel is in normal operating mode (default). 1: the channel is powered down if it is configured as a DAC.

RESET FUNCTION

The AD5592R/AD5592R-1 can be reset to their default conditions by writing to the reset register, as shown in Table 44. This write resets all registers to their default values and reconfigures the I/Ox pins to their default values (85 kΩ pull-down resistor to GND). The reset function takes 250 µs maximum; do not write new data to the AD5592R/AD5592R-1 during this time. The AD5592R has a $\overline{\text{RESET}}$ pin that performs the same function. For normal operation, $\overline{\text{RESET}}$ is tied high. A falling edge on $\overline{\text{RESET}}$ triggers the reset function.

READBACK AND LDAC MODE REGISTER

The values contained in the AD5592R/AD5592R-1 registers can be read back to ensure that the registers are correctly set up. The register readback is initiated by writing to the readback and LDAC mode register with Bit D6 set to 1. Bit D5 to Bit D2 select which register is to be read back. The register data is clocked out of the AD5592R/AD5592R-1 on the next SPI transfer.

Bit D1 to Bit D0 of the readback and LDAC mode register select the LDAC mode. The LDAC mode determines if data written to a DAC input register is also transferred to the DAC register. See the LDAC Mode Operation section for details of the LDAC mode function.

Table 44. Software Reset

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	1	1	1	1	0	1	1	0	1	0	1	1	0	0
Control register write	Write to reset register				Reset the AD5592R/AD5592R-1										

Table 45. Readback and LDAC Mode Register

MSB														LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	Register address				Reserved				EN	REG_READBACK				LDAC mode	

Table 46. Bit Descriptions for the Readback and LDAC Mode Register

Bit(s)	Bit Name	Description
D15	MSB	Set this bit to 0.
D14 to D11	Register address	Set these bits to 0b0111.
D10 to D7	Reserved	Reserved. Set these bits to 0.
D6	EN	Enable readback. Note that the LDAC mode bits are always used regardless of the EN bit. 1: Bit D5 to Bit D2 select which register is read back. Bit D6 automatically clears when the read is complete. 0: no readback is initiated.
D5 to D2	REG_READBACK	If Bit D6 is 1, Bits D5 to Bit D2 determine which register is to be read back. 0000: NOP. 0001: DAC readback. 0010: ADC sequence. 0011: general-purpose configuration. 0100: ADC pin configuration. 0101: DAC pin configuration. 0110: pull-down configuration. 0111: LDAC configuration. 1000: GPIO write configuration. 1001: GPIO write data. 1010: GPIO read configuration. 1011: power-down and reference control. 1100: open-drain configuration. 1101: three-state pin configuration. 1110: reserved. 1111: software reset.
D1 to D0	LDAC mode	Determines how data written to an input register of a DAC is handled. 00: data written to an input register is immediately copied to a DAC register, and the DAC output updates (default). 01: data written to an input register is not copied to a DAC register. The DAC output is not updated. 10: data in the input registers is copied to the corresponding DAC registers. When the data has been transferred, the DAC outputs are updated simultaneously. 11: reserved.

APPLICATIONS INFORMATION

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5592R/AD5592R-1 is via a serial bus that uses a standard protocol compatible with DSPs and microcontrollers. The communications channel requires a 4-wire interface consisting of a clock signal, a data input signal, a data output signal, and a synchronization signal. The devices require a 16-bit data-word with data valid on the falling edge of SCLK.

AD5592R/AD5592R-1 TO SPI INTERFACE

The SPI interface of the AD5592R/AD5592R-1 is designed to be easily connected to industry-standard DSPs and microcontrollers. Figure 48 shows the AD5592R/AD5592R-1 connected to the Analog Devices, Inc., ADSP-BF531 Blackfin® DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5592R/AD5592R-1.

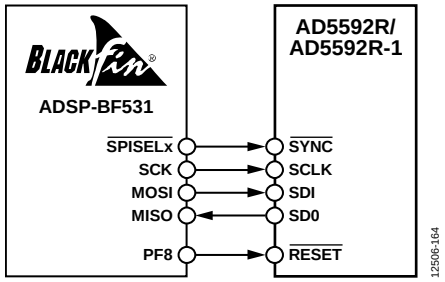


Figure 48. ADSP-BF531 SPI Interface

AD5592R/AD5592R-1 TO SPORT INTERFACE

The Analog Devices ADSP-BF527 has two serial ports (SPORT). Figure 49 shows how a SPORT interface can be used to control the AD5592R/AD5592R-1. The ADSP-BF527 has an SPI port that can also be used. This method is the same as when using the ADSP-BF531.

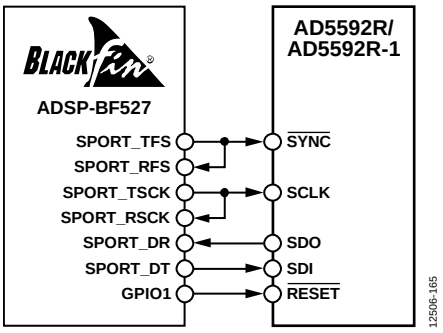


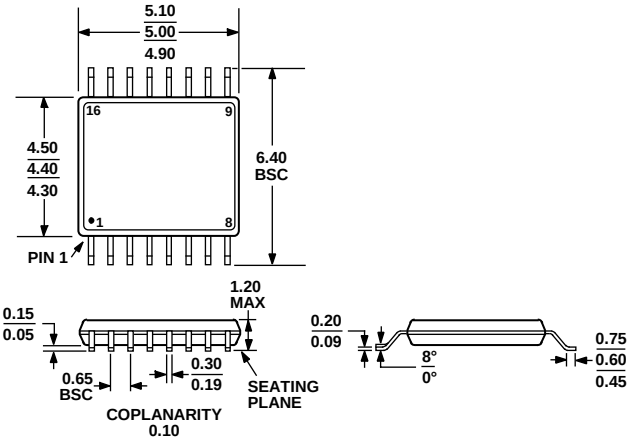
Figure 49. ADSP-BF527 SPORT Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board (PCB) on which the AD5592R or the AD5592R-1 is mounted must be designed so that the AD5592R/AD5592R-1 lie on the analog plane.

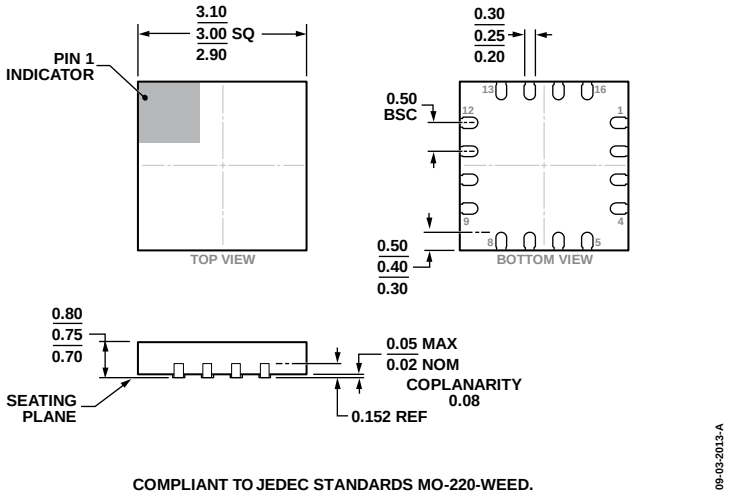
The AD5592R/AD5592R-1 must have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI). Ceramic capacitors, for example, provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 50. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WEED.

Figure 51. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-32)
Dimensions shown in millimeters

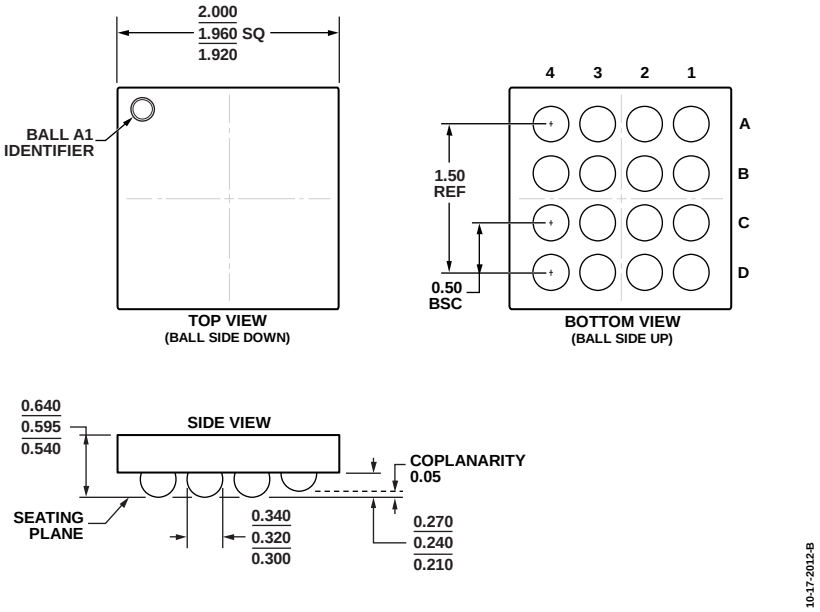


Figure 52. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
AD5592RBCBZ-1-RL7	−40°C to +105°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-3	
AD5592RBCPZ-1-RL7	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-32	DMD
AD5592RBRUZ	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
AD5592RBRUZ-RL7	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
AD5592RBCBZ-RL7	−40°C to +105°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-3	
AD5592RBCPZ-RL7	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-32	DMG
EVAL-AD5592R-1SDZ		Evaluation Board		
EVAL-SDP-CB1Z		Controller Board		

[1] Z = RoHS Compliant Part.