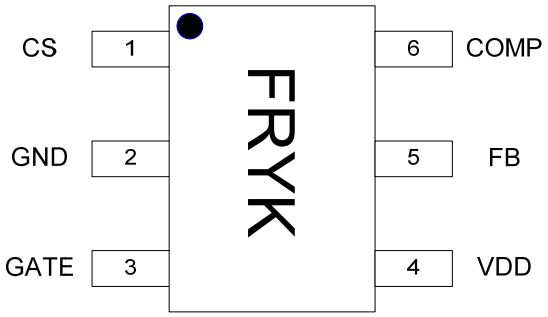
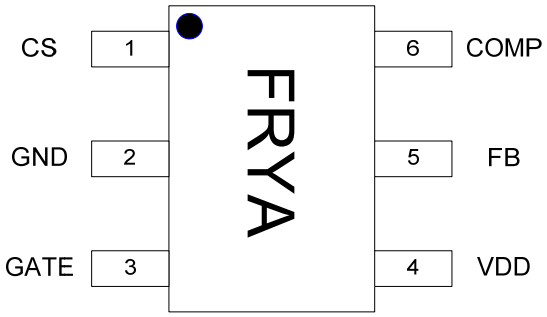
ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING METHOD	MINIMUM SWITCHING FREQUENCY	TOP MARK
ACT413US-T	-40°C to 85°C	SOT23-6	6	TUBE & REEL	1164Hz	FRYK
ACT413AUS-T	-40°C to 85°C	SOT23-6	6	TUBE & REEL	550Hz	FRYA

PIN CONFIGURATION



SOT23-6
ACT413US



SOT23-6
ACT413AUS

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CS	Current Sense Pin. Connect an external resistor (R_{CS}) between this pin and ground to set peak current limit for the primary switch.
2	GND	Ground.
3	GATE	Gate Drive. Gate driver for the external MOSFET transistor.
4	VDD	Power Supply. This pin provides bias power for the IC during startup and steady state operation.
5	FB	Feedback Pin. Connect this pin to a resistor divider network from the auxiliary winding.
6	COMP	Compensation Pin.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
FB, CS, COMP to GND	-0.3 to + 6	V
VDD, GATE to GND	-0.3 to + 22	V
Maximum Power Dissipation (SOT23-6)	0.45	W
Operating Junction Temperature	-40 to 150	˚C
Junction to Ambient Thermal Resistance (θ_{JA})	220	˚C/W
Operating Junction Temperature	-40 to 150	˚C
Storage Temperature	-55 to 150	˚C
Lead Temperature (Soldering, 10 sec)	300	˚C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 13V, L_M = 0.56mH, R_{CS} = 1.05Ω, V_{OUT} = 5V, N_P = 56, N_S = 5, N_A = 13, T_A = 25°C, unless otherwise specified,5V2.4A application.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
VDD Turn-On Voltage	V_{DDON}	V_{DD} Rising from 0V	11.11	12.35	13.58	V
VDD Turn-Off Voltage	V_{DDOFF}	V_{DD} Falling after Turn-on	6.1	6.8	7.5	V
VDD Over Voltage Protection	V_{DDOVP}	V_{DD} Rising from 0V	18.45	20.5	22.55	V
Start Up Supply Current	I_{DDST}	V_{DD} = 11V, before VDD Turn-on		5	10	μA
IDD Supply Current	I_{DD}	V_{DD} = 12V, after VDD Turn-on (no switching)		0.55	1	mA
IDD Supply Current at Fault Mode	I_{DD}	V_{DD} = 12V, after VDD Turn-on, fault = 1		0.25		mA
Feedback						
Effective FB Reference Voltage	V_{FBREF}		2.23	2.25	2.28	V
FB Sampling Blanking Time	T_{FB_BLK}	Light load	0.38	0.45	0.52	μs
		Heavy Load	1.1	1.3	1.5	μs
Time needed for FB Sampling (After blanking)	T_{FB_SAMP}	FB sampling	0.5	0.65	0.75	μs
		CC and Knee point detecting	0.22	0.25	0.29	μs
FB Leakage Current	I_{BVFB}	V_{FB} = 3V			1	μA
Current Limit						
CS Current Limit Threshold	V_{CSLIM}		0.99	1.00	1.01	V
CS Minimum Current Limits Threshold	V_{CSMIN}			300		mV
CS to GATE Propagation Delay				60		ns
Leading Edge Blanking Time	$T_{CSBLANK}$	Light Load		150		ns
		Heavy Load		636		ns

ELECTRICAL CHARACTERISTICS CONT'D

V_{DD} = 13V, L_M = 0.56mH, R_{CS} = 1.05Ω, V_{OUT} = 5V, N_P = 56, N_S = 5, N_A = 13, T_A = 25°C, unless otherwise specified,5V2.4A application.)

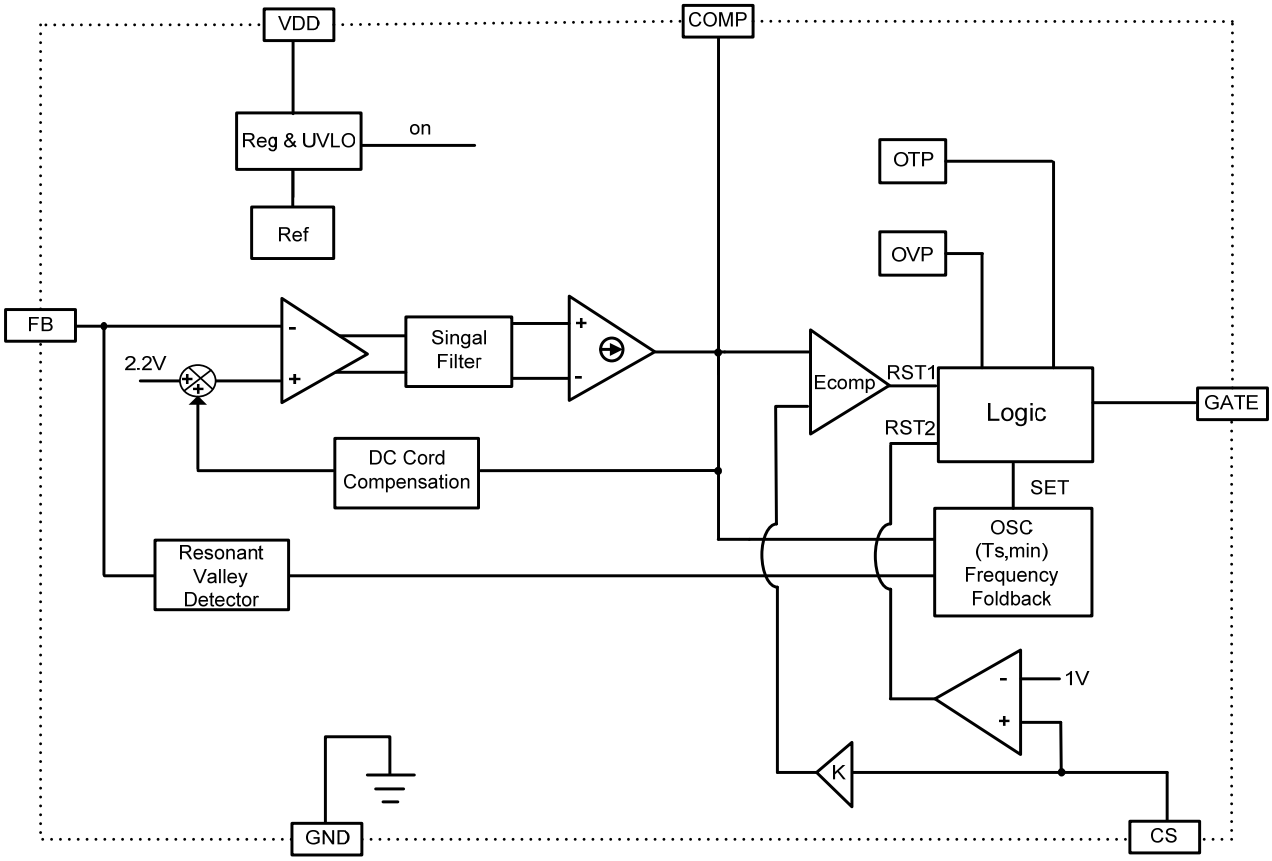
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RCORD						
Output Cable Resistance Compensation	DV_{COMP}	ACT413/ACT413A		6		%
GATE DRIVE						
Gate Rise Time	T_{RISE}	VDD = 10V, CL = 1nF		150	250	ns
Gate Falling Time	T_{FALL}	VDD = 10V, CL = 1nF		90		ns
Gate Low Level ON-Resistance	R_{ONLO}	I_{SINK} = 30mA		10		Ω
Gate High Level ON-Resistance	R_{ONHI}	I_{SOURCE} = 30mA		31		Ω
Gate Leakage Current		GATE = 18V, before VDD turn-on			1	μA
COMPENSATION						
Inside Compensate Resistor	R_{COMP}	ACT413/ACT413A		0		kΩ
Output Sink Current	I_{COMP_SINK}	V_{FB} = 3V, V_{COMP} = 2V	15	40		μA
Output Source Current	I_{COMP_SOURCE}	V_{FB} = 1.5V, V_{COMP} = 2V	15	40		μA
Transconductance of Error Amplifier	Gm			71		μA/V
Maximum Output Voltage	$V_{COMPMAX}$	V_{FB} = 1.5V		3.5		V
Minimum Output Voltage	$V_{COMPMIN}$	V_{FB} = 3V		0.4		V
CS to COMP Gain				2		V/V
Pre-Amp Gain				1		V/V
COMP Leakage Current		COMP = 2.5V			1	μA
OSCILLATOR						
Maximum Switching	f_{MAX}		76	85	94	kHz
Maximum Duty Cycle	D_{MAX}		65	75		%
Minimum Switching Frequency	f_{MIN}	ACT413		1164		Hz
		ACT413A		550		

ELECTRICAL CHARACTERISTICS CONT'D

V_{DD} = 13V, L_M = 0.56mH, R_{CS} = 1.05Ω, V_{OUT} = 5V, N_P = 56, N_S = 5, N_A = 13, T_A = 25°C, unless otherwise specified,5V2.4A application.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Protection						
CS Short Waiting Time			2	2.25	3	μs
CS Short Detection Threshold				0.1	0.15	V
CS Open Threshold Voltage				1.75		V
Abnormal OCP Blanking Time				190		ns
Inductance Short CS Threshold Voltage				1.75		V
Thermal Shutdown Temperature				135		˚C
Thermal Hysteresis				20		˚C
Line UVLO	I_{FBUVLO}			0.2		mA
Line UVLO Hysteresis				20		μA
Line OVP	I_{FBOVP}			2.4		mA
VFB Over Voltage Protection				3		V
Valley Detection						
Valley Detection Time Window		V_{COMP} = 0.45V		3.3		μs

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

ACT413/ACT413A is a high performance peak current mode low-voltage PWM controller IC. The controller includes the most advance features that are required in the adaptor applications up to 36 Watt. Unique fast startup, frequency fold back, QR switching technique, accurate OLP, low standby mode operation, external compensation adjustment, short winding protection, OCP, OTP, OVP and UVLO are included in the controller.

Startup

Startup current of ACT413/ACT413A is designed to be very low so that VDD could be charged to V_{DDON} threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, two 2MΩ, 1/8 W startup resistors could be used together with a VDD capacitor(4.7uF) to provide a fast startup and yet low power dissipation design solution.
During startup period, the IC begins to operate with minimum Ippk to minimize the switching stresses for the main switch, output diode and transformers. And then, the IC operates at maximum power output to achieve fast rise time. After this, V_{OUT} reaches about 90% V_{OUT}, the IC operates with a 'soft-landing' mode (decrease Ippk) to avoid output overshoot.

Constant Voltage (CV) Mode Operation

In constant voltage operation, the ACT413/ACT413A senses the output voltage at FB pin through a resistor divider network R5 and R6 in Figure 2. The signal at FB pin is pre-amplified against the internal reference voltage, and the secondary side output voltage is extracted based on Active-Semi's proprietary filter architecture.

This error signal is then amplified by the internal error amplifier. When the secondary output voltage is above regulation, the error amplifier output voltage decreases to reduce the switch current. When the secondary output voltage is below regulation, the error amplifier output voltage increases to ramp up the switch current to bring the secondary output back to regulation. The output regulation voltage is determined by the following relationship:

$$V_{OUTCV} = 2.20V \times (1 + \frac{R_{FB1}}{R_{FB2}}) \times \frac{N_S}{N_A} - V_D \qquad (1)$$

where R_{FB1} (R5) and R_{FB2} (R6) are top and bottom feedback resistor, N_S and N_A are numbers of transformer secondary and auxiliary turns, and V_D is the rectifier diode forward drop voltage at approximately 0.1A bias.

Constant Current (CC) Mode Operation

When the secondary output current reaches a level set by the internal current limiting circuit, the ACT413/ACT413A enters current limit condition and causes the secondary output voltage to drop. As the output voltage decreases, so does the flyback voltage in a proportional manner. An internal current shaping circuitry adjusts the switching frequency based on the flyback voltage so that the transferred power remains proportional to the output voltage, resulting
in a constant secondary side output current profile. The energy transferred to the output during each switching cycle is ½(LP × ILIM^2) × η, where LP is the transformer primary inductance, ILIM is the primary peak current, and η is the conversion efficiency. From this formula, the constant output current can be derived:

$$I_{OUTCC} = \frac{1}{2} \times L_p \times (\frac{V_{CS}}{R_{CS}})^2 \times (\frac{\eta \times f_{SW}}{V_{OUTCV}}) \qquad (2)$$

where f_{SW} is the switching frequency and V_{OUTCV} is the nominal secondary output voltage. The constant current operation typically extends down to lower than 40% of nominal output voltage regulation.

Standby (No Load) Mode

In no load standby mode, the ACT413/ACT413A oscillator frequency is further reduced to a minimum frequency while the current pulse is reduced to a minimum level to minimize standby power. The actual minimum switching frequency is programmable with an output preload resistor.

Loop Compensation

The ACT413/ACT413A allows external loop compensation by connecting a capacitor to extend its applications, especially with different V_{OUT} in a wide output power range.

Primary Inductance Compensation

The ACT413/ACT413A integrates a built-in primary inductance compensation circuit to maintain constant OLP despite variations in transformer manufacturing. The compensated ranges is +/-7%.

FUNCTIONAL DESCRIPTION CONT'D

Primary Inductor Current Limit Compensation

The ACT413/ACT413A integrates a primary inductor peak current limit compensation circuit to achieve constant OLP over wide line and wide load range.

Output Cable Resistance Compensation

The ACT413/ACT413A provides internal programmable output cable resistance compensation during constant voltage regulation, monotonically adding an output voltage correction up to predetermined percentage at full power.

The feature allows better output voltage accuracy by compensating for the output voltage drop due to the output cable resistance.

Frequency Fold-back

When the load drops to 75% of full load level, ACT413/ACT413A starts to decrease the switching frequency, which is proportional to the load current ,to improve the efficiency of the converter as show in Functional Block Diagram.

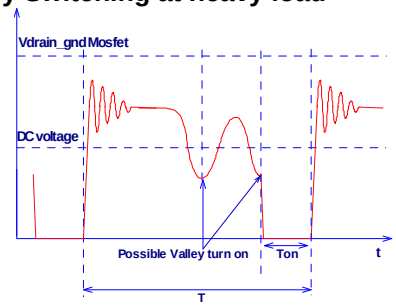
This enables the application to meet all latest green energy standards. The actual minimum switching frequency is programmable with a small dummy load (while still meeting standby power).

Valley Switching

ACT413/ACT413A employed valley switching from medium load to heavy load to reduce switching loss and EMI. After the switch is turned off, the ringing voltage from the auxiliary winding is applied to the VFB pin through feedback network R5, R6. Internally, the VFB pin is connected to an zero-crossing detector to generate the switch turn on signal when the conditions are met. In light load, the frequency fold back scheme starts to take control to determine the switch turn on signal, so thus the switching frequency.

Figure 1:

Valley Switching at heavy load



Protection Features

The ACT413/ACT413A provides full protection functions. The following table summarizes all protection functions.

PROTECTION FUNCTIONS	FAILURE CONDITION	PROTECTION MODE
V_{DD} Over Voltage	V_{DD} > 20.5V (4 duty cycle)	Auto Restart
VFB Over Voltage	V_{FB} > 3V (4 duty cycle)	Auto Restart
Over Temperature	T > 135°C	Auto Restart
Short Winding/ Short Diode	V_{CS} > 1.75V	Auto Restart
Over Load	IPK = I_{LIMIT}	Auto Restart
Output Short Circuit	V_{FB} < 0.56V	Auto Restart
Open Loop	No switching for 4 cycle	Auto Restart
V_{CC} Under Voltage	V_{CC} < 6.8V	Auto Restart

Auto-Restart Operation

ACT413/ACT413A will enter auto-restart mode when a fault is identified. There is a startup phase in the auto-restart mode. After this startup phase the conditions are checked whether the failure is still present. Normal operation proceeds once the failure mode is removed. Otherwise, new startup phase will be initiated again.

To reduce the power loss during fault mode, the startup delay control is implemented. The startup delay time increases over lines.

Over Load Protection (OLP)

When the secondary output current reaches a level set by the internal current limiting circuit, the ACT413/ACT413A enters current limit condition and causes the secondary output voltage to drop, the IC enters fault mode and enter auto restart mode.

ACT413/ACT413A is able to achieve very accurate OLP (constant I_{OUT}) independent of input lines and primary inductor values.

Short Circuit Protection

When the secondary side output is short circuited, the ACT413/ACT413A enters hiccup mode

TYPICAL APPLICATION CONT'D

operation. This hiccup behavior continues until the short circuit is removed.

FB Over Voltage Protection

The ACT413/ACT413A includes output over-voltage protection circuitry, which shuts down the IC when the output voltage is 40% above the normal regulation voltage 4 consecutive switching cycles. The ACT413/ACT413A enters hiccup mode when an output over voltage fault is detected.

VDD Over Voltage Protection

ACT413/ACT413A can monitor the converter output voltage. The voltage generated by the auxiliary winding tracks converter's output voltage through VDD, which is in proportion to the turn ratio $(V_{OUT}+V_{DIODE})$ xN_A/N_S. When the V_{OUT} is abnormally higher than design value for four consecutive cycles, IC will enter the restart process. A counter is used to reduce sensitivity to noise and prevent the auto start unnecessary.

Open Loop Protection

ACT413/ACT413A is able to protect itself from damage when the control loop is open. The typical open loop condition includes either VFB floating or RFB5 open.

Over Temperature Shutdown

The thermal shutdown circuitry detects the ACT413/ACT413A die temperature. The threshold is set at typical 135˚C. When the die temperature rises above this threshold (135˚C) the ACT413/ACT413A is disabled and remains disabled until the die temperature falls below 115˚C, at which point the ACT413/ACT413A is re-enabled.

TYPICAL APPLICATION CONT'D

Design Example

The design example below gives the procedure for a DCM fly back converter using an ACT413/ACT413A. Refer to Application Circuit Figure 2, the design for an adapter application starts with the following specification:

Input Voltage Range	90VAC - 265VAC, 50/60Hz
Output Power, P_O	12W
Output Voltage, V_{OUTCV}	5V
Full Load Current, I_{OUTFL}	2.4A
CC Current, I_{OUTMAX}	2.4-3A
System Efficiency CV, η	0.81

The operation for the circuit shown in Figure 1 is as follows: the rectifier bridge BD1 and the capacitor C1/C2 convert the AC line voltage to DC. This voltage supplies the primary winding of the transformer T1 and the startup resistor R7/R8 to VDD pin of ACT413/ACT413A and C4. The primary power current path is formed by the transformer's primary winding, the mosfet, and the current sense resistor R9. The resistors R3, R2, diode D2 and capacitor C3 create a snubber clamping network that protects Q1 from voltage spike from the transformer primary winding leakage inductance. The network consisting of capacitor C4, diode D3 and resistor R4 provides a VDD supply voltage for ACT413/ACT413A from the auxiliary winding of the transformer. The resistor R4 is optional, which filters out spikes and noise to makes VDD more stable. C4 is the decoupling capacitor of the supply voltage and energy storage component for startup. During power startup, the current charges C4 through startup resistor R7/R8 from the rectified high voltage. The diode D4 and the capacitor C7/C6 rectify filter the output voltage. The resistor divider consists of R5 and R6 programs the output voltage.

Since a bridge rectifier and bulk input capacitors are used, the resulting minimum and maximum DC input voltages can be calculated:

$$V_{INDC\_MIN} = \sqrt{2V_{INAC\_MIN}^2 - \frac{2P_{OUT}(\frac{1}{2f_L} - t_C)}{\eta \times C_{IN}}} = \sqrt{2 \times 85^2 - \frac{2 \times 12 \times (\frac{1}{2 \times 47} - 3.5ms)}{0.81 \times 25\,\mu F}} \approx 80V \quad (3)$$

$$V_{IN(MAX)DC} = \sqrt{2} \times V_{IN(MAX)AC} = \sqrt{2} \times (265\,V_{AC}) = 375\,V \quad (4)$$

Where η is the estimated circuit efficiency, f_L is the line frequency, t_C is the estimated rectifier conduction time, C_{IN} is empirically selected to be 10μF+15μF electrolytic capacitors.

The maximum duty cycle is set to be 40% at low line voltage 85VAC and the circuit efficiency is estimated to be 81%. Then the maximum average input current is:

$$I_{IN\_MAX} = \frac{V_{OUT} \times I_{OUT\_FL}}{V_{INDC\_MIN} \times \eta} = \frac{5 \times 2.4}{80 \times 0.81} = 185\ mA \quad (5)$$

The maximum input primary peak current:

$$I_{LIM} = \frac{2 \times L_{IN}}{D_{MAX}} = \frac{2 \times 185}{0.4} = 925\ mA \quad (6)$$

The primary inductance of the transformer:

$$L_p = \frac{V_{INDC\_MIN} D_{max}}{I_{LIM} \times f_s} = \frac{80 \times 0.4}{925\ mA \times 65\ k} \approx 0.56\ mH \quad (7)$$

The maximum primary turns on time:

$$T_{ON\_MAX} = L_p \frac{I_{LIM}}{V_{INDC\_MIN}} = \frac{0.56\,mH \times 925\,mA}{80} = 6.48\,\mu s \quad (8)$$

The ringing periods from primary inductance with mosfet Drain-Source capacitor:

$$T_{RINGING\_MAX} = 2\pi\sqrt{L_{p\_MAX} C_{DS\_MAX}} = 2 \times 3.14 \times \sqrt{0.56mH \times (1+7\%) \times 100PF} = 1.54\,\mu s \quad (9)$$

Design only an half ringing cycle at maximum load in minimum low line, so secondly reset time:

$$T_{RST} = T_{SW} - T_{ON\_MAX} - 0.5T_{RINGING\_MAX} = 1/65kHz - 6.48\,\mu s - 0.5 \times 1.54\,\mu s = 8.13\,\mu s \quad (10)$$

Base on conservation of energy and transformer transform identity, the primary to secondary turns ratio N_P/N_S:

$$\frac{N_P}{N_S} = \frac{T_{ON}}{T_{RST}} \times \frac{V_{IN\_MIN}}{V_{OUT} + V_D} = \frac{6.48}{8.13} \times \frac{80}{5 + 0.45} = 11.7 \quad (11)$$

The auxiliary to secondary turns ratio N_A/N_S:

$$\frac{N_A}{N_S} = \frac{V_{DD} + V_D'}{V_{OUT} + V_D} = \frac{13 + 0.45}{5 + 0.45} = 2.47 \quad (12)$$

TYPICAL APPLICATION CONT'D

An EE13++ core is selected for the transformer for small PCB size. From the manufacture's catalogue recommendation, the gapped core with an effective inductance A_{LE} of 18 nH/T^2 is selected. The turn of the primary winding is:

$$N_P = \sqrt{\frac{L_P}{A_{LE}}} = \sqrt{\frac{0.56\,mH}{18\,nH\ /\ T^2}} \approx 56\,T \qquad (13)$$

The turns of secondary and auxiliary winding can be derived accordingly:

$$N_S = \frac{N_s}{N_p} \times N_p = \frac{1}{11.7} \times 56 \approx 5\,T \qquad (14)$$

$$N_A = \frac{N_A}{N_S} \times N_s = 2.47 \times 5 \approx 13\,T \qquad (15)$$

Determining the value of the current sense resistor (R9) uses the peak current in the design. Since the ACT413/ACT413A internal current limit is set to 1V, the design of the current sense resistor is given by:

$$R_{CS} = \frac{V_{CS}}{\sqrt{\frac{2 \times I_{OUT\_OCP} \times V_{OUT}}{L_P \times F_{MAX} \times \eta_{system}}}} = \frac{1}{\sqrt{\frac{2 \times 3 \times 5}{0.56\,mH \times 75\,kHz \times 0.81}}} \approx 1.05.\Omega \qquad (16)$$

The voltage feedback resistors are selected according to the Ioccmax and Vo. The design Io_cc max is given by:

$$f_s = \frac{N_p}{N_s} \times \frac{R_{fb1} \times R_{fb2}}{R_{fb1} + R_{fb2}} \times \frac{V_O + V_D}{L_p \times \frac{V_{cs}}{R_{cs}} \times K_{f\_sw}} \qquad (17)$$

The design Vo is given by:

$$V_o = (1 + \frac{R_{fb1}}{R_{fb2}}) \times \frac{N_s}{N_a} \times V_{FB} - V_D \qquad (18)$$

Where k is IC constant and K=0.000022, then we can get the value:

$$R_{fb1} = 56.2K, R_{fb2} = 11.3K \qquad (19)$$

When selecting the output capacitor, a low ESR electrolytic capacitor is recommended to minimize ripple from the current ripple. The approximate equation for the output capacitance value is given by:

$$C_{OUT} = \frac{I_{OUT}}{f_{sw} \times V_{RIPPLE}} = \frac{2.4}{80\,k \times 50\,mV} = 600\ \mu F \qquad (20)$$

Two 680µF electrolytic capacitors are used to keep the ripple small.

PCB Layout Guideline

Good PCB layout is critical to have optimal performance. Decoupling capacitor (C4) and feedback resistor (R5/R6) should be placed close to VDD and FB pin respectively. There are two main power path loops. One is formed by C1/C2, primary winding, Mosfet transistor and current sense resistor (R9). The other is secondary winding, rectifier D4 and output capacitors (C7/C6). Keep these loop areas as small as possible. Connecting high current ground returns, the input capacitor ground lead, and the ACT413/ACT413A GND pin to a single point (star ground configuration).

Figure 2:

ACT413/ACT413A, Universal VAC Input, 5V/2.4A Output Charger

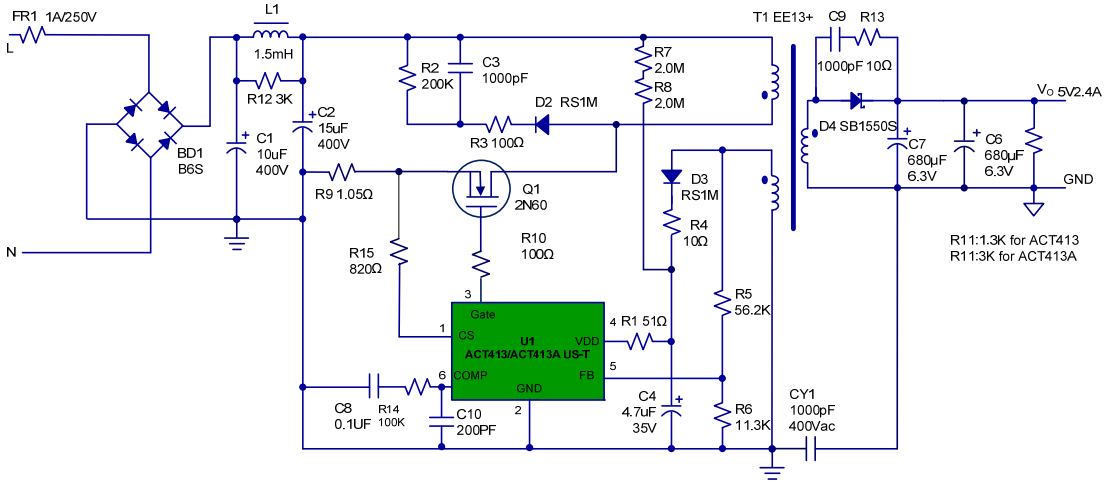
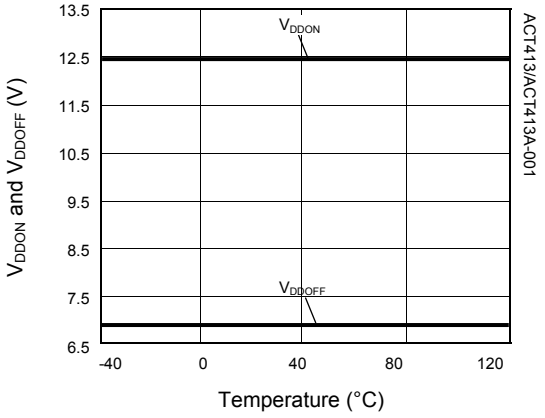


Table 1: **ACT413/ACT413A Bill of Materials**

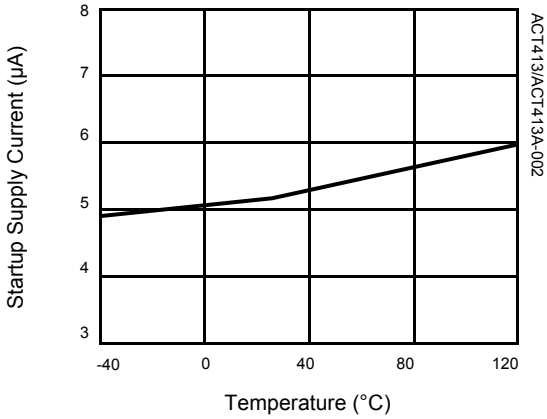
ITEM	REFERENCE	DESCRIPTION	QTY	MANUFACTURER
1	U1	IC, ACT413/ACT413A,SOT23-6	1	Active-Semi.
2	C1	Capacitor, Electrolytic, 10μF/400V, 10x15mm	1	KSC
3	C2	Capacitor, Electrolytic, 15μF/400V, 10x15mm	1	KSC
4	C3	Capacitor, Ceramic, 1000pF/500V, 0805,SMD	1	POE
5	C4	Capacitor, Electrolytic,4.7μF/35V,5x11mm	1	KSC
6	C6,C7	Capacitor, Electrolytic, 820μF/6.3V, 6.3 × 16mm	2	KSC
7	C8	Capacitor, Ceramic, 0.1μF/25V, 0805,SMD	1	POE
8	C9	Capacitor, Ceramic, 1000pF/100V, 0805,SMD	1	POE
9	C10	Capacitor, Ceramic, 200pF/50V, 0805,SMD	1	POE
10	CY1	Safety Y1,Capacitor,1000pF/400V,Dip	1	UXT
11	BD1	Bridge Rectifier,D1010S,1000V/1.0A,SDIP	1	PANJIT
12	D2,D3	Fast Recovery Rectifier, RS1M,1000V/1.0A, RMA	2	PANJIT
13	D4	Diode, Schottky, 50V/15A, S15U50S, SMD	1	Vishay
14	L1	Axial Inductor, 1.5mH, 5*7,Dip	1	SoKa
15	L2	Axial Inductor, 0.55*5T, 5*7,Dip	1	SoKa
16	Q1	Mosfet Transistor, 2N60,TO-251	1	Infineon
17	PCB1	PCB, L*W*T=40x28x1.6mm,Cem-1,Rev:A	1	Jintong
18	FR1	Fuse,1A/250V	1	TY-OHM
19	R2	Carbon Resistor, 200KΩ, 1206, 5%	1	TY-OHM
20	R3,R10	Chip Resistor, 100Ω, 0805, 5%	2	TY-OHM
21	R1	Chip Resistor, 51Ω, 0805, 5%	1	TY-OHM
22	R4,R13	Chip Resistor, 10Ω, 0805, 5%	2	TY-OHM
23	R5	Chip Resistor, 56.2KΩ, 0805,1%	1	TY-OHM
24	R6	Chip Resistor, 11.3KΩ, 0805, 1%	1	TY-OHM
25	R7,R8	Chip Resistor, 2MΩ, 0805 , 5%	2	TY-OHM
26	R9	Chip Resistor, 1.05Ω, 1206,1%	1	TY-OHM
27	R11	Chip Resistor, 1.3KΩ (ACT413)/3KΩ (ACT413A), 0805 , 5%	1	TY-OHM
28	R15	Chip Resistor, 820Ω, 0805 , 5%	1	TY-OHM
29	R12	Chip Resistor, 3KΩ, 0805 , 5%	1	TY-OHM
30	R14	Chip Resistor, 100KΩ, 0805, 5%	1	TY-OHM
31	T1	Transformer, Lp=0.56mH, EE13++	1	

TYPICAL PERFORMANCE CHARACTERISTICS

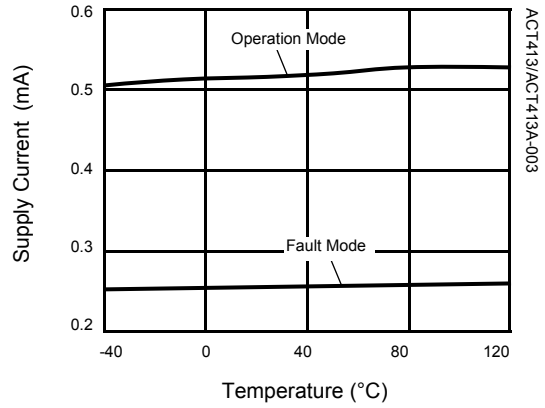
VDD ON/OFF Voltage vs. Temperature



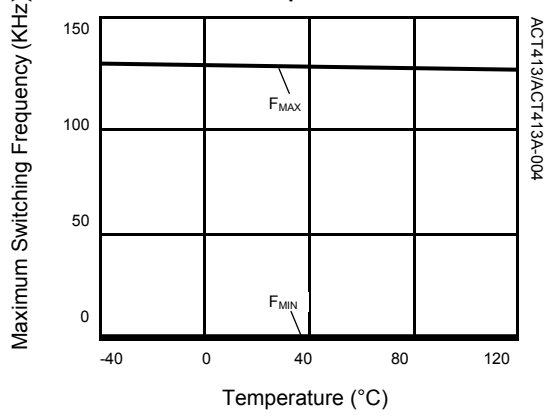
Startup Supply Current vs. Temperature



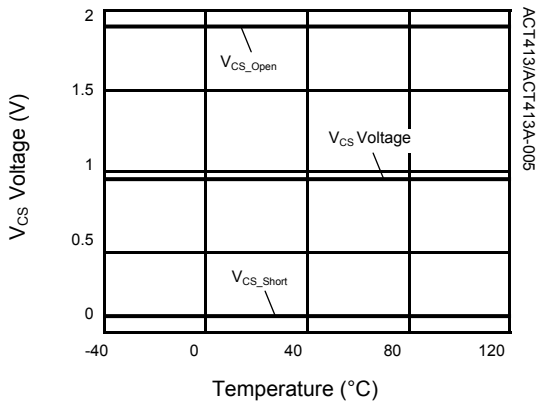
Supply Current at Operation/Fault Mode vs. Temperature



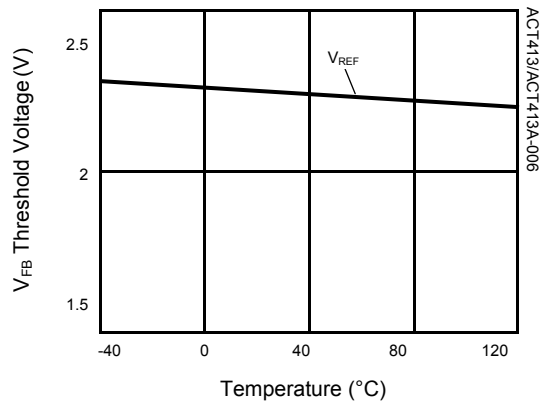
Maximum/Minimum Switching Frequency vs. Temperature



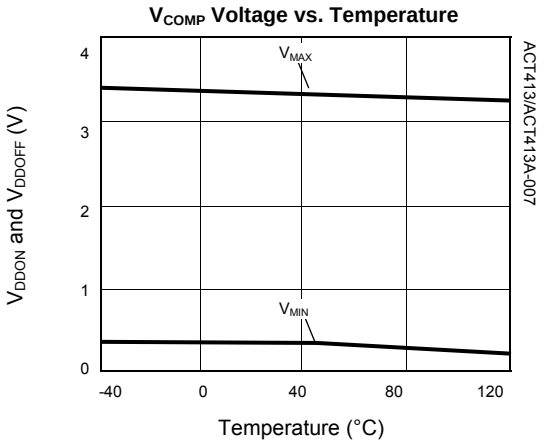
V_{CS} Voltage vs. Temperature



V_{FB} Threshold Voltage vs. Temperature

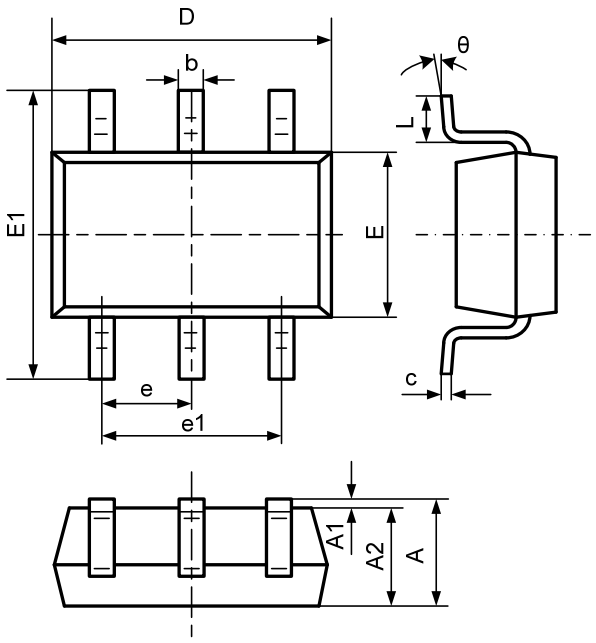


TYPICAL PERFORMANCE CHARACTERISTICS



PACKAGE OUTLINE

SOT23-6 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	-	1.45	-	0.057
A1	0	0.15	0.000	0.006
A2	0.9	1.3	0.035	0.051
b	0.3	0.5	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.9 BSC		0.114 BSC	
E	1.6 BSC		0.063 BSC	
E1	2.8 BSC		0.110 BSC	
e	0.95 BSC		0.037 BSC	
e1	1.9 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°