

1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	On-state rms current (full sine wave)	TO-220FPAB	$T_c = 102\text{ °C}$	4	A
		DPAK	$T_c = 112\text{ °C}$		
		DPAK with 0.5 cm copper	$T_{amb} = 60\text{ °C}$	1	
I_{TSM}	Non repetitive surge peak on-state current T_j initial = 25 °C, (full cycle sine wave)	f = 50 Hz	$t_p = 20\text{ ms}$	32	A
		f = 60 Hz	$t_p = 16.7\text{ ms}$	30	
I^2t	I^2t for fuse selection		$t_p = 10\text{ ms}$	6	A ² s
dI/dt	Critical rate of rise on-state current $I_G = 2 \times I_{GT}$, $t_r \leq 100\text{ ns}$	f = 120 Hz	$T_j = 125\text{ °C}$	100	A/ μ s
$V_{PP}^{(1)}$	Non repetitive line peak pulse voltage ⁽¹⁾		$T_j = 25\text{ °C}$	2	kV
$P_{G(AV)}$	Average gate power dissipation		$T_j = 125\text{ °C}$	0.1	W
P_{GM}	Peak gate power dissipation ($t_p = 20\text{ }\mu$ s)		$T_j = 125\text{ °C}$	10	W
I_{GM}	Peak gate current ($t_p = 20\text{ }\mu$ s)		$T_j = 125\text{ °C}$	1.6	A
T_{stg}	Storage temperature range			-40 to +150	°C
T_j	Operating junction temperature range			-40 to +125	°C
T_L	Lead temperature for soldering during 10 s (at 3 mm from plastic case)			260	°C
V_{ins}	Insulation rms voltage (60 seconds)			2000	V

1. according to test described by standard IEC 61000-4-5, see Figure 17 for conditions

Table 2. Electrical characteristics ($T_j = 25\text{ °C}$, unless otherwise specified)

Symbol	Test conditions	Quadrant		Value		Unit
				ACST410	ACST435	
$I_{GT}^{(1)}$	$V_{OUT} = 12\text{ V}$, $R_L = 33\text{ }\Omega$	I - II - III	Max.	10	35	mA
V_{GT}			Max.	1.0	1.1	V
V_{GD}	$V_{OUT} = V_{DRM}$, $R_L = 3.3\text{ k}\Omega$, $T_j = 125\text{ °C}$	I - II - III	Min.	0.2		V
$I_H^{(2)}$	$I_{OUT} = 500\text{ mA}$		Max.	20	25	mA
I_L	$I_G = 1.2 \times I_{GT}$	I - II - III	Max.	40	60	mA
dV/dt ⁽²⁾	$V_{OUT} = 67\% V_{DRM}$, gate open, $T_j = 125\text{ °C}$		Min.	500	1000	V/ μ s
(dI/dt) _c ⁽²⁾	Without snubber, $T_j = 125\text{ °C}$		Min.		5	A/ms
(dI/dt) _c ⁽²⁾	(dV/dt) _c = 15 V/ μ s, $T_j = 125\text{ °C}$		Min.	2		A/ms
V_{CL}	$I_{CL} = 0.1\text{ mA}$, $t_p = 1\text{ ms}$		Min.	850		V

1. Minimum I_{GT} is guaranteed at 5% of $I_{GT\text{ max}}$

2. For both polarities of OUT pin referenced to COM pin

Table 3. Static characteristics

Symbol	Test conditions			Value	Unit
$V_{TM}^{(1)}$	$I_{OUT} = 5.6 \text{ A}$, $t_p = 500 \mu\text{s}$	$T_j = 25 \text{ }^\circ\text{C}$	Max.	1.7	V
$V_{T0}^{(1)}$	Threshold voltage	$T_j = 125 \text{ }^\circ\text{C}$	Max.	0.9	V
$R_D^{(1)}$	Dynamic resistance	$T_j = 125 \text{ }^\circ\text{C}$	Max.	110	mΩ
I_{DRM}	$V_{OUT} = V_{DRM}/V_{RRM}$	$T_j = 25 \text{ }^\circ\text{C}$	Max.	20	μA
I_{RRM}		$T_j = 125 \text{ }^\circ\text{C}$		0.5	mA

1. For both polarities of OUT pin referenced to COM pin

Table 4. Thermal characteristics

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case for full cycle sine wave conduction	DPAK	2.6	$^\circ\text{C/W}$
		TO-220FPAB	4.6	
$R_{th(j-a)}$	Junction to ambient	TO-220FPAB	60	
	Junction to ambient, $S_{CU} = 0.5 \text{ cm}^2$ ⁽¹⁾	DPAK	70	

1. S_{CU} = copper surface under tab

1.1 Characteristics (curves)

Figure 1. Maximum power dissipation versus RMS on-state current

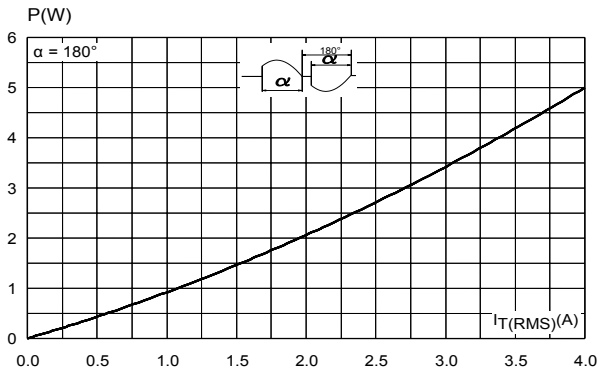


Figure 2. On-state RMS current versus case temperature (full cycle)

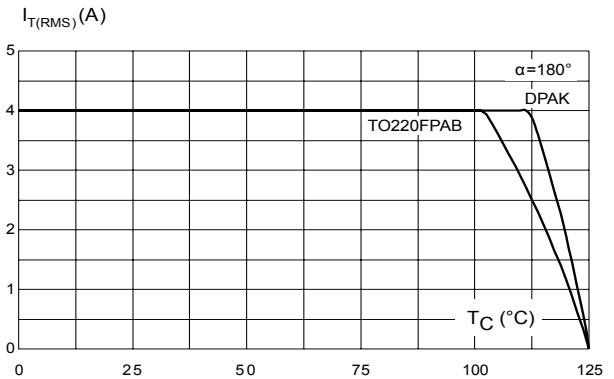


Figure 3. On-state RMS current versus ambient temperature (free air convection, full cycle)

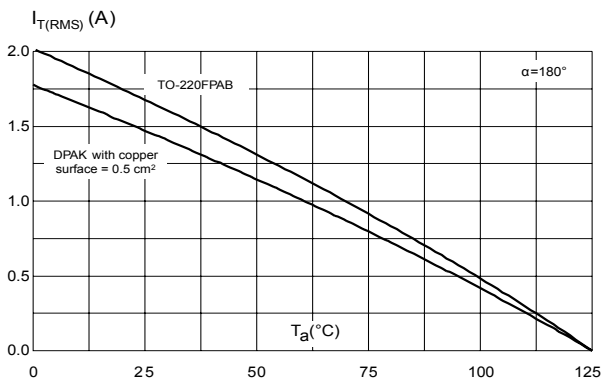


Figure 4. Relative variation of thermal impedance junction to case versus pulse duration

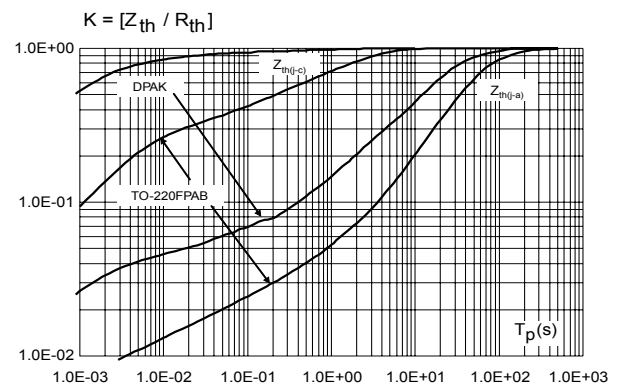


Figure 5. Relative variation of gate trigger current and gate trigger voltage versus junction temperature (typical values)

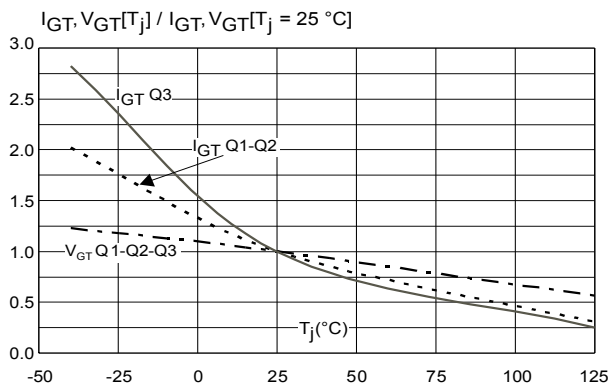


Figure 6. Relative variation of holding current and latching current versus junction temperature (typical values)

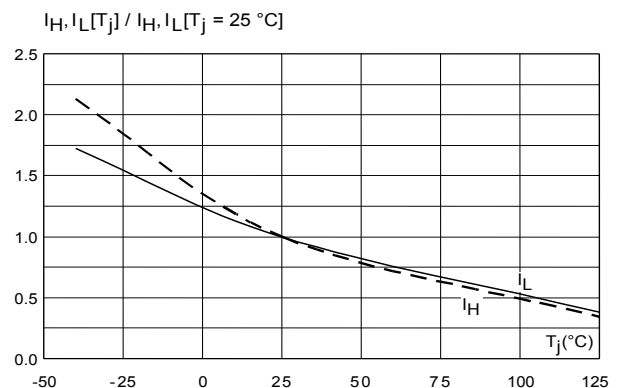


Figure 7. Surge peak on-state current versus number of cycles

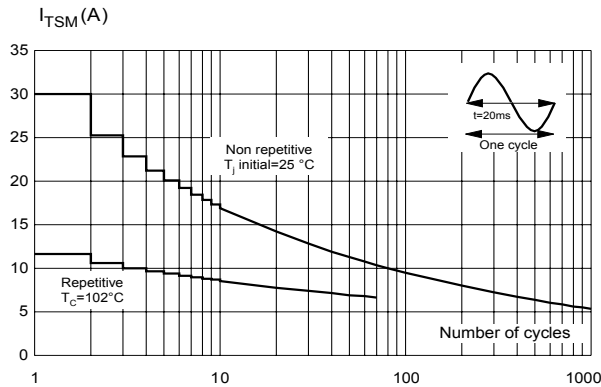


Figure 8. Non repetitive surge peak on-state current for a sinusoidal pulse width

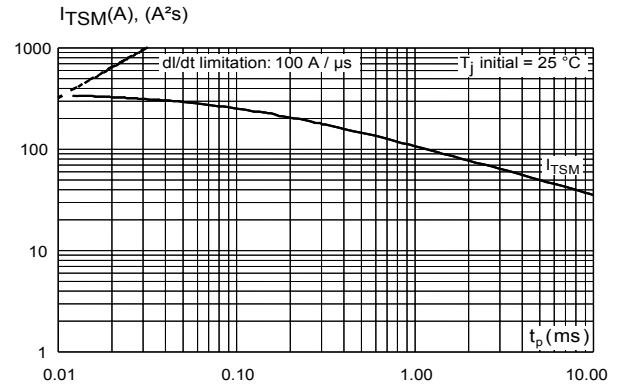


Figure 9. On-state characteristics (maximum values)

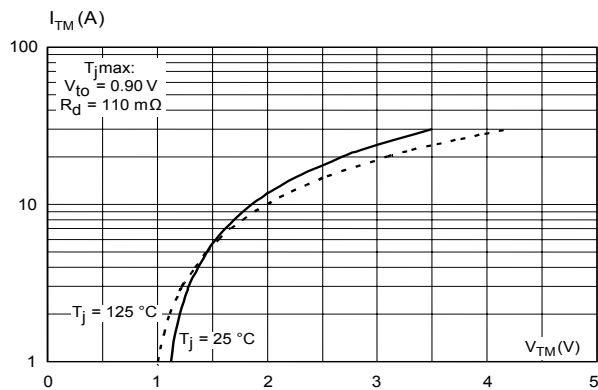


Figure 10. Relative variation of critical rate of decrease of main current (di/dt)_c versus junction temperature

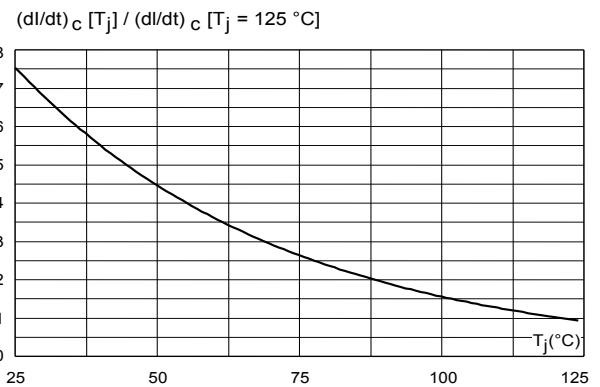


Figure 11. Relative variation of static dV/dt immunity versus junction temperature (gate open)

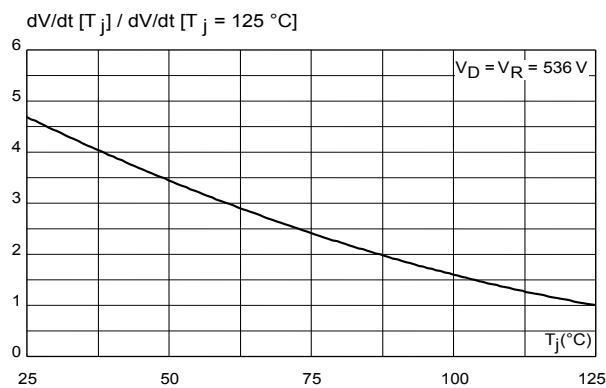


Figure 12. Relative variation of Leakage current versus junction temperature

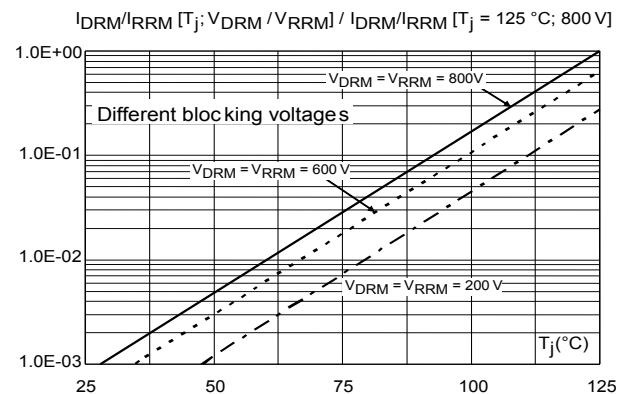


Figure 13. Relative variation of the clamping voltage versus junction temperature (minimum values)

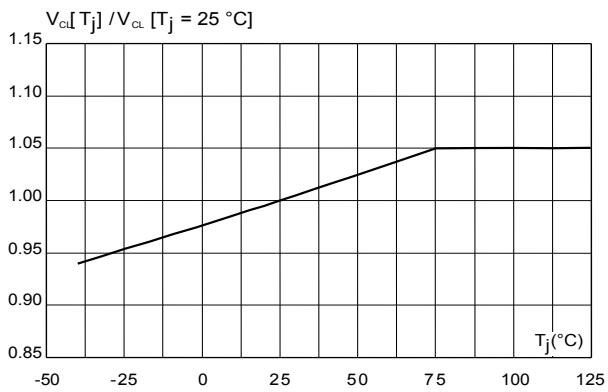
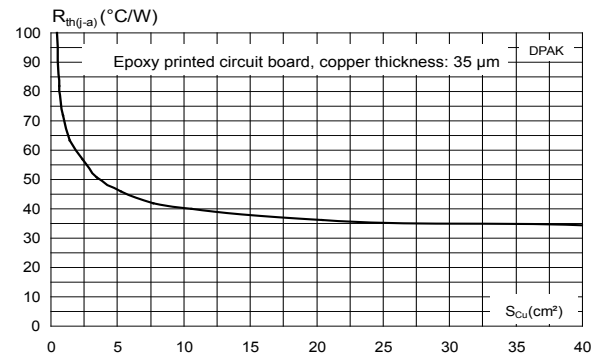


Figure 14. Thermal resistance junction to ambient versus copper surface under tab (typical values)



2 Application information

2.1 Typical application descriptions

The ACST4 device has been designed to control medium power load, such as AC motors in home appliances. Thanks to its thermal and turn off commutation performances, the ACST4 switch is able to drive an inductive load up to 4 A with no turn off additional snubber. It also provides high thermal performances in static and transient modes such as the compressor inrush current or high torque operating conditions of an AC motor. Thanks to its low gate triggering current level, the ACST4 can be driven directly by an MCU through a simple gate resistor as shown Figure 15 and Figure 16.

Figure 15. Compressor control – typical diagrams

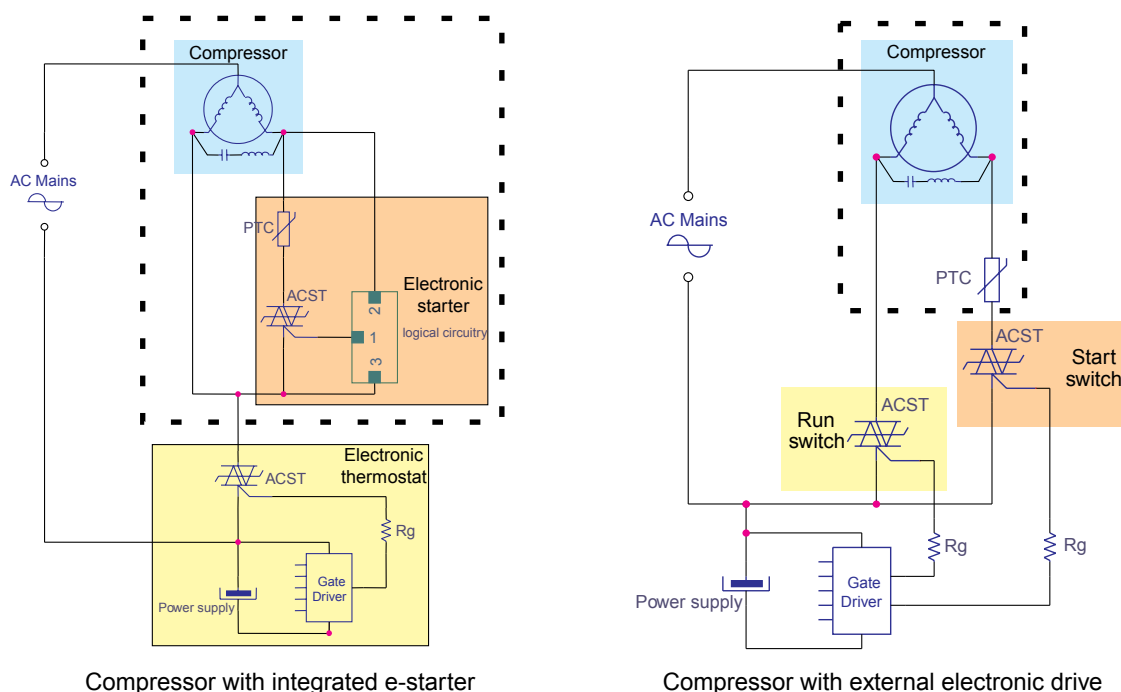
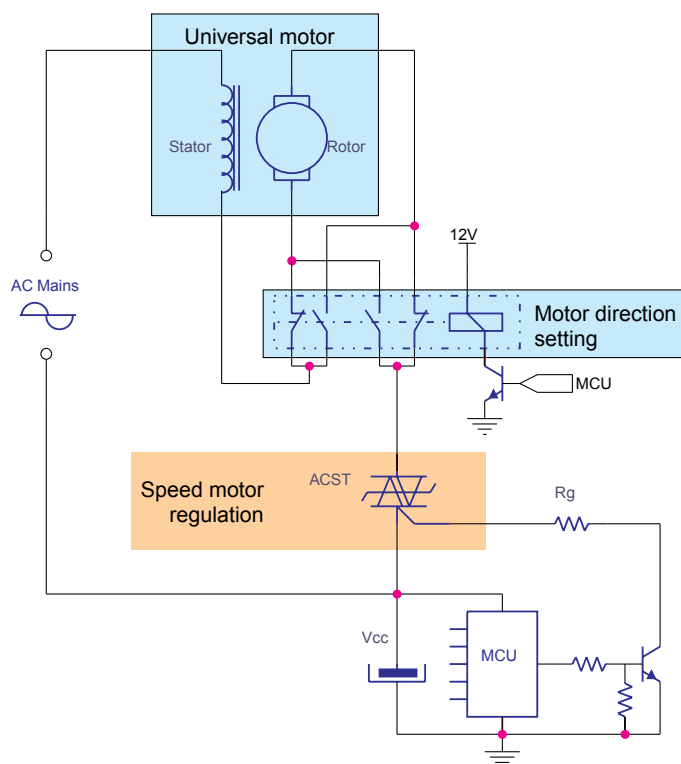


Figure 16. Universal drum motor control – typical diagram



2.2 AC line transient voltage ruggedness

In comparison with standard Triacs, which are not robust against surge voltage, the ACST4 is self-protected against over-voltage, specified by the new parameter V_{CL} . The ACST4 switch can safely withstand AC line transient voltages either by clamping the low energy spikes, such as inductive spikes at switch off, or by switching to the on state (for less than 10 ms) to dissipate higher energy shocks through the load. This safety feature works even with high turn-on current ramp up.

The test circuit of represents the ACST4 application, and is used to stress the ACST switch according to the IEC 61000-4-5 standard conditions. With the additional effect of the load which is limiting the current, the ACST switch withstands the voltage spikes up to 2 kV on top of the peak line voltage. The protection is based on an overvoltage crowbar technology. The ACST4 folds back safely to the on state as shown in . The ACST4 recovers its blocking voltage capability after the surge and the next zero current crossing.

Such a non repetitive test can be done at least 10 times on each AC line voltage polarity.

Figure 17. Overvoltage ruggedness test circuit for resistive and inductive loads for IEC 61000-4-5 standards

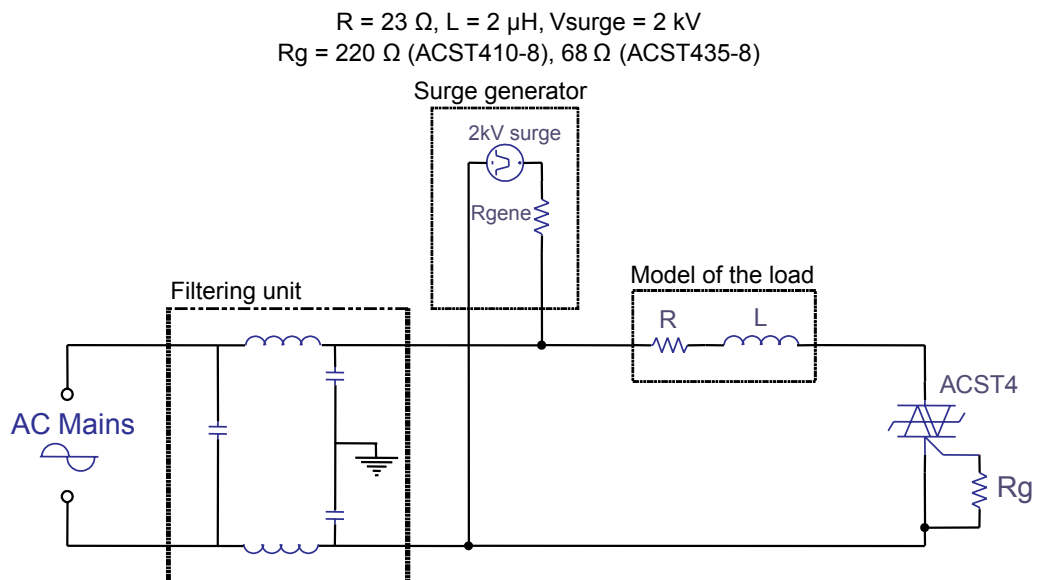
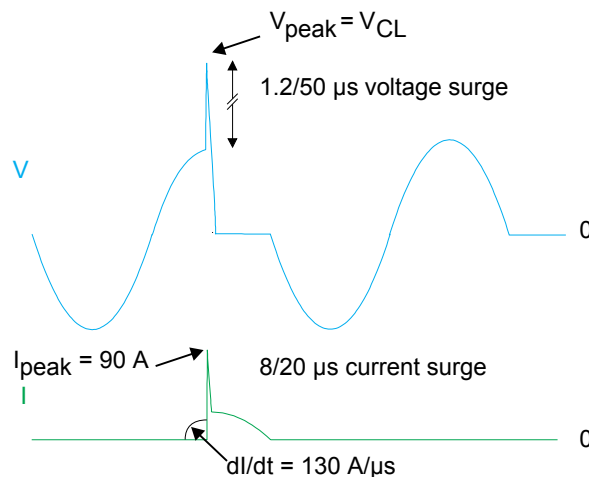


Figure 18. Typical voltage and current waveforms across the ACST4 during IEC 61000-4-5 standard test



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 TO-220FPAB package information

- Epoxy meets UL94, V0
- Recommended torque: 0.4 to 0.6 N·m

Figure 19. TO-220FPAB package outline

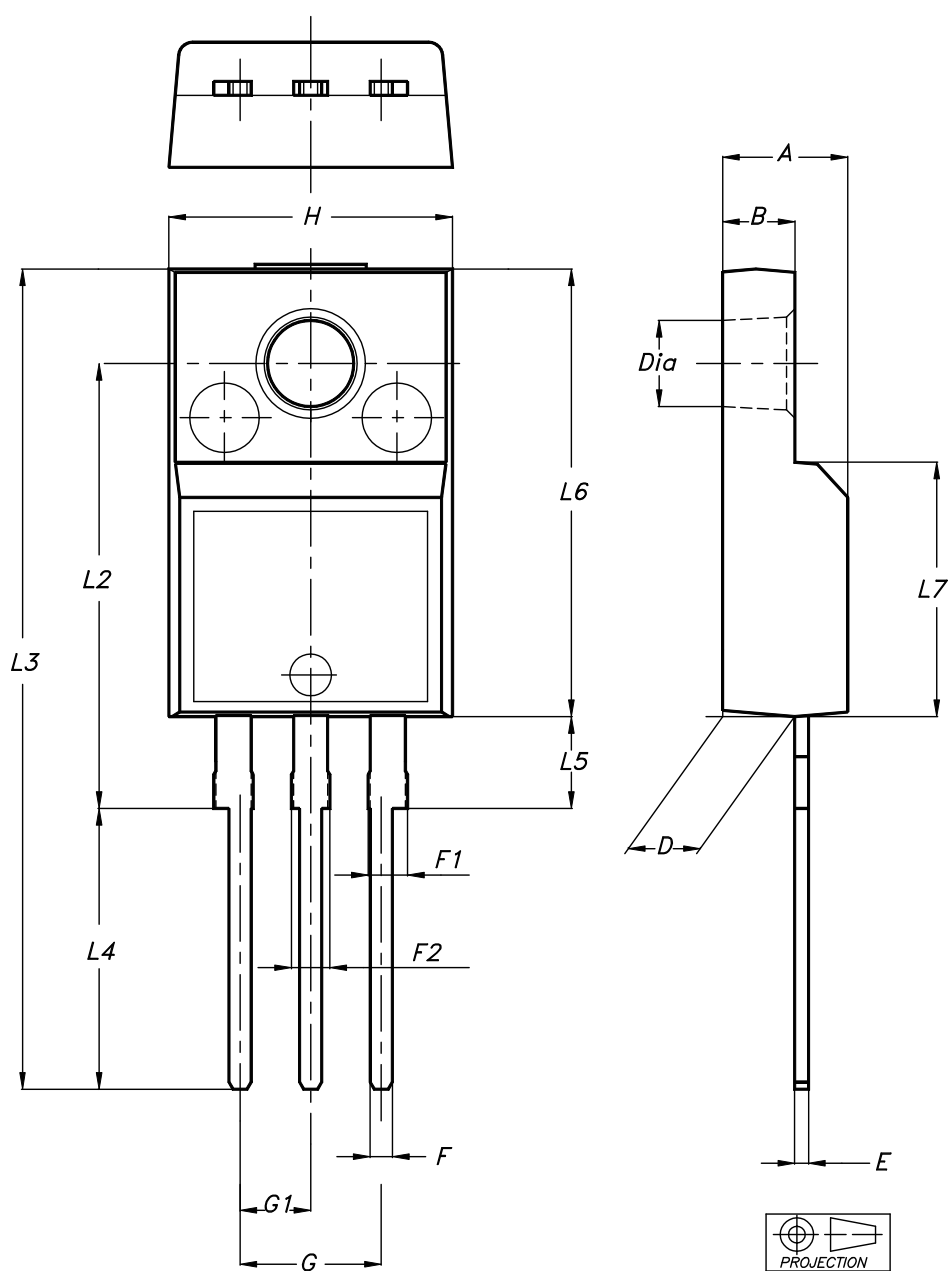


Table 5. TO-220FPAB package mechanical data

Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.40	4.60	0.1739	0.1818
B	2.5	2.7	0.0988	0.1067
D	2.50	2.75	0.0988	0.1087
E	0.45	0.70	0.0178	0.0277
F	0.75	1.0	0.0296	0.0395
F1	1.15	1.70	0.0455	0.0672
F2	1.15	1.70	0.0455	0.0672
G	4.95	5.20	0.1957	0.2055
G1	2.40	2.70	0.0949	0.1067
H	10.00	10.40	0.3953	0.4111
L2	16.00 typ.		0.6324 typ.	
L3	28.60	30.60	1.1304	1.2095
L4	9.80	10.6	0.3874	0.4190
L5	2.90	3.60	0.1146	0.1423
L6	15.90	16.40	0.6285	0.6482
L7	9.00	9.30	0.3557	0.3676
Dia	3.0	3.20	0.1186	0.1265

3.2 DPAK package information

- Molding compounded resin is halogen free and meets UL94 flammability standard, level V0
- Lead-free package leads plating

Figure 20. DPAK package outline

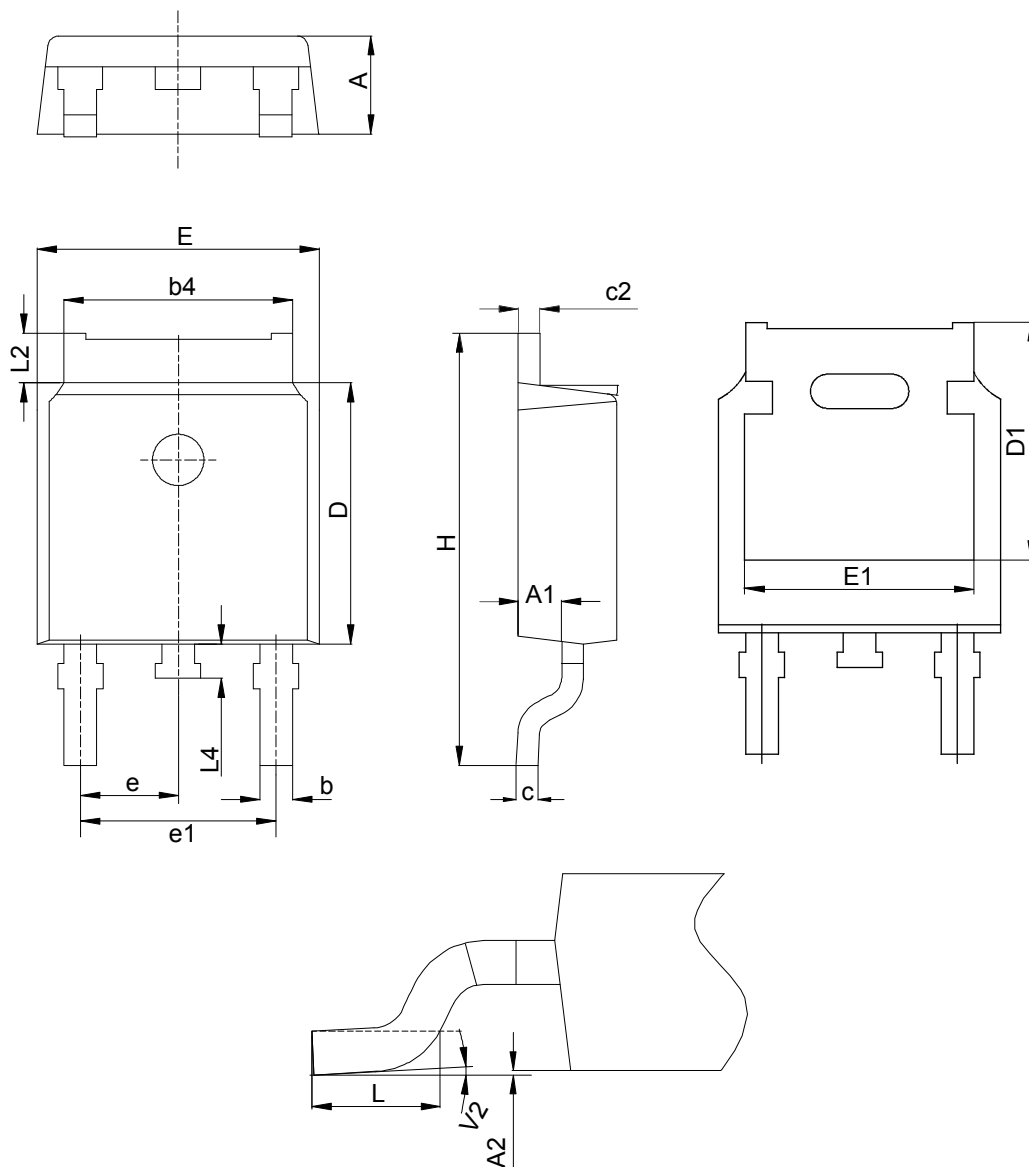


Table 6. DPAK package mechanical data

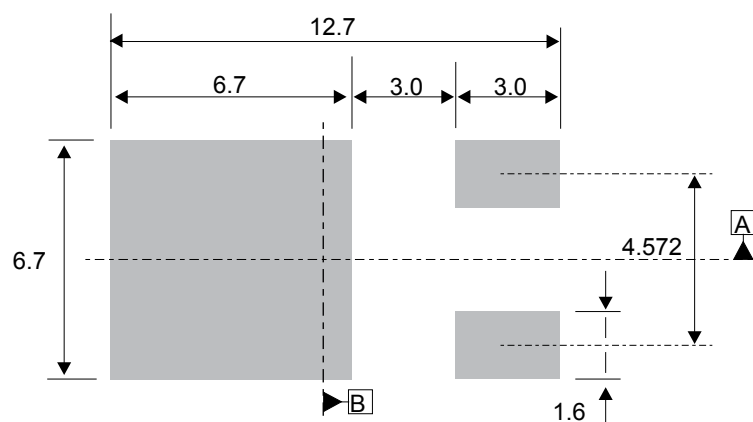
Ref.	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18		2.40	0.0858		0.0945
A1	0.90		1.10	0.0354		0.0433
A2	0.03		0.23	0.0012		0.0091
b	0.64		0.90	0.0252		0.354
b4	4.95		5.46	0.1949		0.2150
c	0.46		0.61	0.0181		0.0240
c2	0.46		0.60	0.0181		0.0236
D	5.97		6.22	0.2350		0.2449
D1	4.95		5.60	0.1949		0.2205
E	6.35		6.73	0.2500		0.2650
E1	4.32		5.50	0.1701		0.2165
e		2.286			0.0900	
e1	4.40		4.70	0.1732		0.1850
H	9.35		10.40	0.3681		0.4094
L	1.00		1.78	0.0394		0.0701
L2			1.27			0.0500
L4	0.60		1.02	0.0236		0.0402
V2 ⁽²⁾	-8°		+8°	-8°		+8°

1. Dimensions in inches are given for reference only

2. Degree

Note: This package drawing may slightly differ from the physical package. However, all the specified dimensions are guaranteed.

Figure 21. DPAK recommended footprint (dimensions are in mm)



The device must be positioned within $\oplus 0.05$ AB

4 Ordering information

Figure 22. Ordering information scheme

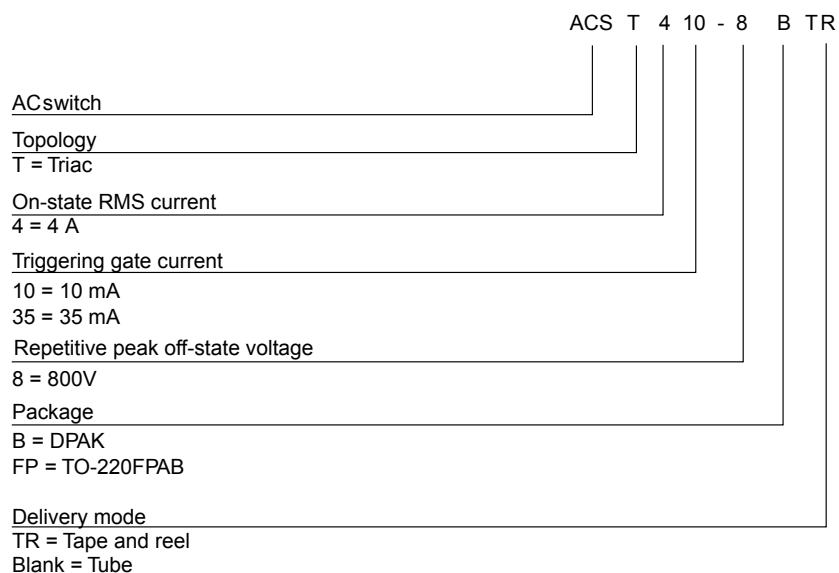


Table 7. Ordering information

Order code	Marking	Package	Weight	Base qty.	Packing mode
ACST410-8B	ACST4108	DPAK	1.5 g	50	Tube
ACST410-8BTR		DPAK		2500	Tape and reel
ACST410-8FP		TO-220FPAB	2.4 g	50	Tube
ACST435-8B	ACST4358	DPAK	1.5 g	50	Tube
ACST435-8BTR		DPAK		2500	Tape and reel
ACST435-8FP		TO-220FPAB	2.4 g	50	Tube

Revision history

Table 8. Document revision history

Date	Version	Changes
Jan-2003	3A	Previous update.
04-Jul-2007	4	Reformatted to current standard. Added package.
18-Dec-2009	5	V _{DRM} /V _{RRM} updated to 800 V. Order codes updated.
02-Jun-2014	6	Updated DPAK package information and reformatted to current standard.
21-Oct-2014	7	Updated Table 2, Table 3, Table 4, Features and Description.
18-May-2017	8	Updated Features in cover page, Table 2 and Figure 14.
19-Dec-2019	9	Update DPAK package information.
03-Sep-2020	10	Updated Table 7. Ordering information .
12-May-2021	11	Updated Features .
03-Aug-2021	12	Updated Table 7 .

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