A8501

2 MHz, 4 Channel×100 mA WLED/RGB Driver with Output Disconnect

FEATURES AND BENEFITS

- 600 kHz to 2.2 MHz switching frequency—ability to operate above the AM band
- Internal bias supply for single-supply operation (V_{IN} = 6.8 to 21 V)
- Boost converter with integrated 40 V DMOS switch and OVP–load-dump protection
- 3.5 µA shutdown current—limits battery drain
- Active current sharing between LED strings for 0.8% current matching and 0.7% accuracy
- Drive up to 9 series LEDs in 4 parallel strings, 36 LEDs maximum (V_f = 3.5 V, I_f = 100 mA)
- LED sinks rated for 100 mA each (400 mA total)
- PWM dimming with LED PWM duty cycle control
- 4000:1 dimming range
- Extensive fault mode protection schemes:
  - □ Shorted LED protection against misconnected loads—with true output disconnect
  - □ Open LED disconnect protects against LED failures
  - □ External thermistor sensing to limit LED temperature
  - □ Output overvoltage protection (OVP): 19.5 V default can be adjusted as high as 38 V
  - □ Open Schottky and open OVP resistor protection against external component failure
  - □ Input under- and overvoltage protection (UVLO and OVLO) against V_{IN} variation
  - □ Boost current limit, output short circuit limit, overtemperature protection (OTP), and soft start

PACKAGE:

28-pin TSSOP with exposed thermal pad (package LP)

Not to scale

DESCRIPTION

The A8501 is a multioutput WLED/RGB driver for backlighting medium-size displays. The A8501 integrates a boost converter and four 100 mA current sinks. LED channels can be tied together for up to 400 mA sink capability. It can work from a single power supply of 6.8 to 21 V and withstand up to 40 V. The boost converter is a constant frequency, current-mode converter.

Operating frequency can be set to 2 MHz in order to avoid interference with the AM radio band. The integrated boost DMOS switch is rated for 40 V at 3.6 A. PWM dimming allows LED currents to be controlled at up to a 1000:1 ratio. Additional 4:1 dimming can be achieved by using the DIM pin.

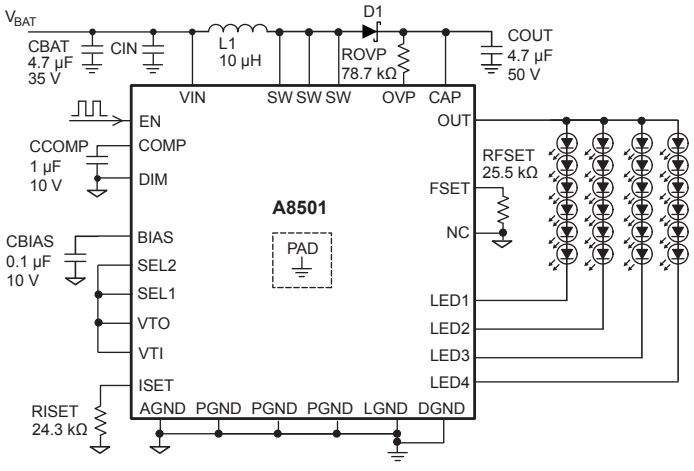
The A8501 provides protection against output connector shorts through an integrated output disconnect switch. An optional external thermistor can be used to limit LED current based on panel temperature.

The device is supplied in a surface mount, 28-pin TSSOP package (suffix LP), with exposed thermal pad for enhanced thermal dissipation. It is lead (Pb) free, with a leadframe plating choice of 100% matte-tin (suffix T) or tin-bismuth (suffix B).

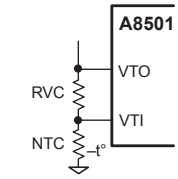
APPLICATIONS

- GPS navigation systems
- Automotive infotainment
- Back-up camera displays
- Cluster backlighting
- Portable DVD players
- Industrial LCD displays

Figure 1: LCD monitor backlight driving 4 LED strings. On/off and dimming control using ENABLE pin.
• Current = 50 mA per string
• OVP = 35 V nominal
• Switching frequency = 2 MHz



Typical Application



Optional Configuration for Thermal Derating

SPECIFICATIONS

Selection Guide

Part Number	Operating Temperature, T_A	Packing	Package	Leadframe Plating
A8501ELPTR-T	–40°C to 85°C	4000 pieces per 13-in. reel	28-pin TSSOP with exposed thermal pad	100% matte tin
A8501KLPTR-T	–40°C to 125°C			

Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Units
SW, OVP, CAP, OUT Pins			–0.3 to 40	V
LED1 through LED4 Pins			–0.3 to 21	V
VIN Pin	V_{IN}	Steady state	–0.3 to 34	V
		Transient < 1 s	40	V
DIM Pin	V_{DIM}		–0.3 to 6	V
Remaining Pins			–0.3 to 7	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
		Range G	–40 to 105	ºC
		Range K	–40 to 125	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

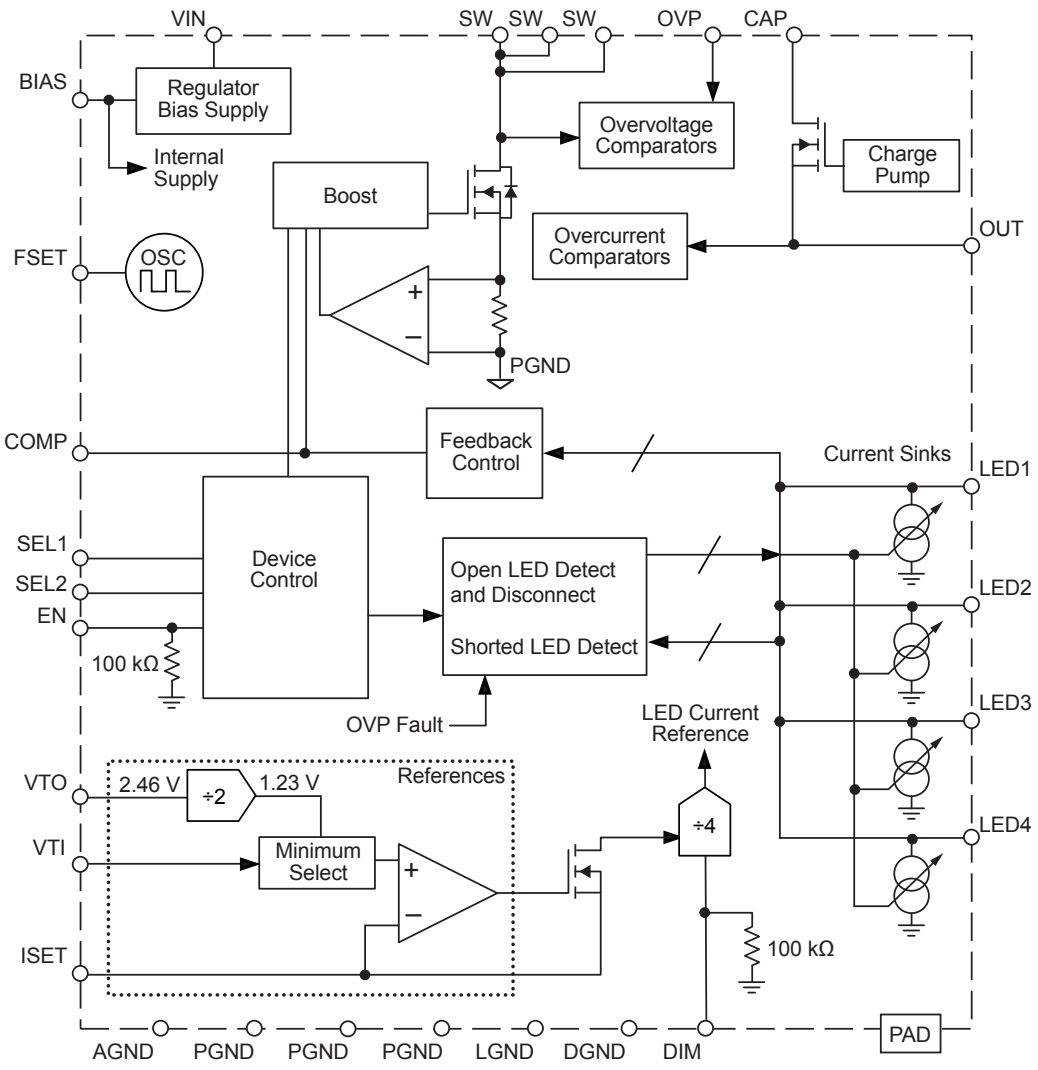
*Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	28	ºC/W

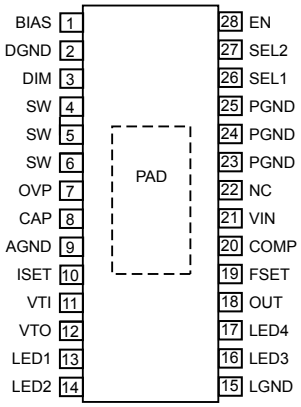
*Additional thermal information available on Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



Functional Block Diagram

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



Pin-out Diagram

Terminal List Table

Number	Name	Function
1	BIAS	Output of internal 6 V bias supply. Decouple with a 0.1 µF ceramic capacitor to DGND.
2	DGND	Digital signal ground. Connect AGND, DGND, LGND, PGND, and PAD using star ground connection.
3	DIM	Sets I_{LED} by adjusting the I_{SET} to I_{LEDx} current gain, A_{ISET} . When DIM = V_{IL} , A_{ISET} = 960 and when DIM=V_{IH} , A_{ISET} = 240.
4, 5, 6	SW	DMOS switch drain node. Tie these three pins together on the PCB.
7	OVP	To enable overvoltage protection, connect this pin through a resistor to the CAP pin. The default OVP level, with 0 Ω resistor, is 19.5 V. External resistor can set OVP up to 38 V.
8	CAP	Input connection for output disconnect switch.
9	AGND	Analog signal ground. Connect AGND, DGND, LGND, PGND, and PAD using star ground connection.
10	ISET	Sets the 100% current level through LED strings. Set by value of RISET connected between ISET and AGND.
11	VTI	ISET voltage override. Sets the ISET voltage when V_{TI} < 1.23 V. Tie directly to VTO pin to disable this feature. This pin can be used for LED current thermal derating or external analog LED current control. See the Typical Application Circuits section for additional information.
12	VTO	2.46 V output voltage. Use this voltage to bias an external NTC resistor or as a DAC reference. This pin can be used as a logic high signal for the SEL and DIM pins.
13,14,16,17	LEDX	LED current sinks.
15	LGND	Power ground for LED current sinks. Connect AGND, DGND, LGND, PGND, and PAD using star ground connection.
18	OUT	Output connection for output disconnect switch. Connect LED common connection to this pin.
19	FSET	Connect RFSET between FSET and AGND to set boost switching frequency.
20	COMP	Sets boost loop compensation. Connect external compensation capacitor between COMP and AGND for boost converter stability.
21	VIN	Input supply for the device. Decouple with a 0.1 µF ceramic capacitor.
22	NC	Not connected internally. It is recommended to connect this pin to external ground.
23, 24, 25	PGND	Power ground. Connect AGND, DGND, LGND, PGND, and PAD using star ground connection.
26	SEL1	SEL1 and SEL2 together select which LED strings are enabled. See Functional Description section.
27	SEL2	
28	EN	Enable and PWM LED current control. Apply logic-level PWM for PWM-controlled dimming mode.
–	PAD	Exposed thermal pad. Connect AGND, DGND, LGND, PGND, and PAD using star ground connection. Connect to PCB copper layer for enhanced heat dissipation.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: valid using circuit shown in figure 1; V_{IN} = 12 V, EN = SEL1 = SEL2 = 5 V, R_{ISET} = 12.4 kΩ, R_{FSET} = 24.3 kΩ, VTO shorted to VTI guaranteed over the full operating temperature range with $T_A = T_J$, typical specifications are at T_A = 25ºC; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
General						
Input Voltage Range	V_{IN}		8	–	21	V
Undervoltage Lockout Threshold	$V_{UVLO(th)}$	V_{IN} falling	5.7	6.5	6.8	V
UVLO Hysteresis Window	$V_{UVLO(hys)}$		0.21	0.55	0.81	V
Overvoltage Lockout Threshold	$V_{OVLO(th)}$	V_{IN} rising	29	32	34	V
Supply Current	I_S	2 MHz switching at no load	4	11	15	mA
		EN = V_{IL}, in shutdown, T_A = 25°C, CAP = VIN = SW = OVP = 16 V, $I_S = I_{VIN} + I_{SW} + I_{CAP} + I_{OVP}$	–	3.5	6	µA
		EN = V_{IL}, in shutdown, T_A = –40°C to 125°C, CAP = VIN = SW = OVP = 16 V, $I_S = I_{VIN} + I_{SW} + I_{CAP} + I_{OVP}$	–	3.5	10	µA
		EN = V_{IL}, not in shutdown, $I_S = I_{VIN}$	–	2	4	mA
Logic Input levels (DIM, EN, SELx Pins)						
Input Voltage Level-Low	V_{IL}		–	–	0.4	V
Input Voltage Level-High	V_{IH}		1.5	–	–	V
Input Leakage Current (EN, DIM pins)	I_{lkg1}	V_{DIM}, V_{EN} = 5 V	30	50	70	µA
Input Leakage Current (SELx pins)	I_{lkg2}	V_{SELx} = 5 V	–	–	1	µA
Overvoltage Protection						
Output Overvoltage Threshold	$V_{OVP(th)}$	OVP pin connected to OUT pin	18	19.5	21	V
OVP Sense Current	I_{OVPH}		183	200	217	µA
OVP Leakage Current	$I_{OVP(lkg)}$	V_{OVP} = 18 V, EN = V_{IL}, in shutdown	–	0.1	1	µA
Boost Switch						
Switch On Resistance	$R_{SWDS(on)}$	I_{SW} = 2 A	40	100	300	mΩ
Switch Leakage Current	$I_{SW(lkg)}$	V_{SW} = 21 V	–	0.1	10	µA
Switch Current Limit	$I_{SW(lim)}$		3	3.6	5.3	A
LED Current Sinks						
LEDx Regulation Voltage	V_{LED}	$V_{LED1} = V_{LED2} = V_{LED3} = V_{LED4}$	–	750	1100	mV
I_{ISET} to I_{LEDx} Current Gain	A_{ISET}	I_{ISET} = 100 µA, DIM = V_{IL}	914	960	1008	A/A
		I_{ISET} = 100 µA, DIM= V_{IH}	228	240	252	A/A
ISET Pin Voltage	V_{ISET}		1.13	1.235	1.34	V
VTO Pin Voltage	V_{TO}	I_{VTO} = 1 mA	2.00	2.46	2.65	V
VTO Pin Current Maximum	$I_{TO(max)}$	I_{VTO} increased until V_{TO} drops by 1%	1.5	2.4	5	mA
VTI Pin Voltage	$V_{TI(falling)}$	V_{TI} start >1.34 V, VTI pin voltage decreasing before control changes to VTI pin	1.00	1.12	1.23	V
	$V_{TI(rising)}$	V_{TI} start <1 V VTI pin increasing before changing to internal reference	1.13	1.235	1.34	V
ISET Pin Allowable Current Range	I_{ISET}		20	–	100	µA

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): valid using circuit shown in figure 1; V_{IN} = 12 V, EN = SEL1 = SEL2 = 5 V, R_{ISET} = 12.4 kΩ, R_{FSET} = 24.3 kΩ, VTO shorted to VTI guaranteed over the full operating temperature range with $T_A = T_J$, typical specifications are at T_A = 25ºC; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LEDx Accuracy[1]	Err_{LED}	RISET = 12.4 kΩ. 100% current ratio, measured as the average of V_{LEDx}, for LED1 through LED4, with V_{LEDx} = 0.75 V, $T_A = T_J$ = 0 to 125°C	–	0.7	3	%
LEDx Matching[2]	Δ_{LEDx}	I_{ISET} = 100 µA, 100% current ratio, with V_{LEDx} = 0.75 V	–	0.8	3	%
LED Switch Leakage Current	$I_{S(lkg)}$	V_{LEDx} = 17.5 V, EN = V_{IL} = 0 V	4.8	8.75	12.8	µA
LEDx Short Detect Voltage Threshold	V_{LEDSC}	On any LEDx pin, forces latched shutdown	17.5	19	21	V
Output Disconnect Switch On-Resistance	$R_{ODS(on)}$	V_{IN} = 8 V, I_{OUT} = 400 mA, T_J = 125°C	–	2	4	Ω
Oscillator						
FSET Pin Voltage	V_{FSET}	R_{FSET} = 24.3 kΩ	1.14	1.235	1.33	V
Frequency	f_{OSC}	R_{FSET} = 24.3 kΩ	1.8	2.1	2.4	MHz
		R_{FSET} = 51.1 kΩ	0.850	1	1.285	MHz
		R_{FSET} = 84.5 kΩ	0.5	0.6	0.8	MHz
Minimum Switch Off-Time	$t_{off(min)}$		–	60	110	ns
Minimum Switch On-Time	$t_{on(min)}$		–	60	110	ns
Soft Start						
Soft Start Boost Current Limit	$I_{SWSS(lim)}$	Initial soft start current for boost switch	0.4	0.6	0.75	A
Soft Start LEDx Current	I_{LEDSS}	Current through each enabled LEDx pin during soft start, R_{ISET} = 12.4 kΩ	3	5	10	mA
PWM Timing on EN pin						
Maximum PWM Dimming Off-Time	t_{PWML}	Measured while EN = low, during dimming control, and internal references are powered on (exceeding t_{PWML} results in shutdown)	–	131,072	–	f_{SW} cycles
Minimum PWM On-Time	t_{PWMH}		–	–	6	µs
PWM High to LED On Delay	$t_{dPWM(on)}$	Time between PWM enable and when LED current reaches 90% of maximum, with internal references enabled and t_{PWML} not exceeded	–	3	–	µs
PWM Low to LED Off Delay	$t_{dPWM(off)}$	Time between EN going low and when LED current reaches 10% of maximum, with internal references enabled and t_{PWML} not exceeded	–	0.5	–	µs
Thermal Shutdown Threshold[3]	T_{TSD}	Device temperature rising	150	172	195	°C
Thermal Shutdown Hysteresis[3]	$T_{TSD(hys)}$		15	20	25	°C

[1]LED accuracy is defined as (I_{ISET} × 960 – I_{LED}(av)) / (I_{ISET} × 960), I_{LED}(av) measured as the average of I_{LED1} through I_{LED4}.
[2]LED current matching is defined as (I_{LEDx} – I_{LED}(av)) / I_{LED}(av), with I_{LED}(av) as defined in footnote 1.
[3]Guaranteed by design and characterization, functional tested in production.

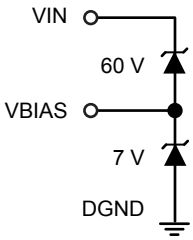
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PERFORMANCE CHARACTERISTICS

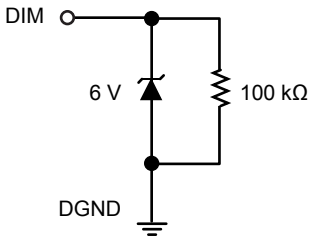
Electrostatic Discharge Structures

Equivalent ESD on Pins

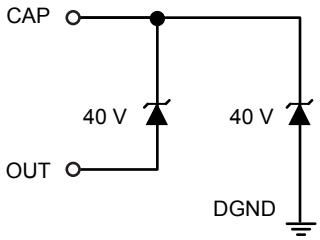
VIN / VBIAS



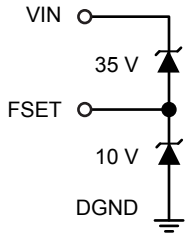
DIM



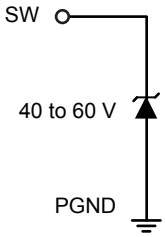
CAP / OUT



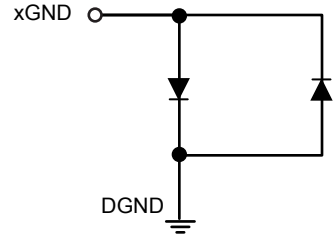
VIN / FSET



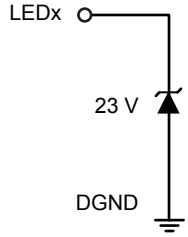
SW



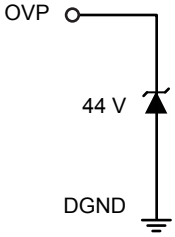
AGND, LGND, PGND, and DGND



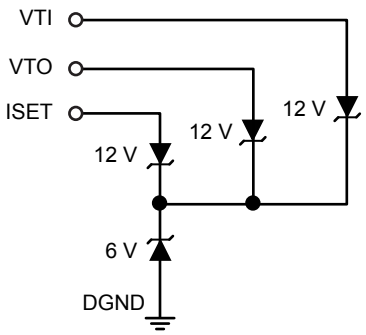
LEDx



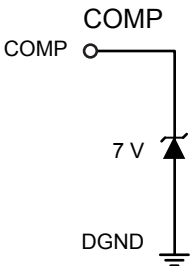
OVP



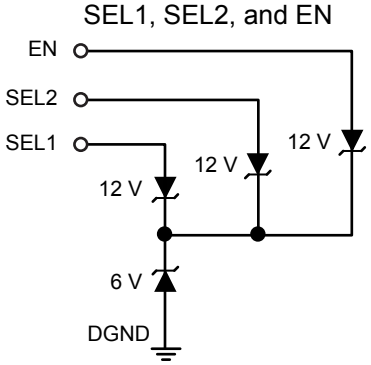
ISET, VTO, and VTI



COMP



SEL1, SEL2, and EN

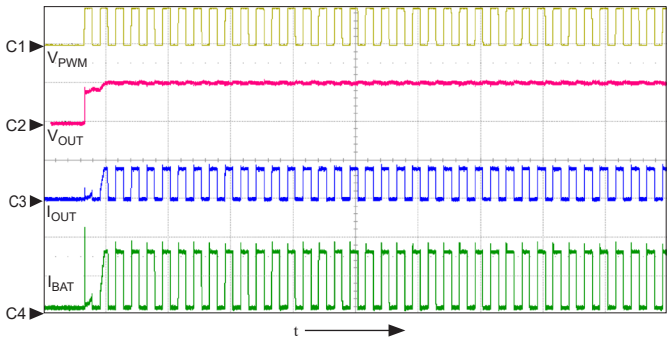


Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PERFORMANCE CHARACTERISTICS

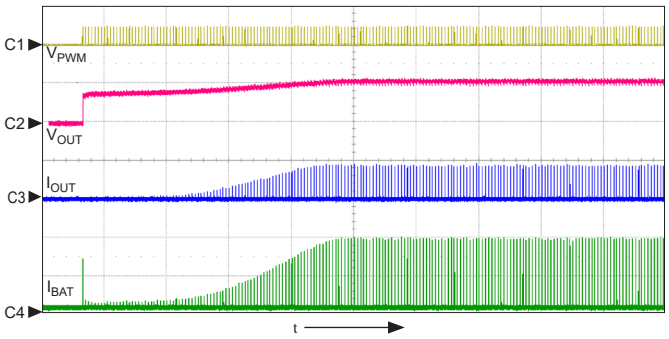
PWM Waveforms
V_{BAT} = 12 V, I_{OUT} = 400 mA, f_{PWM} = 200 Hz
4 channels enabled, 6 LEDs each channel

50% PWM Duty Cycle (Startup)



Symbol	Parameter	Units/Division
C1	V_{BAT}	5 V
C2	V_{OUT}	20 V
C3	I_{OUT}	500 mA
C4	I_{BAT}	500 mA
t	time	20 ms

1% PWM Duty Cycle (Startup)



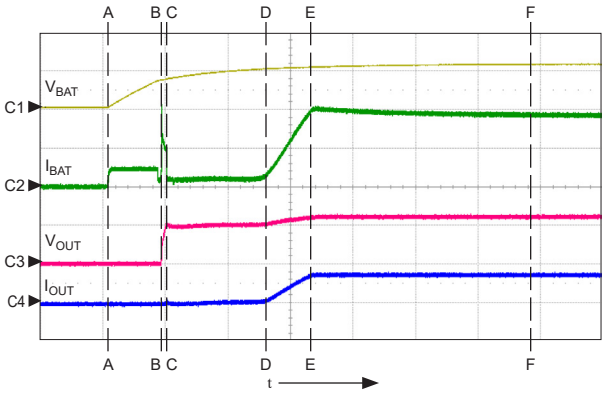
Symbol	Parameter	Units/Division
C1	V_{PWM}	5 V
C2	V_{OUT}	20 V
C3	I_{OUT}	500 mA
C4	I_{BAT}	500 mA
t	time	100 ms

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PERFORMANCE CHARACTERISTICS

Startup Waveforms

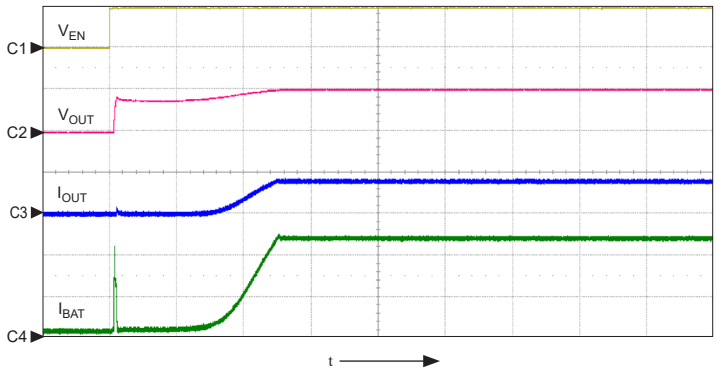
Soft Start Turn On Using Rising V_{BAT}
V_{EN} = 5 V, V_{BAT} = 0 V to 12 V, I_{OUT} = 400 mA
4 channels enabled, 6 series LEDs each



Symbol	Parameter	Units/Division
C1	V_{BAT}	10 V
C2	I_{BAT}	500 mA
C3	V_{OUT}	20 V
C4	I_{OUT}	500 mA
t	time	5 ms

A. V_{BAT} voltage slowly increased with EN held high.
A–B. Input bulk capacitor C_{BAT} and boost output capacitor C_{OUT} are charged to V_{UVLO} .
B. V_{BAT} reaches V_{UVLO}, and enables A8501 through soft start.
B–C. During soft start period, boost switch peak current is limited to 600 mA and LED current to $^1/_{20}$ of desired level. Narrow current spike at B is due to parasitic capacitance from OUT to ground and C_{BIAS}. COMP pin is help low during soft start.
D. After V_{OUT} reaches a level such that all LED pins > 0.75 V, the A8501 comes out of soft start.
C–E. After initial rise of V_{OUT}, the capacitor C_{COMP} starts charging slowly (C_{COMP} not shown).
E. V_{COMP} reaches desired level for stable operation.
F. A8501 and LEDs reach thermal steady state.

Turn On Using EN Pin
V_{BAT} = 8 V, V_{EN} = 0 V to 5 V, I_{OUT} = 400 mA
4 channels enabled, 6 series LEDs each

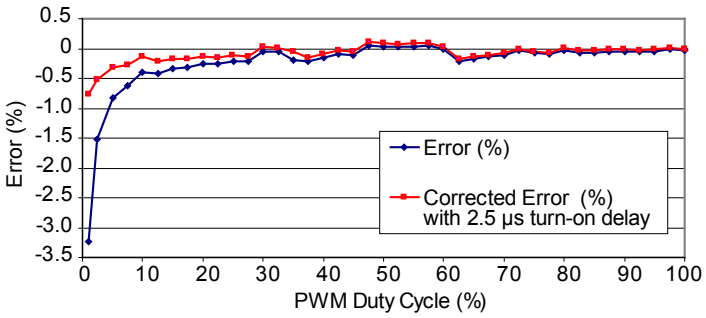


Symbol	Parameter	Units/Division
C1	V_{EN}	5 V
C2	V_{OUT}	20 V
C3	I_{OUT}	500 mA
C4	I_{BAT}	500 mA
t	time	2 ms

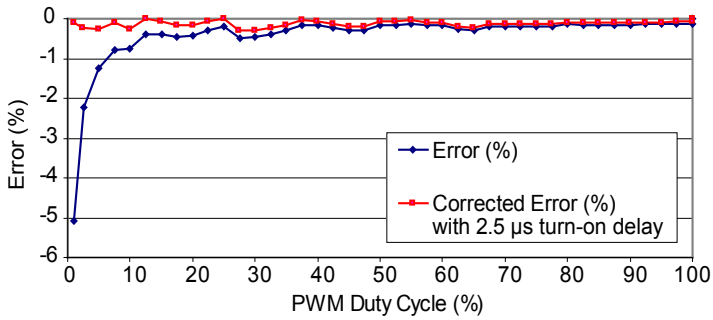
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PERFORMANCE CHARACTERISTICS

LED Current Error at 100 Hz PWM

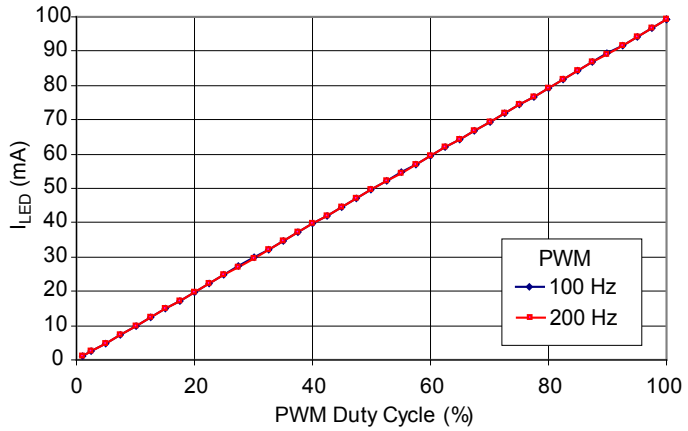


LED Current Error at 200 Hz PWM

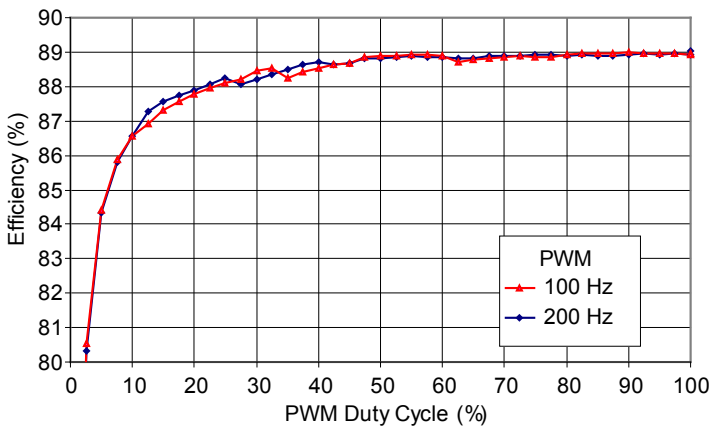


The LED Current Error graph shows the effect of PWM duty cycles on LED current error, according to the relationship: Error (%) = (I_{ISET} × 960 x PWM Duty cycle – I_{LED}(av)) / (I_{ISET} × 960 x PWM Duty cycle) .
At lower PWM duty cycles, turn-on delay adversely affects LED current accuracy. This accuracy can be improved by extending the applied PWM signal by 2.5 µs. For example, at 100 Hz PWM and 1% PWM duty cycle, the on-time would be 100 µs. The effects of that turn-on delay could be offset by applying a 102.5 µs PWM pulse.

LED Current versus PWM Duty Cycle



Efficiency versus PWM Duty Cycle

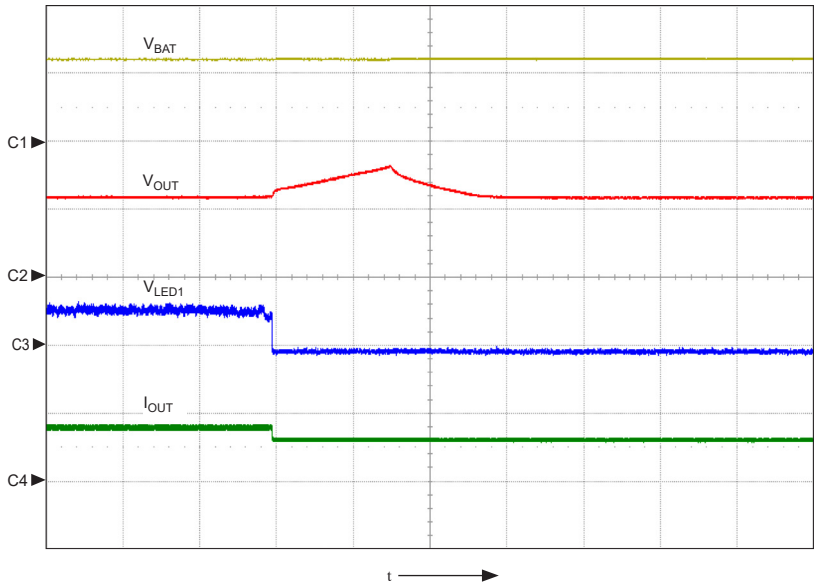


Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PERFORMANCE CHARACTERISTICS

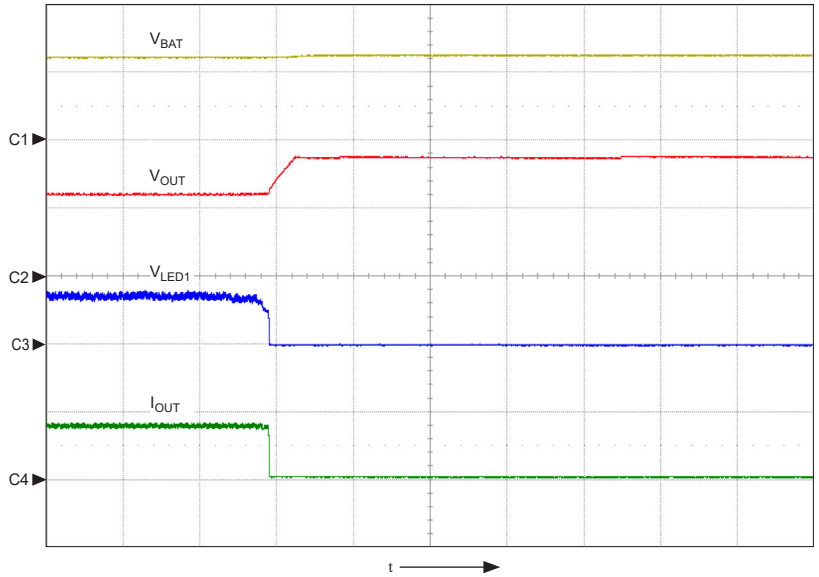
Output LED Open Protection
V_{BAT}= 12 V, I_{LED} = 100 mA per LED string, EN = high

LED string #1 disconnected. V_{OUT} increases to OVP level, and LED string #1 is removed from regulation. The rest of the LED strings continue to function normally.



Symbol	Parameter	Units/Division
C1	V_{BAT}	10 V
C2	V_{OUT}	20 V
C3	V_{LED1}	1 V
C4	I_{OUT}	500 mA
t	time	100 µs

All four LED strings disconnected simultaneously. V_{OUT} increases to OVP level, and all LED strings are removed from regulation.



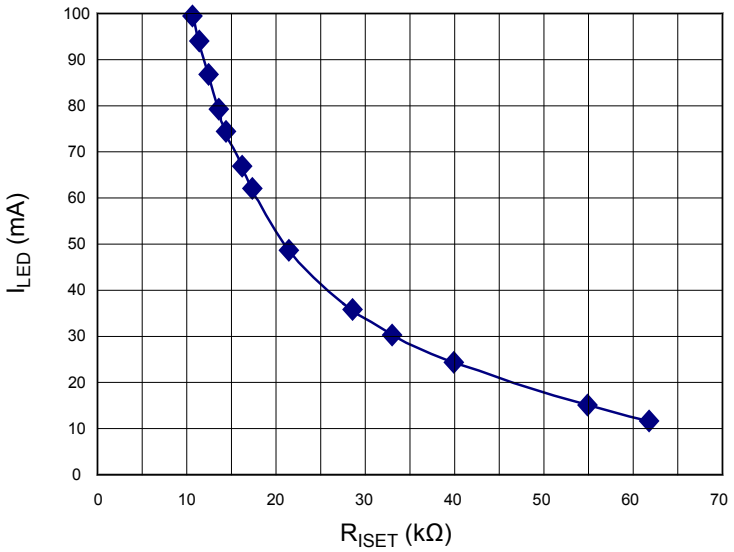
Symbol	Parameter	Units/Division
C1	V_{BAT}	10 V
C2	V_{OUT}	20 V
C3	V_{LED1}	1 V
C4	I_{OUT}	500 mA
t	time	100 µs

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

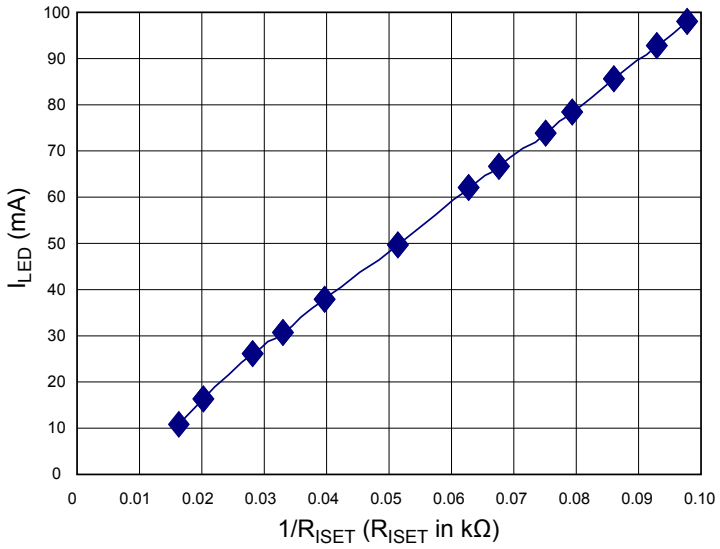
PERFORMANCE CHARACTERISTICS

ISET Characterization

LED Current versus R_{ISET}



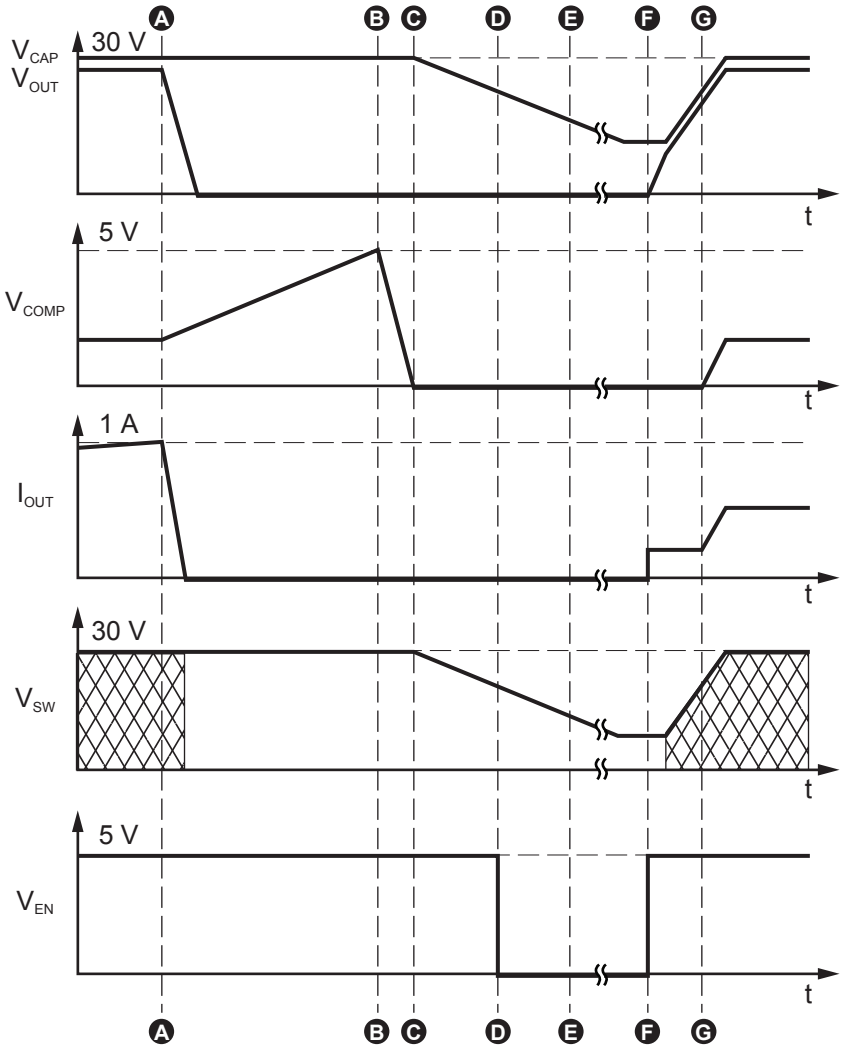
LED Current versus $1/R_{ISET}$



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PERFORMANCE CHARACTERISTICS

Disconnect Switch Overcurrent Fault Timing Diagram



A. Overcurrent on disconnect switch is detected and disconnect switch latches off. Boost is turned off when >3 V is detected across the disconnect switch. LEDs stop sinking current because there is insufficient voltage across them.

B. COMP pin reaches lockout level. LEDs are internally turned off and the COMP pin is discharged.

C. COMP pin reaches ground voltage, LEDs are internally turned on, in soft start mode, and boost is put into soft start mode. Boost and LEDs remain off because V_{OUT} is still at ground potential due to the disconnect switch being latched off.

D. User turns off EN.

E. The A8501 shuts down when EN is off for more than 131,072 clock cycles. If any other fault conditions were present prior to shutdown, such as: open LED, TSD, shorted LED, or secondary OVP, these are now cleared and the part is ready to be re-enabled.

F. User re-enables operation. A8501 enters soft start mode.

G. Soft start mode finished.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PERFORMANCE CHARACTERISTICS

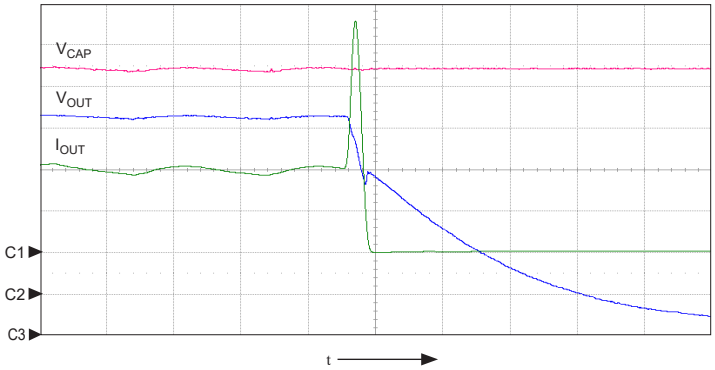
Fault Protection

V_{BAT} = 12 V, I_{LED} = 100 mA per string

4 channels enabled, 8 series LEDs each

VOUT to LED1 Short

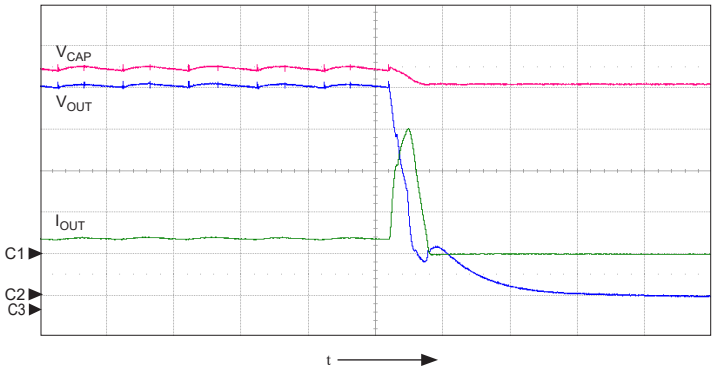
(LED Short Detect activated, causing a latched shutdown)



Symbol	Parameter	Units/Division
C1	I_{OUT}	200 mA
C2	V_{CAP}	5 V
C3	V_{OUT}	5 V
t	time	1 µs

V_{OUT} to Ground Short

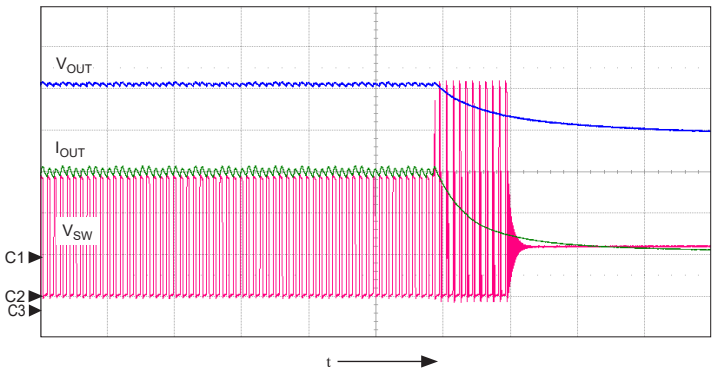
(Output Disconnect Switch opens to prevent any damage)



Symbol	Parameter	Units/Division
C1	I_{OUT}	1 A
C2	V_{CAP}	5 V
C3	V_{OUT}	5 V
t	time	2 µs

Open Schottky Diode Disconnect

(Secondary OVP activated, causing a latched shutdown)



Symbol	Parameter	Units/Division
C1	I_{OUT}	200 mA
C2	V_{SW}	10 V
C3	V_{OUT}	5 V
t	time	20 µs

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL CHARACTERISTICS

Description

The A8501 is a multioutput WLED/RGB driver for display backlighting. It uses a boost converter architecture to generate output voltage to drive 4 channels with up to 9 LEDs per channel (V_f= 3.5 V, I_f= 100 mA). The current-mode boost converter operates at constant frequency. The boost switching frequency can be set from 600 kHz to 2.2 MHz by an external resistor connected across FSET and AGND. The integrated boost DMOS switch is rated for 40 V at 3.6 A. This switch is protected against overvoltage, and provides pulse-by-pulse current limiting independently of boost converter duty cycle.

The A8501 has 4 well-matched current sinks, which provide regulated current through the load LEDs for uniform display brightness. All LEDx sinks are rated for 21 V to allow PWM dimming control.

FREQUENCY SELECTION

The switching frequency on the SW pin, f_{SW}, can be set by applying the following equation:

$$f_{SW} = 51/R_{FSET} \quad , \qquad (1)$$

where f_{SW} is in MHz, and R_{FSET} is in kΩ.

LED SELECTION

Which LED strings are enabled is determined by the combined settings of the SEL1 and SEL2 pins, according to the following table:

Table 1: LED Channel Selection

SEL1 Pin	SEL2 Pin	Enabled LEDx Outputs
Low	Low	Only LED1
High	Low	LED1 and LED2
Low	High	LED1, LED2, and LED3
High	High	All channels

LED strings that are connected to the A8501, but are not enabled through the SELx pins, may cause a shutdown if the voltage on the corresponding LEDx pins exceeds V_{LEDSC}. Refer to the LED Short Detect section for further details. Unused LEDx pins can be left open or connected to ground.

Use matched forward voltage LEDs for better efficiency.

The application circuit shown in Figure 1 is a boost converter and the output voltage is always higher than the battery voltage. Therefore, the quantity of LEDs per string should be such that the required output voltage is higher than the maximum battery voltage. If the battery voltage is higher than the output voltage, the A8501 will switch with minimum pulse width, and the actual output voltage will be higher than the required voltage. The excess voltage will be dropped across the LED strings. This lowers efficiency and increases power dissipation, resulting in higher device temperature. If battery voltage must be higher than required output voltage, use a SEPIC converter, as shown in Figure 10.

Enabling the IC

The A8501 is enabled by pulling the EN pin to logic high, provided that VIN is above UVLO threshold, If EN=H before VIN is applied, the IC will only startup after VIN has raised above UVLO threshold, This is illustrated by startup waveforms shown on page 9.

Soft-Start and Compensation

At startup, the output capacitor is discharged and the A8501 enters soft start. The boost current is limited to 0.6 A and all active LEDx pins sink $^1/_{20}$ of the set current until all the enabled LEDx pins reach 0.75 V. When the A8501 comes out of soft start, the boost current and the LEDx pin currents are set to normal. The output capacitor charges to voltage required to supply full LEDx currents within a few cycles. Once V_{OUT} reaches the required level, LEDx current toggles between 0 and 100% in response to PWM signals. Soft start behavior on evaluation boards is shown in the Performance Characteristics section.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

LED Current Setting

The maximum LED current can be up to 100 mA per channel, and is set through the ISET pin. Connect a resistor, RISET, between this pin and AGND to set the reference current level, I_{ISET} , according to the following formula:

$$I_{ISET} = 1.235 / R_{ISET} , \quad (2)$$

where I_{ISET} is in mA and R_{ISET} is in kΩ.

This current is multiplied internally with a gain of 960, and mirrored on all enabled LED pins. This sets the maximum current through the LEDs, referred as the *100% current*.

DIMMING

The LED current can be reduced from the 100% current level by three alternative dimming methods:

- PWM dimming using the EN pin. PWM dimming is performed by applying an external PWM signal on the EN pin. When the EN pin is pulled high, the A8501 turns on and all enabled LEDs sink 100% current. The sequence is shown in Figure 2. For optimal accuracy, the external PWM signal should be in the range 100 to 300 Hz. The slight delay between PWM signal and the LED current causes an error. To compensate for the error, a small turn-on delay should be added to the PWM signal as shown on page 10 of the Performance Characteristics section. When EN is pulled low, the boost converter and LED sinks are turned off. The compensation (COMP) pin is floated, and critical internal circuits are kept active. If EN is pulled low for more than t_{PWML} , the device enters shutdown mode and clears all internal fault registers. As an example, for a 2 MHz clock, the maximum PWM low period while avoiding shutdown is 65 ms.
- Analog dimming using the DIM pin. When the DIM pin is pulled low, the LED sinks draw 100 % current; when the pin is pulled high, the LED current level drops to 25%.
- Analog dimming using the VTI pin. External DC voltage can be applied to the VTI pin to control LED current. LED current varies as a function of voltage on the VTI pin. This configuration is shown in Figure 5.

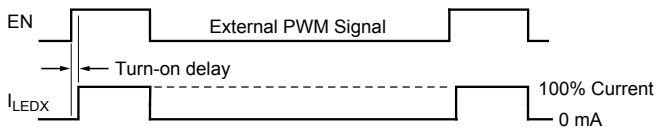


Figure 2: Timing Diagram of External PWM Signal and LED Current

LED Open Detect

When any LED string opens, the boost circuit increases the output voltage until it reaches the overvoltage protection level. The OVP event causes any LED string that is not in regulation to be locked-out from regulating the loop. By removing the open LED from controlling the boost, the output voltage returns to normal operating voltage. Every OVP event retests all LED strings. An EN low signal does not reset the LED string regulation lock unless it shuts down the device (exceeds t_{PWML}). The locked-out LED pins always attempt to sink desired current regardless of lock-out state.

LED Short Detect

Any LED pin that has a voltage exceeding V_{LEDSC} will force the device to disable the boost circuit and LEDx outputs until EN shuts down the A8501 (EN low exceeds t_{PWML}). This protects the LEDx pins from potentially hazardous voltages when multiple LEDs are shorted in one string.

Overvoltage Protection

The A8501 has overvoltage protection (OVP) and open Schottky diode protection.

The OVP has a default level of 19.5 V and can be increased up to 38 V by the selection of an external resistor, as shown in figure 3. When the current though OVP pin exceeds 200 µA, the OVP comparator goes low. When V_{OUT} falls and current through the OVP pin drops below 165 µA, the OVP is released.

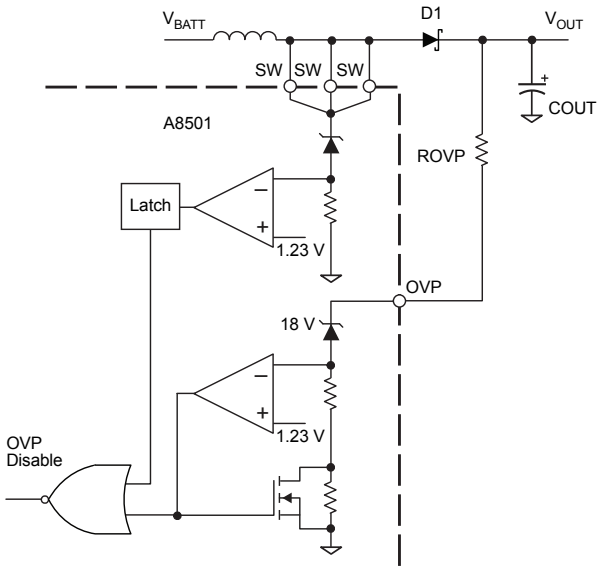


Figure 3: Overvoltage Protection (OVP) Circuit

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The following equation can be used to determine the resistance for setting the OVP level:

$$R_{OVP} = (V_{OVP} - 19.5) / 200\ \mu A \quad , \qquad (3)$$

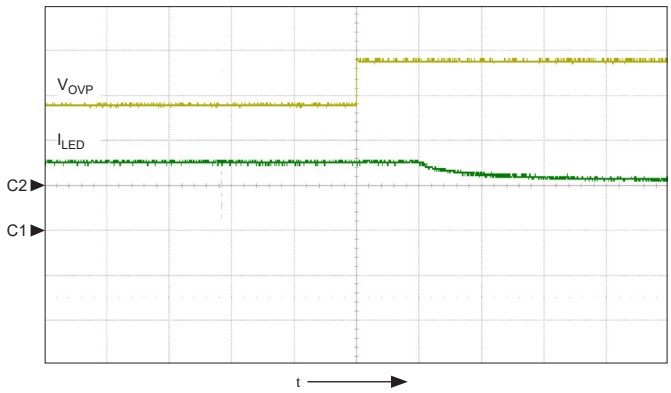
where V_{OVP} is the target typical OVP level, and R_{OVP} is the value of the external resistor, in Ω.

A8501 has secondary overvoltage protection to protect internal switches in the event of an open diode condition. Open Schottky diode detection is implemented by detecting overvoltage on the SW pin. If voltage on the SW pin exceeds the device safe operating voltage rating, the A8501 disables and remains latched. The IC must shut down before it can be reenabled.

OVERCURRENT PROTECTION

The boost switch is protected with pulse-by-pulse current limiting at 3.6 A. The output disconnect switch protects against output overcurrent. At 1 A typical, the A8501 disables. This process is detailed in the Disconnect Switch Overcurrent Fault Timing diagram in the Performance Characteristics section, page 13.

In some instances, when the LEDs are connected by long wires and also some output capacitance (such as ESD capacitors) is present, a clamping diode on the output must be used. This diode will prevent the output from momentarily going negative during a short circuit condition. The diode must be chosen such that its reverse breakdown voltage is higher than normal operating voltage and its reverse current leakage is small. Please refer to the application note *Output Diode Clamping for the A8501* for more details.



Symbol	Parameter	Units/Division
C1	V_{OVP}	10 V
C2	I_{LED}	50 mA
t	time	100 µs

Figure 4: Output Overvoltage Protection (OVP) Operation

INPUT UVLO

When V_{IN} rises above the UVLO enable hysteresis ($V_{UVLO(th)}$ + $V_{UVLO(hys)}$), the A8501 is enabled. It is disabled when V_{IN} falls below $V_{UVLO(th)}$ for more than 50 µs. This lag is to avoid shutting down because of momentary glitches in the power supply.

INPUT OVLO

When V_{IN} rises above $V_{OVLO(th)}$ for more than 50 µs, the A8501 is disabled, the boost converter shuts down instantly, and LED current falls gradually with the CAP pin capacitor. When V_{IN} falls below $V_{OVLO(th)}$ and EN is high, the device is reenabled.

THERMAL DERATING

Thermal derating can be achieved by connecting an NTC thermistor between VTI and ground, as shown in figure 5. When the A8501 is enabled and V_{TI} > 1.1 V, 100% current for the LEDs is controlled by the ISET and DIM pins. This is represented by the solid blue curves in figure 6. When V_{TI} falls below 1.1 V, V_{ISET} starts to follow V_{TI}, resulting in I_{LEDX} varying proportionately with V_{TI} represented by the overlap of the dotted and solid curves. The proportion of I_{LED} to V_{TI}, when LED current is controlled through the VTI pin, is calculated as:

$$I_{ILEDx} = 960 \times V_{TI} / R_{ISET} \ , \qquad (4)$$

where I_{LEDx} is the LEDx pin current in mA, and R_{ISET} is in kΩ.

There is a hysteresis built into the VTI pin circuit, so while V_{TI} is decreasing, there is a delay before proportional change begins if VTI pin voltage starts above 1.1 V, as shown by the solid blue curves in figure 6. When V_{TI} starts below 1.1 V, or falls below 1.1 V during operation and then starts increasing again V_{ISET} will follow V_{TI} until the voltage reaches 1.23 V as shown by the red-and-white dotted curves in Figure 6.

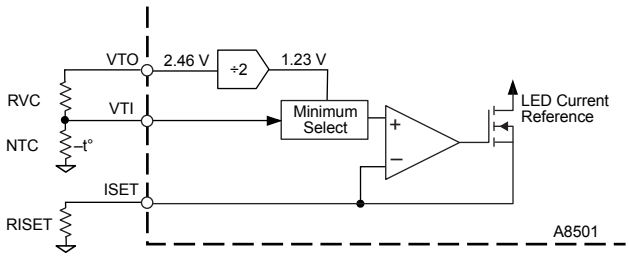
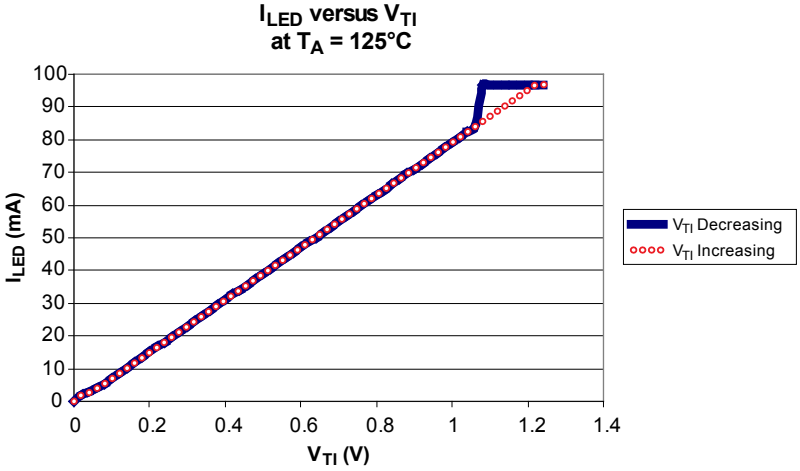


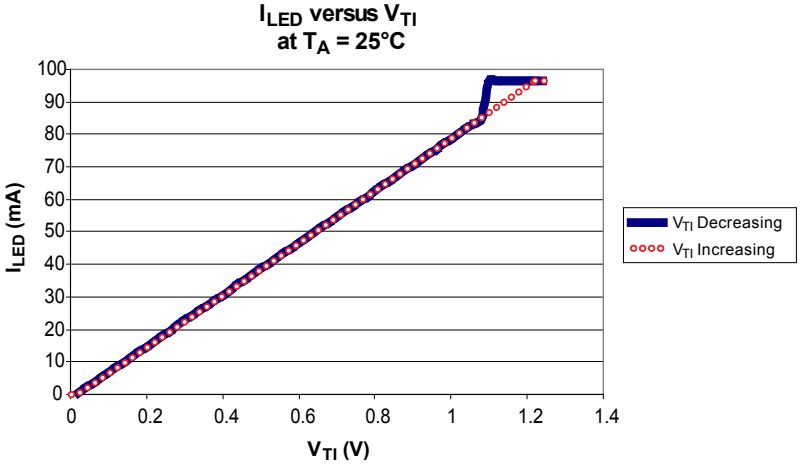
Figure 5: Thermal Derating Reference Circuit

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

(A)



(B)



(C)

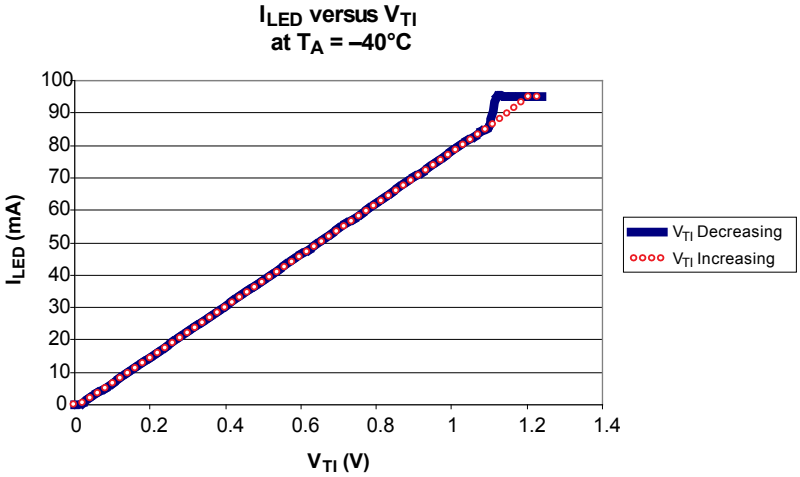


Figure 6: LEDx Current versus V_{TI}

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Bias Supply

The BIAS pin provides regulated 6 V for internal circuits. Connect a CBIAS capacitor with a value in the range of 0.1 to 1 µF.

Efficiency Considerations

For better efficiency, use a high quality inductor with relatively low DCR and core loss.

Use a low forward voltage Schottky diode with relatively low junction capacitance.

Use matched forward voltage LEDs for better efficiency.

The A8501 provides an output disconnect function through a load switch that is connected from the boost converter output (CAP) to LED connection (OUT). This function protects the system against short circuit conditions from common anode LED connection to ground, for both boost and SEPIC configurations.

When comparing the efficiency of the A8501 with an alternate implementation requiring an external input/output disconnect function, the additional power dissipation in this disconnect switch must be considered for a proper comparison. To bypass the disconnect switch, short the CAP pin to the OUT pin to have a direct connection from the boost regulator to the common anode LED node. When the disconnect switch is bypassed, both the boost and the SEPIC implementations are not protected against output short circuit conditions.

Audible Noise Considerations

Multilayer ceramic capacitors cause audible noise when subjected to voltage ripple in the audio frequency range, due to the piezoelectric effect. Ceramic capacitors connected across boost converters can also cause audible noise due to voltage ripple at dimming frequencies. During the PWM dimming off-time, the voltage across the capacitors drops due to leakage through the output disconnect switch and the OVP pin. This voltage is regulated to the desired output level during the PWM dimming on-time. This voltage ripple may cause audible noise.

Audible noise can be minimized with higher dimming frequency, but at higher dimming frequencies accuracy may be affected, as shown in the Performance Characteristics section. It is recommended to use 200 Hz for optimum performance.

Selecting a sufficiently large capacitor across the boost output can reduce voltage ripple and noise. It is observed that the audible noise below 250 mV ripple is negligible.

The value to select for a boost capacitor can be calculated using the following formula:

$$C \geq \frac{I_{lk} \times (1 - D_{FPWMmin})}{f_{PWM} \times 0.25} \quad . \qquad (5)$$

where

I_{lk} is the leakage current; select I_{lk} = 165 µA at a 30 V output and 175 µA at a 40 V output,

$D_{FPWMmin}$ is the minimum dimming PWM duty cycle, and

f_{PWM} is the dimming frequency; typically 200 Hz.

For example, if the dimming frequency is 200 Hz, the minimum dimming PWM duty cycle = 10%, and V_{OUT} = 30 V, then select the boost capacitor as:

$$C = \frac{165\ \mu A \times (1 - 0.1)}{200 \times 0.25} = 3\ \mu F \quad .$$

The capacitance of ceramic capacitors drops with DC bias. Use an appropriate capacitor to get at least 3 µF at 30 V.

The selection of a ripple voltage of 0.25 V is based on a typical MLCC. This ripple level depends on the type and construction of the MLCC. Increase the boost capacitor if noise exists at 0.25 V.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION INFORMATION

Design Example

This section provides a method for selecting component values when designing an application using the A8501.

ASSUMPTIONS

For the purposes of this example, the following are given as the application requirements:

- V_{BAT}: 8 to 18 V
- Quantity of LED channels, $\#_{CHANNELS}$: 3
- Quantity of series LEDs per channel, $\#_{SERIESLEDS}$: 8
- LED current per channel, I_{LED}: 80 mA
- Total current all channels, $I_{OUT} = I_{LED} \times \#_{CHANNELS}$
- V_f at 80 mA: 3 to 3.4 V
- f_{SW}: 2 MHz
- T_A(max): 65°C

DIMMING

The A8501 can work with wide range of PWM frequencies. A small delay between the PWM signal and the LED current may have a noticeable effect at high PWM frequencies combined with low PWM duty cycles. For example, at 100 Hz and 10% PWM duty cycle, the PWM on-period is 1 ms. In that period, the delay causes only a 0.6% error. If the PWM frequency is 1 kHz, this error is 6%. However, the error caused by the turn-on delay can be decreased by increasing the applied PWM duty cycle as shown on page 10 in the Performance Characteristics section.

PROCEDURE

The procedure consists of selecting the appropriate configuration and then the individual component values, in an ordered sequence.

1. Identify the SEL*x* pins to use. For 3 channels:
   A. connect pin SEL2 to V_{TO}
   B. connect pin SEL1 to ground
2. Connect LEDs to pins LED1 through LED3 (leave pin LED4 open).
3. Select resistor RISET (connected between pin ISET and AGND). Given I_{LED} = 80 mA and A_{ISET} = 960, then:

$$R_{ISET} = 1.235 / (I_{LED} / A_{ISET}) . \quad (6)$$

Substituting:

$$R_{ISET} = 1.235 / (0.080 / 960) = 14.82\ k\Omega .$$

Select a common value: 14.7 kΩ, 1%.

4. Select resistor RFSET (connected between pin FSET and AGND). Given:

$$R_{FSET} = 51 / f_{SW} , \quad (7)$$

for a 2 MHz switching frequency, select:

$$R_{FSET} = 51 / 2 = 25.5\ k\Omega , 1\%.$$

5. Select resistor ROVP (connect to the OVP pin to set the OVP level, V_{OUT}(max)). Given V_f(max) = 3.4 V, 0.75 V as the V_{LED} regulation level, and worst case output disconnect switch voltage drop, then:

$$V_{OUT}(\max) = (V_f(\max) \times \#_{SERIESLEDS}) + V_{LED} + (R_{ODS(on)} \times I_{LED} \times \#_{CHANNELS}) . \quad (8)$$

Substituting:

$$V_{OUT}(max) = (3.4 \times 8 + 0.75) + (4 \times 0.08 \times 3) = 28.91\ V .$$

The switch resistance $R_{ODS(on)}$ can be found in the electrical table and is listed as worst case at 4 Ω at high temperatures. To set the output OVP level to 33 V, given an I_{OVPH} of 200 µA, and $V_{OVP(th)}$ = 19.5 V:

$$R_{OVP} = (V_{OVP} - V_{OVP(th)}) / I_{OVPH} . \quad (9)$$

Substituting:

$$R_{OVP} = (33 - 19.5) / 200 \times 10^{-6} = 68\ k\Omega . \quad (10)$$

6. Select inductor L1. This should assume a maximum boost converter duty cycle, D(max), at V_{BAT}(min) and 90% efficiency, η.

$$D(max) = 1 - (V_{BAT}(min) \times \eta) / V_{OUT}(max) \quad (11)$$

$$D(max) = 1 - (8 \times 0.9) / 28.91 = 75\% .$$

Then calculate maximum switch on-time:

$$t_{on}(max) = D(max) / f_{SW} \quad (12)$$

$$= 0.75 / 2 \times 10^6 = 375\ ns .$$

Maximum input current can be calculated as:

$$I_{BAT} = (V_{OUT}(max) \times I_{OUT}) / (V_{BAT}(min) \times \eta) \quad (13)$$

$$I_{BAT}(max) = [28.91 \times (0.080 \times 3)] / (8 \times 0.9) = 963\ mA.$$

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Set inductor ripple at 30% of I_{BAT}(max):

$$I_L = I_{BAT}(max) \times I_{Lripple}(Ideal) \quad . \qquad (14)$$

Substituting:

$$\Delta I_L = 0.3 \times 963 = 289\ mA$$

Given, during switch on-time:

$$V_{BAT}(min) = L \times \Delta I_L \times f_{SW} / D \ , \qquad (15)$$

$$8 = L \times 0.289 \times 2 \times 10^6 / 0.75, \text{ and}$$

$$L = 10.4\ \mu H \ .$$

Select a common value: $L_{(used)}$ = 10 µH.

It is recommended to select an inductor that can handle a DC current level that is greater than 963 mA, at the peak current level (saturation) of 963 mA + 289 mA / 2 = 1.11 A. This is to ensure that the inductor does not saturate at any steady state or transient condition, within specified temperature and tolerance ranges. Inductor saturation level decreases with increasing temperature. It is advisable to use a inductor with a saturation level of 2.0 A. The inductor should have a low DC resistance (DCR) and core loss for better efficiency.

7. Select output capacitor COUT, given:

$$f_{PWM} = 100\ Hz \ , \qquad (16)$$

assuming 20% minimum dimming PWM duty cycle, $D_{PWM(min)}$, and the maximum leakage current through the output disconnect switch at V_{OUT} = 28 V is 165 µA and $V_{COUTripple}$ = 0.25 V.

Select the output capacitor as:

$$C_{OUT} = I_{lk} \times (1 - D_{PWM(min)}) / (f_{PWM} \times V_{COUTripple}) \ . \qquad (17)$$

Substituting:

$$C_{OUT} = 165\ \mu A \times (1 - 0.2) / (100 \times 0.25) = 5.3\ \mu F \ . \qquad (18)$$

Select 6.8 µF.

The RMS current through COUT is given by:

$$C_{rms} = I_{OUT} \times \left(\frac{D(\max) + (r / 12)}{1 - D} \right)^{1/2} \ , \qquad (19)$$

where:

$$r = \Delta I_L / I_{BAT}(max) \ , \text{ and} \qquad (20)$$

$$\Delta I_L = \left(\frac{V_{BAT}(\min) \times D}{L_{(used)} \times f_{SW}} \right) \ . \qquad (21)$$

Substituting:

$$(80\ mA \times 3) \times \{[0.75 + (0.3 / 12)]/(1 - 0.75)\}^{1/2} = 0.422\ A$$

Select a capacitor with an RMS current rating greater than 0.422 A.

8. Select input capacitor CIN, given:

$$C_{IN} = \Delta I_L / (8 \times f_{SW} \times \Delta V_{INripple}) \ , \qquad (22)$$

where $\Delta V_{INripple}$ is the input ripple voltage, which can be assumed to be 1% of V_{BAT}. Then:

$$C_{IN} = 0.3 / (8 \times 2 \times 10^6 \times 0.01 \times 8) = 0.23\ \mu F \ .$$

Select a 2.2 µF or higher, 35 or 50 V, ceramic capacitor, X5R or X7R grade.

The RMS current through CIN is given by:

$$I_{INRMS} = (I_{OUT} \times r) / [(1 - D) \times 12^{1/2}], \qquad (23)$$

$$= [(80\ mA \times 3) \times 0.3] / [(1 - 0.75) \times 3.46] = 83\ mA \ .$$

Select a capacitor with an RMS current rating greater than 83 mA.

9. Select the boost diode D1 (connect between the SW pins and the output). D1 should be a Schottky diode with low forward drop and junction capacitance.

   The diode reverse voltage rating should be greater than V_{OUT}. A 40 to 50 V diode rating is recommended.

   The diode DC current rating should be greater than I_{OUT} and the peak repetitive current rating should be > I_{BAT}(max) + ΔI_L / 2.

10. Select the compensation capacitor CCOMP (connect between the COMP pin and ground). Typically, use a 1 µF capacitor to reduce audio hum during PWM dimming.

11. Calculate Power Loss. Calculate power loss at various operating conditions to estimate worst-case power dissipation.

    A. Loss in LED drive:

    $I_{LEDx} \times V_{LEDx}$ for one string

    $$+ (I_{LEDx} \times V_{LEDx}(av) + 0.75$$

    $$\times \textit{ quantity of remaining enabled LED strings}), \qquad (24)$$

    where V_{LEDx} is the regulation voltage of the LEDx pins, 0.75 V typical, and worst-case drop is mismatch due to LED V_f.

    A good approximation for V_{LEDx}(av) is 0.8 V. This assumes that some of the remaining strings will regulate below, and some above, a value of 1.55 V. If the predicted

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

LED matching is tighter, then a lower value can be used. If the predicted LED mismatch is large, then a higher value should be used. To get the complete and accurate power dissipation, the user will need to measure each individual LED pin to get the exact V_{LED} voltage:

$$(80\ mA \times 0.75) + [80\ mA \times 2 \times (0.8 + 0.75)] = 0.308\ W$$

B. Loss in low drop-out regulator (LDO) + bias:

$$P_{LDO} = V_{BAT}(max) \times I_{BIAS}, \quad (25)$$

with bias current during switching 17 mA typical.

C. Boost switch conduction loss:

$$I^2_{BAT}(max) \times D \times R_{DS(on)} \times (1 + r^2/12), \quad (26)$$

where:

$$r = \Delta I_L / I_{BAT}(max). \quad (27)$$

D. Boost switch switching loss:

$$V_{OUT} \times I_{BAT}(max) \times (t_{rise} + t_{fall}) \times f_{SW}. \quad (28)$$

Switch loss calculations assume negligible input gate charge on internal boost MOSFET until $V_{G(th)}$ (gate threshold), compared to the Miller charge; t_{rise} and t_{fall} are measured in the lab under full load conditions. To approximate this value, use 5 ns for rise and fall times.

E. Diode loss:

$$Diode\ switching\ loss = 0.2 \times C_d \times V^2_{OUT} \times f_{SW}, \quad (29)$$

where C_d is the average junction capacitance of the Schottky diode. Then:

$$Diode\ conduction\ loss = V_f \times I_{BAT}(max) \times (1–D) \quad (30)$$

F. Inductor DCR loss:

$$I^2_{IN} \times R_{DC} \times (1 + r^2/12). \quad (31)$$

G. Inductor core loss:

This value is an estimate. The default value would be 50 mW at 1 A ripple current, and then scaled based on ripple current.

H. Power loss in output disconnect switch:

$$P_{SWDISC(on)} = R_{ODS(on)} \times I_{OUT}^2, \quad (32)$$

If the Output Disconnect Switch On-Resistance, $R_{ODS(on)}$, is 2 Ω, then:

$$P_{SWDISC(on)} = 2 \times 0.24^2 = 0.11\ W.$$

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

TYPICAL APPLICATION CIRCUITS

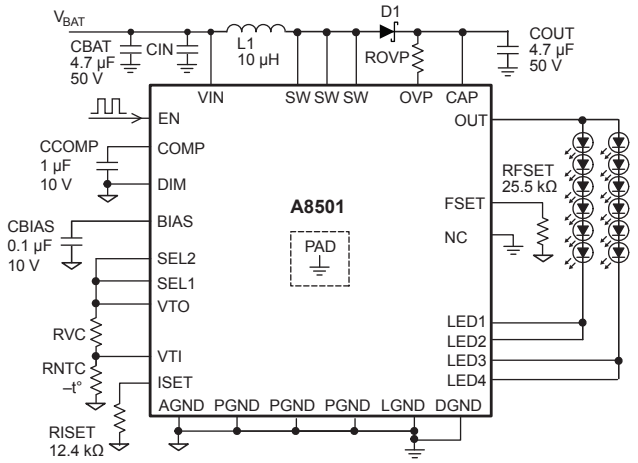


Figure 7: Typical Circuit for Driving 2 LED Strings at Up To 35 V at 200 mA per LED String, with Thermal Derating

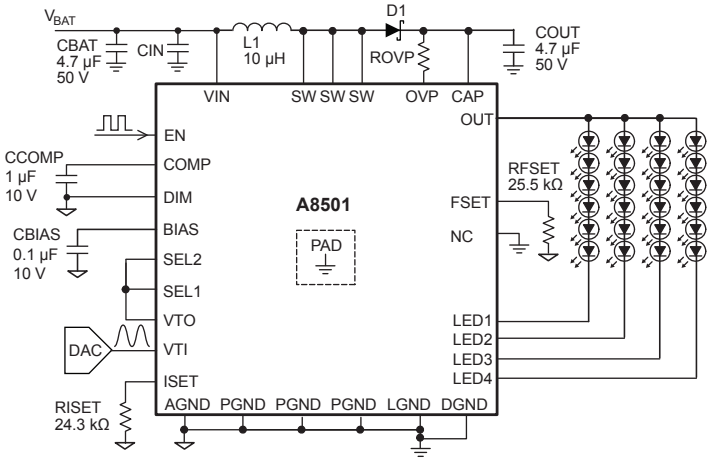


Figure 8: Typical Circuit for Analog Dimming with External DC Voltage

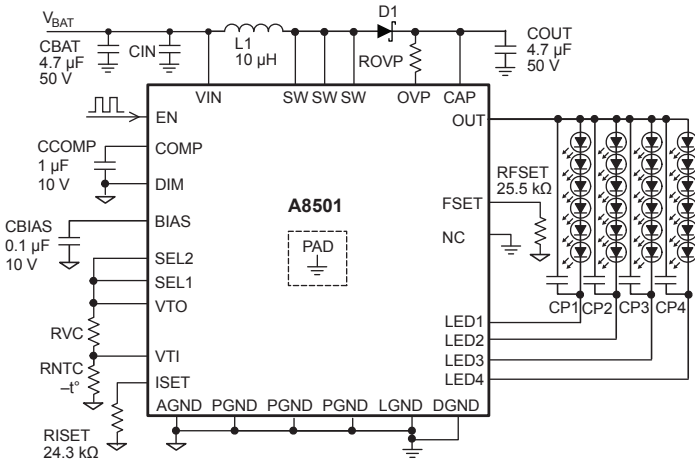


Figure 9: Typical Circuit with ESD Capacitors Across LEDs (CPx ≤10 nF), with Thermal Derating

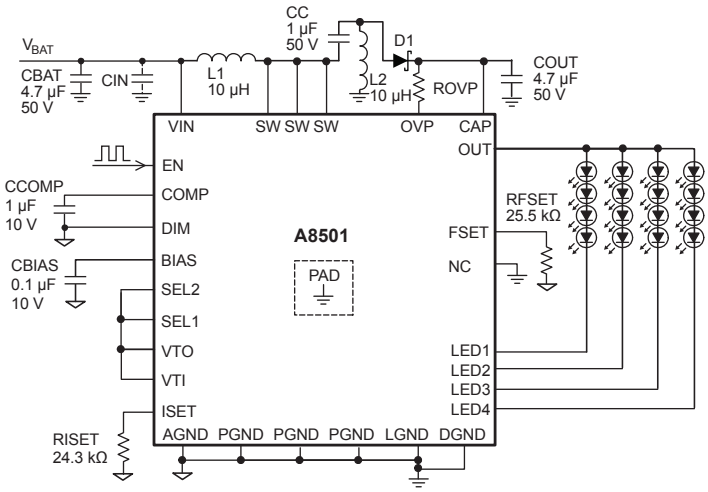


Figure 10: Typical Circuit as SEPIC Converter

(SEPIC converters can provide output voltage higher or lower than the input voltage; this topology can be used if the required output voltage level is within application input voltage range)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference MO-153 AET)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

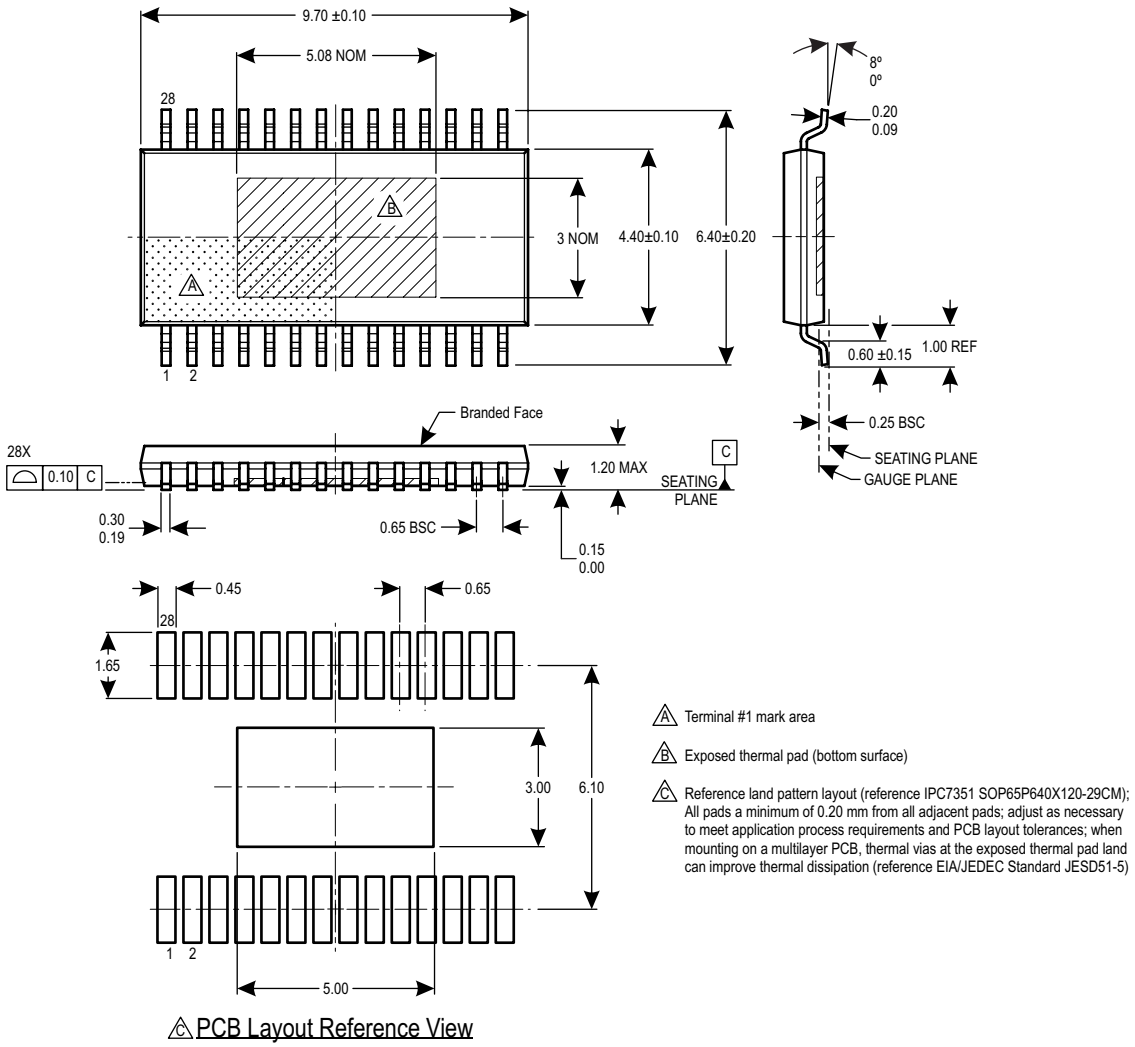


Figure 11: Package LP, 28-Pin TSSOP with Exposed Thermal Pad

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
5	November 17, 2014	Revised startup sequence.
6	February 7, 2019	Product status changed to Not for New Design.
7	March 4, 2019	Updated Selection Guide (page 2)
8	March 17, 2020	Minor editorial updates

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com